**PHILIPS**

Data handbook

Electronic
components
and materials

# Integrated circuits

Book IC08 1986

# ECL 10K and 100K logic families

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# ECL 10K and 100K logic families

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# DATA HANDBOOK SYSTEM

Our Data Handbook System comprises more than 60 books with specifications on electronic components, subassemblies and materials. It is made up of four series of handbooks:

| | |
|---|---|
| ELECTRON TUBES | BLUE |
| SEMICONDUCTORS | RED |
| INTEGRATED CIRCUITS | PURPLE |
| COMPONENTS AND MATERIALS | GREEN |

The contents of each series are listed on pages iv to viii.

The data handbooks contain all pertinent data available at the time of publication, and each is revised and reissued periodically.

When ratings or specifications differ from those published in the preceding edition they are indicated with arrows in the page margin. Where application information is given it is advisory and does not form part of the product specification.

Condensed data on the preferred products of Philips Electronic Components and Materials Division is given in our Preferred Type Range catalogue (issued annually).

Information on current Data Handbooks and on how to obtain a subscription for future issues is available from any of the Organizations listed on the back cover.
Product specialists are at your service and enquiries will be answered promptly.

# ELECTRON TUBES (BLUE SERIES)

The blue series of data handbooks comprises:

| | |
|---|---|
| **T1** | **Tubes for r.f. heating** |
| **T2a** | **Transmitting tubes for communications, glass types** |
| **T2b** | **Transmitting tubes for communications, ceramic types** |
| **T3** | **Klystrons** |
| **T4** | **Magnetrons for microwave heating** |
| **T5** | **Cathode-ray tubes**<br>Instrument tubes, monitor and display tubes, C.R. tubes for special applications |
| **T6** | **Geiger-Müller tubes** |
| **T8** | **Colour display systems**<br>Colour TV picture tubes, colour data graphic display tube assemblies, deflection units |
| **T9** | **Photo and electron multipliers** |
| **T10** | **Plumbicon camera tubes and accessories** |
| **T11** | **Microwave semiconductors and components** |
| **T12** | **Vidicon and Newvicon camera tubes** |
| **T13** | **Image intensifiers and infrared detectors** |
| **T15** | **Dry reed switches** |
| **T16** | **Monochrome tubes and deflection units**<br>Black and white TV picture tubes, monochrome data graphic display tubes, deflection units |

# SEMICONDUCTORS (RED SERIES)

The red series of data handbooks comprises:

| | |
|---|---|
| **S1** | **Diodes**<br>Small-signal silicon diodes, voltage regulator diodes (< 1,5 W), voltage reference diodes, tuner diodes, rectifier diodes |
| **S2a** | **Power diodes** |
| **S2b** | **Thyristors and triacs** |
| **S3** | **Small-signal transistors** |
| **S4a** | **Low-frequency power transistors and hybrid modules** |
| **S4b** | **High-voltage and switching power transistors** |
| **S5** | **Field-effect transistors** |
| **S6** | **R.F. power transistors and modules** |
| **S7** | **Surface mounted semiconductors** |
| **S8a** | **Light-emitting diodes** |
| **S8b** | **Devices for optoelectronics**<br>Optocouplers, photosensitive diodes and transistors, infrared light-emitting diodes and infrared sensitive devices, laser and fibre-optic components |
| **S9** | **Power MOS transistors** |
| **S10** | **Wideband transistors and wideband hybrid IC modules** |
| **S11** | **Microwave transistors** |
| **S12** | **Surface acoustic wave devices** |
| **S13** | **Semiconductor sensors** |

# INTEGRATED CIRCUITS (PURPLE SERIES)

The NEW SERIES of handbooks is now completed. With effect from the publication date of this handbook the "N" in the handbook code number will be deleted.
Handbooks to be replaced during 1986 are shown below.

The purple series of handbooks comprises:

| | | |
|---|---|---|
| **IC01** | **Radio, audio and associated systems**<br>Bipolar, MOS | new issue 1986<br>IC01N 1985 |
| **IC02a/b** | **Video and associated systems**<br>Bipolar, MOS | new issue 1986<br>IC02Na/b 1985 |
| **IC03** | **Integrated circuits for telephony**<br>Bipolar, MOS | new issue 1986<br>IC03N 1985 |
| **IC04** | **HE4000B logic family**<br>CMOS | new issue 1986<br>IC4 1983 |
| **IC05N** | **HE4000B logic family — uncased ICs**<br>CMOS | published 1984 |
| **IC06N** | **High-speed CMOS; PC74HC/HCT/HCU**<br>Logic family | published 1986 |
| **IC08** | **ECL 10K and 100K logic families** | New issue 1986<br>IC08N 1984 |
| **IC09N** | **TTL logic series** | published 1986 |
| **IC10** | **Memories**<br>MOS, TTL, ECL | new issue 1986<br>IC7 1982 |
| **IC11N** | **Linear LSI** | published 1985 |
| **Supplement to IC11N** | **Linear LSI** | published 1986 |
| **IC12** | **I$^2$C-bus compatible ICs** | not yet issued |
| **IC13** | **Semi-custom**<br>Programmable Logic Devices (PLD) | new issue 1986<br>IC13N 1985 |
| **IC14N** | **Microprocessors, microcontrollers and peripherals**<br>Bipolar, MOS | published 1985 |
| **IC15** | **FAST TTL logic series** | new issue 1986<br>IC15N 1985 |
| **IC16** | **CMOS integrated circuits for clocks and watches** | first issue 1986 |
| **IC17** | **Integrated Services Digital Networks (ISDN)** | not yet issued |
| **IC18** | **Microprocessors and peripherals** | new issue 1986* |

* The Microprocessors were included in handbook IC14N 1985, so IC18 will replace that part of IC14N.

# COMPONENTS AND MATERIALS (GREEN SERIES)

The green series of data handbooks comprises:

| | |
|---|---|
| **C2** | **Television tuners, coaxial aerial input assemblies, surface acoustic wave filters** |
| **C3** | **Loudspeakers** |
| **C4** | **Ferroxcube potcores, square cores and cross cores** |
| **C5** | **Ferroxcube for power, audio/video and accelerators** |
| **C6** | **Synchronous motors and gearboxes** |
| **C7** | **Variable capacitors** |
| **C8** | **Variable mains transformers** |
| **C9** | **Piezoelectric quartz devices** |
| **C11** | **Varistors, thermistors and sensors** |
| **C12** | **Potentiometers, encoders and switches** |
| **C13** | **Fixed resistors** |
| **C14** | **Electrolytic and solid capacitors** |
| **C15** | **Ceramic capacitors** |
| **C16** | **Permanent magnet materials** |
| **C17** | **Stepping motors and associated electronics** |
| **C18** | **Direct current motors** |
| **C19** | **Piezoelectric ceramics** |
| **C20** | **Wire-wound components for TVs and monitors** |
| **C22** | **Film capacitors** |

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# Introduction

**ECL Products**

## EMITTER-COUPLED LOGIC (ECL)

Emitter-coupled logic is the fastest logic technology available for practical use. Traditionally developed for the high-speed elements of mainframe computers, it is being applied wherever ultra-high switching speeds are required. Typical applications include signal generations and processing, digital switching and filtering networks, arithmetic and logic units of computers, optical transmission line interfaces and digital video systems.

This data manual describes the 10K and 100K ECL series. Other ECL products such as ECL Memories, are available from the Bipolar Memory family and ECL semicustom products, such as Advanced Customized ECL (ACE), are available from the Application Specific Division.

| LOGIC FAMILIES | GATE DELAY ns | POWER CONSUMPTION mW |
|---|---|---|
| **Conventional Logic** | | |
| TTL | 10 | 10 |
| LS TTL | 9 | 2 |
| S TTL | 3 | 20 |
| 10K ECL | 2 | 25 |
| **Advanced Logic** | | |
| FAST | 2 | 4 |
| 100K ECL | 0.75 | 40 |

## GENERAL

The Logic Families table compares the propagation delay and power consumption per gate of 10K and 100K ECL to other logic families.

ECL is a current switching logic. In the basic gate of Figure 1, the current from the current source flows continuously through either branch A or branch B. The exponential change of emitter current with base-emitter voltage results in rapid switching of the current path and allows a considerable amount of noise immunity to be built into the circuits. Furthermore, the constant current nature of the circuits minimizes voltage fluctuations (noise) due to switching in the supply lines, eliminating the need for ultra-fast, expensive voltage regulators. The effects of switching output loads are isolated from the inputs by the use of separate $V_{CC}$ supplies for the outputs.

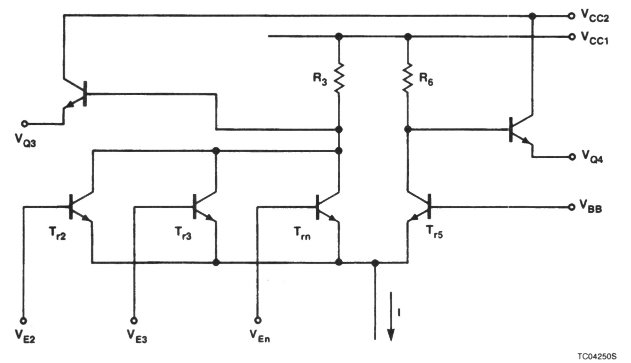


**Figure 1. ECL is a Current-Switching Logic. The Current Drawn From the Supply Voltage ($V_{CC1}$) is thus Independent of the State of the Inputs. The Use of a Separate Supply ($V_{CC2}$) for the Output Load Minimizes the Effect of Output Noise on the Inputs.**

Since there are no internal output load resistors, outputs can be OR-wired, thus saving additional circuitry. Most devices in the family provide complementary outputs, allowing simpler system design and eliminating inverters that would otherwise increase power consumption and circuit cost.

The 100K ECL series is fully compensated for changes in both temperature and voltage, in both the internal bias generator and the output circuitry. Therefore, 100K ECL provides easier thermal management than the 10K or 10H series, which do not provide full temperature compensation in their output voltage circuitry.

The high current drive capability of the 100K ECL, as shown in the table on this page, is a valuable feature when switching signals at speeds requiring transmission line techniques. High current drive contributes to the signal-to-noise ratio achieved at the receiving end. It also permits a large fan-out, since all inputs have an internal pull-down resistor of typically 50,000Ω to $V_{EE}$.

## TECHNICAL FEATURES OF ECL

### The Technology

A conventional planar process is used for the 10K ECL series with a density of about ten gates per mm$^2$ and a delay of 2ns per gate. This junction-isolated process achieves a 1.5GHz transition frequency.

To achieve the 0.75ns per gate delay and 20 gates per mm$^2$ density of 100K ECL, an oxide-isolated SUBILO (**SUB**nanosecond **I**solation by **L**ateral **O**xidation) process is used. This process achieves a transition frequency of about 4.5GHz.

### What ECL Provides

a) First of all, ECL provides very high speed, enabling high frequency operation.

b) Furthermore, the power consumption required (although high for a simple gate) increases less rapidly than the complexity of the functions in an integrated circuit.

c) Moreover, thanks to ECL, it is possible to process fast phenomena in real time (e.g., monitoring of nuclear phenomena, time bases for oscilloscopes; and, in general, all measurements whose resolution should be less than one nanosecond).

d) ECL also makes it possible to treat very complex phenomena in real-time (e.g., meteorology, the management of power networks, or of very large databases (in the case of large computers in which processing time is the determining factor)).

e) Lastly, ECL makes it possible to optimize the cost of a system by accelerating the subsystems that must respond rapidly (such as an ECL multiplier in a TTL computer).

## When to Use ECL

ECL should be used when a gain in speed beyond that achievable with saturating logic families is necessary.

ECL makes it possible to improve the cost of a system. For example, in telecommunications and in data communication, the increase in the line rate makes it possible to use fewer lines, thereby reducing the overall system cost and system maintenance.

ECL should be used for data rates greater than 100 mega bits per second.

## Where to Use ECL

### a) Large-scale Computation

- Any CPU having a cycle time between 10 and 50ns is partly *or* entirely ECL.
- Likewise, high-speed I/O controllers (access channels to disks, memory blocks, high-speed peripherals, or to other processors.)
- Memories having very fast access time are ECL (buffer or "cache" memories, most of the time; but sometimes central memory too, for the fastest large computers).

### b) Small- and Medium-scale Computing

- It is possible to increase the power of a small, microprocessor-based system by adding onto its bus some high-speed hardware functions, such as adders, multipliers, fast Fourier transforms, correlators, etc.
- It is also possible to increase the power of such a system by realizing part or all of the processor itself in ECL.

### c) Instrumentation

ECL makes it possible to build:

- rapid logic or analog testers for components or boards;
- logic analyzers, for the simultaneous acquisition of the logic state of several channels or signals in a system that is being developed or maintained;
- high-speed oscilloscopes, with acquisition, storage, and digital processing of signals;
- very-high-resolution chronometers and high-speed frequency counters.

### d) Telecommunications

- ECL is presently being used in the development of computers that direct telephone switching centers.
- ECL also makes it possible to design new telephone centers that switch wide-based signals (from video or from data channels), or even multiplex many audio channels.
- Lastly, ECL makes it possible to realize high-rate inter-center connections (for concentration, coding, repeaters and regenerators, decoding, demultiplexing) via coaxial cables, optic cables, or microwaves.

### e) Real-time Digital Signal Processing

- ECL is the ideal technology for digital processing of television video signals (filtering, decoding, mixing, special effects, broadcasting).
- ECL also makes it possible to digitalize the principal functions of television sets.
- Real-time simulators of complex phenomena (such as flight simulators or artillery simulators) contain large portions in ECL.
- ECL also lends itself to radar-signal processing.

## COMPARISON WITH OTHER LOGIC FAMILIES; SELECTION CRITERIA

ECL contains essentially the principal functions of other logic families (gates, flip-flops, complex or MSI circuits).

With a few exceptions, the functions are classified according to the following order of their last three digits (with the prefix 10 XXX or 100 XXX):

| | |
|---|---|
| 100 to 109: | Simple gates |
| 110 to 119: | Complex gates and line receivers |
| 120 to 129: | Interfaces |
| 130 to 139: | Flip-flops, counters |
| 140 to 155: | Registers, memories, combination of latches and multiplexers |
| 156 to 179: | Combinatorial MSI (parity, priority, multiplexers, decoders, delay) |
| 180 to 189: | Arithmetic circuits (adders, ALUs) |
| 190 to 399: | Other special interfaces |
| 400 to 499: | High-capacity memories |
| 500 to 699: | Military series |
| 800 to 899: | Microprocessors and associated circuits |

It was not possible to reproduce exactly, under the same numbers, the logic functions existing in TTL, for the following reasons:

1. In general, ECL circuits require three power supply pins, as opposed to two for the TTL circuits. Therefore, the number of pins available for the input/output of logic signals is different.

2. The basic ECL gate performs an OR function, whereas the basic TTL gate performs an AND function.

3. ECL gates have built-in complementary outputs (Q and $\overline{Q}$), thus enabling great flexibility in use. The functions that utilize these outputs are special within the family, and often replace two TTL functions at the same time.

4. In the particular case of the ECL 100K series, the standard package contains 24 pins, thus enabling more complex functions, replacing several TTL types. Thus, a 100170 decoder can be configured as a 1 × 8 or a 2 × 4 device with high or low outputs, thus performing the functions of four TTL decoders.

5. Interface requirements are different for high-speed logic circuits, which normally only handle data, and for slower logic circuits that can be interfaced to display devices ("display drivers") or power devices.

ECL devices can be interfaced in the following ways:

- using short-distance transmission lines [for example, twisted(-pair) wires] with line transmitters having differential inputs;
- through ECL-level data buses, by bus drivers that can provide a high current on the bus, or else can be disconnected, loading it as little as possible, thus realizing the equivalent of tri-state TTL circuits;
- to other logic families; ECL 10K to ECL 100K, ECL to CMOS or to TTL. Specifically, to be able to interface ECL processors to MOS central memories at the TTL level, via bidirectional interfaces.

Table 1 summarizes the principal characteristics of the logic families.

Other high-speed circuits exist which, without strictly being part of the ECL logic families, do have inputs or outputs that are compatible with ECL levels, and rely largely on emitter-coupled techniques in their internal electral circuitry. VHF and UHF frequency dividers ("prescalers") utilized in counters and synthesizers are the best known examples; but multivibrators, phase comparators, analog converters, etc., also exist.

# Introduction

**Table 1. Principal Characteristics of Logic Families**

| PRINCIPAL CHARACTERISTICS | CMOS | | TTL-COMPATIBLE | | | | ECL | |
|---|---|---|---|---|---|---|---|---|
| | HC | HCT | TTL | LS | S | FAST | 10K | 100K |
| Supply Voltage (V) | | 5 | 5 | 5 | 5 | 5 | −5.2 | −4.5 |
| Supply Current (mA) | | 1.4 | 2 | 0.4 | 4 | 1 | 5 | 8 |
| Logic Swing (V) | 3 | 3 | 3 | 3 | 3 | 3 | 0.9 | 0.7 |
| Maximum Fanout | 10 | 10 | 10 | 20 | 10 | 30 | > 30 | > 30 |
| Typical Propagation Delay (ns) | 9 | 9 | 10 | 10 | 3 | 2.8 | 2 | 0.75 |
| Edge Rate (V/ns) | 0.5 | 0.5 | 0.35 | 0.2 | 2.0 | 2.0 | 0.3 | 0.5 |
| Maximum Frequency of a D-type Flip-Flop (MHz) | 15 | 15 | 15 | 25 | 75 | 100 | 125 | 400 |
| Loss of Speed due to Output Loading (ns/Load Utilized) | 1.2 | 1.2 | 0.6 | 0.3 | 0.3 | 0.1 | 0.1 | 0.07 |
| Figure of Merit | | | | | | | | |
| Simple Gate (pj) | 20 | 20 | 100 | 20 | 55 | 14 | 0 | 30 |
| Complex Function (pj) | | | | | | | 10 | 5 |
| Principle Package (pins) | 14, 16 | 14, 16 | 14, 16 | 14, 16 | 14, 16 | 14, 16 | 16 | 24 |
| Number of Product Types | 120 | 120 | > 100 | > 150 | > 100 | > 70 | 60 | 40 |
| Operating Range: Commercial | YES | YES | YES | YES | YES | YES | YES | YES |
| Military | YES | YES | YES | YES | YES | YES | NO | NO |

* Operating speed = 5MHz

**NOTE:**

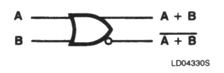
The sets of data given above is a very simplified representation of existing logic families. The values indicated are only approximate; they depend entirely on utilization conditions (supply voltage, loading conditions, etc.) and on the supplier.

## DESCRIPTION OF ECL FAMILIES

Two ECL families (the ECL 10K and the ECL 100K series) are presently considered standard (multiple vendors). The former contains more than 60 types, and the latter approximately 40.

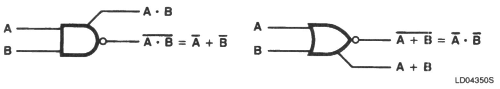
### Logic Diagrams

At the elementary-circuit level, the basic gate is an OR/NOR gate with two inputs and complementary outputs:



The fact that all of these gates have true and complementary (inverting) outputs makes it easier to implement logic diagrams.

Another worthwhile possibility is the **wired-OR** gate which enables the direct connection of the outputs of two gates to obtain an OR function.

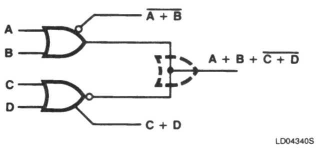

A
B
A · B
$\overline{A \cdot B} = \overline{A} + \overline{B}$
A
B
$\overline{A + B} = \overline{A} \cdot \overline{B}$
A + B
LD04350S

### Design of a Logic Diagram

ECL is based on OR/NOR gates. It is easy to transform AND/NAND gates into OR/NOR gates using the de Morgan laws:

$$A \cdot B = \overline{\overline{A} + \overline{B}} \text{ and } A + B = \overline{\overline{A} \cdot \overline{B}}$$

(A · B indicates an AND operation, A + B indicates an OR operation.)



Some ECL inputs are non-inverting, as opposed to TTL circuits in which these inputs are inverted; for example, the "clear" and "set to one" inputs (CLEAR and SET). This is due to the difference in design between TTL and ECL, in which the basic gates are AND and OR, respectively. Therefore, to "force" an input signal toward the output, a 0 or a 1 is applied, respectively. This requirement does not present a problem, because non-inverting and inverting outputs are almost always available on simple circuits.

Other ECL families have been created in the past, but they have not become as widely known as the others. Among them are MECL 1 and MECL 2, which were the original ECL families.

MECL 3 is fairly close to the performance to the ECL 100K family, but uses more power and is less complete. Lastly, an intermediate series exists between the 10K and 100K families. It retains the operation and speed of the former, and the temperature-compensated electrical levels of the latter.

The 10K family was recently rounded out by faster circuits (the 10KH series, with speeds from 1 to 1.2ns).

# Introduction

## Handling

Like MOS circuits, ECL circuits can easily be damaged by electrostatic discharge (ESD). ESD applied to an input or an output causes very intense, instantaneous currents. When passing through junctions having a small area, these currents can cause a localized fusion of the junction. In the mild case, there will be an increase in the junction leakage current; in the worst case, the junction will be completely short-circuited. The short-circuit can then cause a local fusion of the metallizations of the circuit, and the appearance of an open circuit.

The resistance of TTL and MOS circuits to ESD is increased by the addition of diodes or resistor-diode networks. However, this solution has very limited application in ECL, because it introduces parasitic capacitances that impair the speed of the circuits. Protection is instead ensured by simply limiting discharge currents by means of resistors in series.

All insulators can acquire very high charges by rubbing against one another, or due to friction with moving air. Surface potentials of several tens of kilovolts are found on work-surfaces (laminates, PVC), on floor coverings (plastic flooring, pile carpeting), and on synthetic fabrics (nylon and acrylic). For the sake of prevention, conductive coverings are recommended for floors and work surfaces, connected to ground by resistive paths (1MΩ, for example.) Most risks can be avoided by having operators wear resistive wristbands connected to the work surface. But complete protection must also include a sprayed layer of anti-static varnish on all insulating objects, such as boxes, trays, the insulating portions of tools; or also (if applicable) an ionized air blower, to remove charges from untreated surfaces.

Signetics' ECL devices are shipped in conducting foam or anti-static tubes and foil-lined boxes to minimize ESD during shipment and unloading.

Before opening the shipment of ECL devices, make sure that the individual is grounded by a wrist-band connected to ground by a 1MΩ resistor and all handling means (such as tools, fixtures, benches, and chairs) grounded through a 1MΩ resistor.

After removal from the shipping material, the leads of the ECL devices should always be grounded. In other words, ECL devices should be placed leads-down on a grounded surface, since ungrounded leads will attract static charge.

Before assembly of ECL devices, again make sure that the individual is grounded by a wrist-band connected to ground by a 1MΩ resistor and all handling means (such as tools, fixtures, benches, and chairs) grounded through a 1MΩ resistor.

Do not insert or remove ECL devices in sockets with power applied. Ensure that power supply transients, such as occur during power turn on-off, do not exceed absolute maximum ratings.

After assembly on PC boards, ensure that ESD is minimized during handling, storage, or maintenance.

ECL inputs should never be left floating on a PC board. As a temporary measure, a resistor greater than 10kΩ should be soldered on the open input. The resistor will limit accidental damage if the PC board is removed and brought into contact with static-generating materials.

**Signetics**

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# Ordering Information

Signetics' ECL products are available in 16-pin plastic and ceramic packages for 10K ECL and 24-pin ceramic DIP and flat pack packages for 100K ECL with two temperature ranges (0°C to +85°C for 100K ECL and −30°C to +85°C for 10K ECL). The ordering code for the devices is an alphanumeric sequence as explained below. The ordering codes in the individual data sheets indicate the normal or planned availability of the product. However, the availability of the specific part numbers can be obtained from local Signetics sales offices or franchised distributors.

100101 N

N — Package style

100101 — Device Number

| TEMPERATURE RANGE | DEVICE NUMBER | PACKAGE STYLE |
|---|---|---|
| Commercial Range<br>$T_A = -30°C$ to $+85°C$ | 10100 | N = Plastic DIP<br>F = Cerdip |
| Commercial Range<br>$T_A = 0°C$ to $+85°C$ | 100101 | F = Cerdip<br>Y = Ceramic Flat Pack |

# Product Status

## DEFINITIONS

| Data Sheet Identification | Product Status | Definition |
|---|---|---|
| *Objective Specification* | **Formative or In Design** | This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice. |
| *Preliminary Specification* | **Preproduction Product** | This data sheet contains preliminary data and supplementary data will be published at a later date. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |
| *Product Specification* | **Full Production** | This data sheet contains Final Specifications. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |

# Section 1
# Selection Guides

ECL Products

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# 10K ECL
## Availability Guide

**ECL Products**

### 10K ECL SERIES

| DEVICE TYPE | DESCRIPTION | AVAIL. | COMMENTS |
|---|---|---|---|
| 10100 | Quad 2-Input NOR Gate | A | |
| 10101 | Quad OR/NOR Gate | A | |
| 10102 | Quad 2-Input NOR Gate | A | |
| 10103 | Quad 2-Input OR Gate | A | |
| 10104 | Quad 2-Input AND Gate | A | |
| 10105 | Triple 2-3-2-Input OR/NOR Gate | A | |
| 10106 | Triple 4-3-3-Input NOR Gate | A | |
| 10107 | Triple 2-Input Exclusive-OR/Exclusive-NOR Gate | A | |
| 10108 | Dual 3-Input AND/NAND Gate | A | |
| 10109 | Dual 4-5-Input OR/NOR Gate | A | |
| 10110 | Dual 3-Input/3-Output OR Gate (Line Driver) | A | |
| 10111 | Dual 3-Input/3-Output NOR Gate (Line Driver) | A | |
| 10113 | Quad Exclusive-OR Gate With Enable | A | |
| 10114 | Triple Line Receiver | A | |
| 10115 | Quad Line Receiver | A | |
| 10116 | Triple Line Receiver | A | |
| 10117 | Dual 2-Wide 2-3-Input OR-AND/OR-AND-INVERT Gate | A | |
| 10118 | Dual 2-Wide 3-Input OR-AND Gate | A | |
| 10119 | 4-Wide 4-3-3-3-Input OR-AND Gate | A | |
| 10121 | 4-Wide OR-AND/OR-AND-INVERT Gate | A | |
| 10123 | Triple 4-3-3-Input Bus Driver | A | |
| 10124 | Quad TTL-to-ECL Translator | A | |
| 10125 | Quad ECL-to-TTL Translator | A | |
| 10130 | Dual D-Type Latch | A | |
| 10131 | Dual D-Type Master-Slave Flip-Flop | A | |
| 10132 | Dual 2-Input Multiplexer With Clocked D-Type Latches and Common Reset | A | |
| 10133 | Quad Latch With D-Type Inputs and Enable Outputs | A | |
| 10134 | Dual 2-Input Multiplexer With Clocked D-Type Latches | A | |
| 10135 | Dual J-K Master-Slave Flip-Flop | A | |
| 10136 | Universal Hexadecimal Counter | A | |
| 10137 | Universal Decade Counter | A | |
| 10141 | 4-Bit Universal Shift Register | A | |
| 10149 | 1024-Bit, 4 Bits per Word PROM | A | |
| 10155 | 16-Bit, 2 Bits per Word CAM | A | |
| 10158 | Quad 2-to-1 Multiplexer (Non-Inverting) | A | |

## 10K ECL SERIES (Continued)

| DEVICE TYPE | DESCRIPTION | AVAIL. | COMMENTS |
|---|---|---|---|
| 10159 | Quad 2-to-1 Multiplexer (Inverting) | A | |
| 10160 | 12-Bit Parity Generator/Checker | A | |
| 10161 | 3-Bit Decoder With 2 Enable Inputs (1-of-8 LOW) | A | |
| 10162 | 3-Bit Decoder With 2 Enable Inputs (1-of-8 HIGH) | A | |
| 10164 | 8-Input Multiplexer With Enable Input | A | |
| 10165 | 8-Input Priority Encoder | A | |
| 10171 | Dual 2-Bit Decoder (1-of-4 Lines LOW) | A | |
| 10172 | Dual 2-Bit Decoder (1-of-4 Lines HIGH) | A | |
| 10173 | Quad 2-Input Multiplexer With Latched Outputs | A | |
| 10174 | Dual 4-to-1 Multiplexer With Enable | A | |
| 10175 | Quint D-Latch With Common Reset and 2 Wire-OR Common Clock Inputs | A | |
| 10176 | Hex D-Type Master-Slave Flip-Flop | A | |
| 10179 | Look-Ahead Carry Block Arithmetic Functions | A | |
| 10180 | Dual High-Speed Adder/Subtractor | A | |
| 10181 | 4-Bit Logic Unit/Function Generator | A | |
| 10188 | Hex Buffer (Non-Inverting) | A | |
| 10189 | Hex Inverter | A | |
| 10192 | Quad Differential Line Driver | A | |
| 10210 | Dual 3-Input/3-Output (High-Speed) OR Gate | A | |
| 10211 | Dual 3-Input/3-Output (High-Speed) NOR Gate | A | |
| 10216 | Triple Differential OR/NOR Line Receiver (High-Speed) | A | |
| 10231 | Dual D-Type Master-Slave Flip-Flop (High-Speed) | A | |
| 10422B | 1024-Bit RAM (256 × 4) | P | Q1 '86 |
| 10470A | 4096-Bit RAM (4096 × 1) | P | Q1 '86 |
| 10474A | 4096-Bit RAM (256 × 4) | P | Q1 '86 |

# 100K ECL
## Availability Guide

**ECL Products**

### 100K ECL SERIES

| DEVICE TYPE | DESCRIPTION | AVAIL. | COMMENTS |
|---|---|---|---|
| 100101 | Triple 5-Input Gate | A | |
| 100102 | Quint 2-Input Gate | A | |
| 100107 | Quint Exclusive-OR/NOR | A | |
| 100112 | Quad Driver | A | |
| 100113 | Line Driver | A | |
| 100114 | Line Receiver | A | |
| 100117 | Triple AOI | A | |
| 100118 | 5-Wide AOI | A | |
| 100122 | 9-Bit Buffer Gate | A | |
| 100123 | Hex Bus Driver | A | |
| 100124 | TTL-to-ECL Translator | P | Q4 '86 |
| 100125 | ECL-to-TTL Translator | P | Q4 '86 |
| 100126 | Backplane Driver | A | |
| 100131 | Triple D Flip-Flop (2ns) | A | |
| 100136 | Multipurpose Counting Register | A | |
| 100141 | 8-Bit Universal Shift Register | A | |
| 100145 | 16 × 4 Register File | P | Samples Q4 '86 |
| 100150 | Hex D-Latch | A | |
| 100151 | Hex D Flip-Flop | A | |
| 100155 | Quad Multiplexer/Latch | A | |
| 100158 | Shift Matrix | A | |
| 100160 | Dual 9-Bit Parity | A | |
| 100163 | Dual 8-Input Multiplexer | A | |
| 100164 | 16-Input Multiplexer | A | |
| 100165 | Universal Priority Encoder | A | |
| 100166 | 9-Bit Comparator | A | |
| 100170 | Universal Decoder | A | |
| 100171 | Triple 4-Input Multiplexer | A | |
| 100175 | 100K – 10K Translator | A | Signetics Proprietary |
| 100179 | Carry Look-Ahead Generator | P | Samples Q2 '86 |
| 100180 | Fast 6-Bit Adder | A | |
| 100181 | 4-Bit Binary/Decimal ALU | A | New Release<br>Signetics Proprietary |
| 100255 | TTL – 100K Bidirectional Translator | A | Signetics Proprietary |
| 100422B | 1024-Bit RAM (256 × 4) | P | Q2 '86 |
| 100470A | 4096-Bit RAM (4096 × 1) | P | Q2 '86 |
| 100474A | 4096-Bit RAM (1024 × 4) | P | Q2 '86 |

Signetics

# Functional Selection Guide

**ECL Products**

## GATES

| FUNCTION | DEVICE NUMBER |
|---|---|
| **OR/NOR GATES** | |
| Triple 4-3-3 input NOR | 10106 |
| Quad 2-input NOR with strobe | 10100 |
| Dual 4-5 input OR/NOR | 10109 |
| Triple 2-3-2 input OR/NOR | 10105 |
| Triple 5-input OR/NOR | 100101 |
| Quad 2-input OR/NOR (one input common) | 10101 |
| Quint 2-input OR/NOR with common enable input | 100102 |
| Quad 2-input NOR (one input common) | 10102 |
| Quad 2-input OR (3 OR and 1 OR/NOR) | 10103 |
| **EXCLUSIVE-OR/NOR GATES** | |
| Quad Exclusive-OR with enable input | 10113 |
| Triple 2-input Exclusive-OR/Exclusive-NOR | 10107 |
| Quint Exclusive-OR/Exclusive-NOR with compare output | 100107 |
| **AND, AND/NAND GATES** | |
| Dual 4-input AND/NAND | 10108 |
| Quad 2-input AND | 10104 |
| **OR-AND-INVERT COMBINATION** | |
| Dual 2-wide 3 input OR-AND | 10118 |
| 4-wide 4-3-3-3 input OR-AND | 10119 |
| Dual 2-wide 2-3 input OR-AND/OR-AND-INVERT | 10117 |
| 4-wide OR-AND/OR-AND-INVERT | 10121 |
| Triple 1-2-2 input OR-AND/OR-AND-INVERT | 100117 |
| Quint 2-4-4-4-5 input OR-AND/OR-AND-INVERT | 100118 |

## FLIP-FLOPS

| FUNCTION | DEVICE NUMBER | COMMON CLOCK | CLOCK ENABLE | SET | RESET |
|---|---|---|---|---|---|
| Dual D-type master-slave | 10131 | LOW | LOW | LOW | LOW |
| Dual D-type master-slave (high-speed) | 10231 | LOW | LOW | LOW | LOW |
| Triple D-type master-slave | 100131 | LOW | LOW | LOW | LOW |
| Triple D-type master-slave (high-speed) | 100231 | LOW | | | |
| Hex D-type master-slave | 10176 | LOW | | | |
| Hex D-type master-slave | 100151 | | | | LOW |
| Dual J-K master-slave | 10135 | LOW | LOW | LOW | LOW |

# Functional Selection Guide

## LATCHES

| FUNCTION | DEVICE NUMBER | COMMON CLOCK | RESET | CLOCK ENABLE | OUTPUT |
|---|---|---|---|---|---|
| Dual D-type 2-input multiplexer, clock, and common reset | 10132 | HIGH | HIGH | LOW | True, Comp |
| Dual D-type 2-input multiplexer, clock, and common reset | 10134 | LOW | HIGH | LOW | True, Comp |
| Triple D-type | 100130 | LOW |  | LOW | True |
| Quad with D-type inputs and enable outputs | 10133 | HIGH |  | LOW | Comp |
| Quint D-type with common reset, and 2 wired-OR common clock inputs | 10175 | LOW | LOW |  | True |
| Hex D-type | 100150 |  | LOW | LOW | True, Comp |

## MULTIPLEXER

| FUNCTION | DEVICE NUMBER | ENABLE INPUT | SELECT INPUTS | OUTPUT |
|---|---|---|---|---|
| Quad 2-to-1, non-inverting | 10158 |  | S | True |
| Quad 2-to-1, inverting | 10159 | LOW | S | Comp |
| 8-input with enable input | 10164 | LOW | $A_{S0}$, $A_{S1}$, $A_{S2}$ | True |
| Quad 2-input with latch outputs | 10173 | LOW | $D_S$ | True |
| Dual 4-to-1 with enable input | 10174 | LOW | A, B | True |
| Quad multiplexer/latch | 100155 | LOW | $S_0$, $S_1$ | True & Comp |
| Dual 8-input | 100163 |  | $S_0$, $S_1$, $S_2$ | Comp |
| Triple 4-input with enable input | 100171 | LOW | $S_0$, $S_1$ | True & Comp |
| 16-input | 100164 |  | $S_0$, $S_1$, $S_2$, $S_3$ | Comp |

## DECODER/DEMULTIPLEXER

| FUNCTION | DEVICE NUMBER | ADDRESS INPUT | ENABLE LEVEL | OUTPUT LEVEL |
|---|---|---|---|---|
| 1-of-8 decoder with 2 enable inputs (active LOW outputs) | 10161 | 3 | 2 (LOW) | 8 (LOW) |
| 1-of-8 decoder with 2 enable inputs (active HIGH outputs) | 10162 | 3 | 2 (LOW) | 8 (HIGH) |
| Dual 1-of-4 decoder with one common and two individual inputs (active LOW outputs) | 10171 | 2 | 2 (HIGH), 1 (LOW) | 1 (LOW) |
| Dual 1-of-4 decoder with one common and two individual inputs (active HIGH outputs) | 10172 | 2 | 2 (LOW), 1 (HIGH) | 8 (HIGH) |
| Universal demultiplexer/decoder | 100170 | 5 | 4 (LOW) | 8 (HIGH) |

## REGISTERS/SHIFT REGISTERS

| FUNCTION | DEVICE NUMBER | BITS | SERIAL ENTRY | PARALLEL ENTRY | CLOCK EDGE |
|---|---|---|---|---|---|
| 4-bit universal shift register | 10141 | 4 | $D_n$ | $D_0$, $D_1$, $D_2$, $D_3$ | ↑ |
| 8-bit shift register | 100141 | 8 | $D_n$ | $P_0,\cdots\cdots\cdots,P_7$ | ↑ |
| 16 × 4 read-while-write Register file | 100145 | 16 × 4 |  |  |  |
| 8-bit shift matrix | 100158 | 8 |  | $D_0,\cdots\cdots\cdots,D_7$ |  |

# Functional Selection Guide

## COUNTERS

| FUNCTION | DEVICE NUMBER | MODULUS | PARALLEL ENTRY | PRESETTABLE | CLOCK EDGE |
|---|---|---|---|---|---|
| Universal hexadecimal | 10136 | 16 | Synchronous | X | ↑ |
| Universal decade | 10137 | 10 | Synchronous | X | ↑ |
| 4-stage counter/shift register | 100136 | 4 | Synchronous | X | ↑ |

## BUS AND LINE DRIVERS

| FUNCTION | DEVICE NUMBER | OUTPUT |
|---|---|---|
| Dual 3-input/3-output OR line driver | 10110 | True |
| High-speed dual 3-input/3-output OR line driver | 10210 | True |
| Dual 3-input/3-output NOR line driver | 10111 | Complement |
| High-speed dual 3-input/3-output NOR line driver | 10211 | Complement |
| Triple 4-3-3-input bus driver | 10123 | Complement |
| Quad current-mode differential bus driver | 10192 | True & Complement |
| Quad driver | 100112 | True & Complement |
| Quad driver (high-speed) | 100113 | True & Complement |
| Hex bus driver | 100123 | True |
| 9-bit backplane driver | 100126 | True |

## RECEIVERS

| FUNCTION | DEVICE NUMBER | OUTPUT |
|---|---|---|
| Triple differential line receiver | 10114 | True & Complement |
| Quad differential line receiver | 10115 | True |
| Triple differential line receiver | 10116 | True & Complement |
| Triple differential line receiver (high-speed) | 10216 | True & Complement |
| Quint differential line receiver | 100114 | True & Complement |

## BUFFERS, INVERTERS, TRANSLATORS

| FUNCTION | DEVICE NUMBER | OUTPUT |
|---|---|---|
| Hex buffer with enable input, non-inverting | 10188 | True |
| 9-gate buffer | 100122 | Complement |
| Hex inverter with enable input | 10189 | Complement |
| Quad TTL-to-ECL translator | 10124 | True & Complement |
| Hex TTL-to-ECL translator | 100124 | True |
| Quad ECL-to-TTL translator | 10125 | True |
| Hex ECL-to-TTL translator | 100125 | True |
| 100K-to-10K translator | 100175 | True |
| TTL-to-100K bidirectional translator | 100255 | True |

## PRIORITY ENCODERS

| FUNCTION | DEVICE NUMBER | INPUT ENABLE (LEVEL) | INPUT/OUTPUT (LEVEL) |
|---|---|---|---|
| 8-Input | 10165 | LOW | Active LOW |
| Universal | 100165 | LOW | Active LOW |

# Functional Selection Guide

## ARITHMETIC FUNCTIONS

| FUNCTION | DEVICE NUMBER |
|---|---|
| 4-bit arithmetic logic unit/function generator | 10181 |
| 4-bit binary/BCD ALU | 100181 |
| High-speed 6-bit adder | 100180 |
| Dual 2-bit adder/subtractor | 10180 |
| Look-ahead carry block | 10179 |
| Carry look-ahead generator | 100179 |

## COMPARATORS

| FUNCTION | DEVICE NUMBER |
|---|---|
| 9-bit comparator | 100166 |

## PARITY

| FUNCTION | DEVICE NUMBER |
|---|---|
| 12-bit parity checker/generator | 10160 |
| Dual 9-bit parity generator/8-bit comparator | 100160 |

## LSI

| FUNCTION | DEVICE NUMBER |
|---|---|
| 28-bit ALU | 100310 |
| 4-byte MUX | 100330 |
| 16 × 8 switching matrix | 100331 |
| 4-byte comparator with MUX | 100340 |
| High-speed FIFO RAM controller | 100380 |

## ECL RAMS

| FUNCTION | DEVICE NUMBER |
|---|---|
| 1K-bit (variable organization) | 10422B |
| | 10422C |
| | 100422B |
| | 100422C |
| 4K-bit (4096 × 1) | 10470A |
| | 100470A |
| 4K-bit (1024 × 4) | 10474A |
| | 100474A |

# Section 2
# Quality and Reliability

# Quality and Reliability

**ECL Products**

## SIGNETICS QUALITY

Signetics has put together a winning process for manufacturing ECL Logic. Our standard is zero defects, and current customer quality statistics demonstrate our commitment to this goal.

The ECL Logic produced in the Standard Products Division must meet rigid criteria as defined by our design rules and as evaluated with a thorough product characterization and quality process. The capabilities of our manufacturing process are measured and the results evaluated and reported through our corporate-wide QAO5 database system. The SURE (Systematic Uniform Reliability Evaluation) program monitors the performance of our product in a variety of accelerated environmental stress conditions. All of these programs and systems are intended to prevent product-related problems and to inform our customers and employees of our progress in achieving zero defects.

## RELIABILITY BEGINS WITH THE DESIGN

Reliability and quality must begin with design. No amount of extra testing or inspection will produce reliable ICs from a design that is inherently unreliable. Signetics follows very strict design and layout practices with its digital circuits. To eliminate the possibility of metal migration, current density in any path cannot exceed $1 \times 10^5$Amp/cm$^2$ for 10K ECL and $2 \times 10^5$Amp/cm$^2$ for 100K ECL. Layout rules are followed to minimize the possibility of shorts, circuit anomalies, and SCR-type latch-up effects. Numerous ground-to-substrate connections are required to ensure that the entire chip is at the same potential, thereby precluding internal noise problems.

## PRODUCT CHARACTERIZATION

Before a new design is released, the characterization phase must be completed so that the distribution of parameters resulting from lot-to-lot variations is well within specified limits. Such extensive characterization data also provides a basis for identifying unique application-related problems which are not part of normal data sheet guarantees. Characterization takes place from 0°C to +85°C and at ±10% supply voltage.

## QUALIFICATION

Formal qualification procedures are required for all new or changed products, processes and facilities. These procedures ensure the high level of product reliability our customers expect. New facilities are qualified by corporate groups as well as by the quality organizations of specific units that will operate in the facility. After qualification, products manufactured by the new facility are subjected to highly accelerated environmental stresses to ensure that they can meet rigorous failure rate requirements. New or changed processes are similarly qualified.

## QAO5

The QAO5 system collects the results of product assurance testing on all finished goods lots and feeds this data back to concerned organizations where appropriate action can be taken. The QAO5 reports EPQ (Estimated Process Quality) and AOQ (Average Outgoing Quality) results for electrical visual/mechanical, hermeticity, and documentation audits. Data from this system is available on request.

## THE SURE PROGRAM

The SURE (Systematic Uniform Reliability Evaluation) program audits/monitors products from all Signetics' divisions under a variety of accelerated environmental stress conditions. This program, first introduced in 1964, has evolved to suit changing product complexities and performance requirements.

The SURE program has two major functions: Long-term accelerated stress performance audit and a short-term accelerated stress monitor. In the case of ECL Logic products, samples are selected that represent all generic product groups in all wafer fabrication and assembly locations.

## THE LONG-TERM AUDIT

One hundred devices are subjected to each of the following stresses every eight weeks:

- High Temperature Operating Life: $T_J = 150°C$, 1000 hours, static biased
- High Temperature Storage: $T_J = 150°C$, 1000 hrs
- Temperature-Humidity-Biased Life: 85°C, 85% relative humidity, 1000 hrs, static biased
- Temperature Cycling (Air-to-Air): −65°C to +150°C, 100 cycles

## THE SHORT-TERM MONITOR

Ten parts of each process batch (25,000 pcs typ) are subjected to a High Temperature Operating Life XXX 125°C, 168 hours, reverse biased at $V_{EE} = -5V$.

## SURE REPORTS

The data from these test matrices provides a basic understanding of product capability, an indication of major failure mechanisms and an estimated failure rate resulting from each stress. This data is compiled periodically and is available to customers upon request.

Many customers use this information in lieu of running their own qualification tests, thereby eliminating time-consuming and costly additional testing.

## RELIABILITY ENGINEERING

In addition to the product performance monitors encompassed in the Logic SURE Program, Signetics' Corporate and Division Reliability Engineering departments sustain a broad range of evaluation and qualification activities.

Included in the engineering program are:

- — evaluation and qualification of new or changed materials, assembly/wafer-fab processes and equipment, product designs, facilities and subcontractor;
- — device or generic group failure rate studies;
- — advanced environmental stress development;
- — failure mechanism characterization.

The environmental stresses utilized in the engineering programs are similar to those utilized for the SURE monitor, however, more highly accelerated conditions and extended durations typify the engineering projects. Additional stress systems such as biased pressure pot, power-temperature cycling, and cycle-biased temperature-humidity, are also included in the evaluation programs.

## FAILURE ANALYSIS

The SURE Program and the Reliability Engineering Program both include failure analysis

# Quality and Reliability

activities and are complemented by Corporate, Divisional, and Plant Failure Analysis departments. These engineering units provide a service to our customers who desire detailed failure analysis support, and they in turn provide Signetics with the technical understanding of the failure modes and mechanisms actually experienced in service. This information is essential feedback necessary for the continued assessment of the applicability of the stress conditions utilized to measure product performance.

## ZERO DEFECTS PROGRAM

In recent years United States Industry, and particularly those of you who buy integrated circuits, has increasingly demanded improved product family. We at Signetics believe you have every right to expect quality products from a supplier. The benefits which are derived from quality products can be summed up in the words, lower cost of ownership. Those of you who invest in costly test equipment and engineering to assure that incoming products meet your specifications have a special understanding of the cost of ownership. But your cost does not end there; you are also burdened with inflated inventories, lengthened lead times, and more rework.

## SIGNETICS UNDERSTANDS CUSTOMERS' NEEDS

Signetics has long had an organization of quality professionals within the operating units, coordinated by a corporate quality department. This organization provides leadership, feedback, and direction for achieving our high level of quality. Special programs are targeted on specific quality issues. For example, a program to reduce electrically defective units improved outgoing quality levels by an order of magnitude.

In 1980 we recognized that in order to achieve outgoing levels on the order of 100 ppm (parts per million), down from an industry practice of 10,000 ppm, we needed to supplement our traditional quality programs with one that encompassed all activities and all levels of the company. Such unprecedented low levels could only be achieved by contributions from all employees, from the R&D laboratory to the shipping dock. In short, a program that would effect a total cultural change within Signetics in our attitude toward quality.

## QUALITY PAYS OFF FOR OUR CUSTOMERS

Signetics' dedicated programs in product quality improvement, supplemented by close working relationships with many of our customers, have improved outgoing product quality more than twenty-fold. Today, many major customers no longer test Signetics circuits. Incoming product moves directly from the receiving dock to the production line, greatly accelerating throughput and reducing inventories. Additional customers have pared significantly the amount of sampling done on our products. Others are beginning to adopt these cost-saving practices.

We closely monitor the electrical, visual, and mechanical quality of all our products and review each return to find and correct the cause. Since 1981, over 90% of our customers report a significant improvement in overall quality. (See Figure 1.)

At Signetics, quality means more than working circuits. It means on-time delivery of the right quantity of the product at the agreed upon price. (See Figure 2.) Our quality improvement programs extend out from the traditional areas of product performance into the administrative areas which affect order entry, scheduling, delivery, shipping, and invoicing.

## ONGOING QUALITY PROGRAM

### "Do it Right the First Time"

The intent of this innovative program is to change the perception of Signetics' employees that somehow quality is solely a manufacturing issue where some level of defects is inevitable. This attitude has been replaced by one of acceptance of the fact that all errors and defects are preventable; a point of view shared by technical and administrative functions equally, and, we are sure, welcomed by our customers.

This program extends into every area of the company, and more than 40 qualilty improvement teams throughout the organization drive its ongoing refinement and progress. Key components of the program are the Quality College, the "Make Certain" Program, Corrective Action Teams, and the Error Cause Removal System.

The core concepts of doing it right the first time are embodied in the four absolutes of quality:

1. The definition of quality is conformance to requirements.
2. The system to achieve quality improvement is prevention.
3. The performance standard is zero defects.
4. The measurement system is the cost of quality.

### Quality College

Almost continuously in session, the Quality College is a prerequisite for all management and technical employees. The intensive curriculum is built around the four "absolutes" of quality; colleges are conducted at company facilities throughout the world.

### "Making Certain" — Administrative Quality Improvement

Signetics' experience has shown that the largest source of errors affecting product and

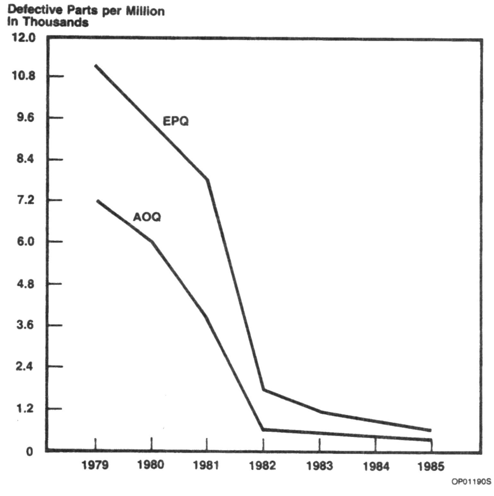

Figure 1. Signetics Quality Progress

# Quality and Reliability

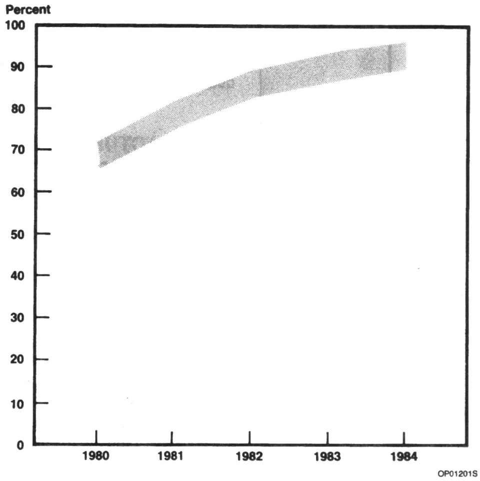

**Figure 2. Performance to Schedule On-Time Delivery**

service quality is found in paperwork and in other administrative functions. The "Make Certain" program focuses the attention of management and administrative personnel on error prevention, beginning with each employee's own actions.

This program promotes defect prevention in three ways: by educating employees as to the impact and cost of administrative errors, by changing attitudes from accepting occasional errors to one of accepting a personal work standard of zero defects, and by providing a formal mechanism for preventing errors.

### Corrective Action Teams

Employees with the perspective, knowledge, and necessary skills are formed into ad hoc groups called Correction Action Teams. These teams, the major force within the company for quality improvement, resolve administrative, technical and manufacturing problems.

### Error Cause Removal (ECR) System

The ECR System permits our employees to report to management any impedient to doing their job right the first time. Once reported, management is obliged to respond promptly with a corrective program. Doing it right the first time in all company activities produces lower cost of ownership through product defect prevention.

### Product Quality Program

To reduce defects in outgoing products to nearly immeasurable levels, we created the Product Quality Program. This is managed by the Product Engineering Council, a task force composed of the top product engineering and test professionals in the company. This group:

1. Sets aggressive product quality improvement goals.
2. Provides corporate-level visibility and focuses on problem areas.
3. Serves as a corporate resource for any group requiring assistance in quality improvement.
4. Drives quality improvement projects.

As a result of this aggressive program, every major customer who reports back to us on product performance is reporting significant progress.

### Standard Quality Programs

Qualification — Formal qualification procedures are required for all new or changed products, processes and facilities. These procedures ensure the high level of product reliability our customers expect. New facilities are qualified by the corporation and by the quality organizations of the product line that will operate the facility. After qualifications, products manufactured by the new facility are subjected to highly accelerated environmental stresses to ensure that the products can meet rigorous failure rate requirements. New or changed processes are qualified similarly.

Failure Analysis — This vital function is conducted by product line and plant failure analysis units coordinated through the corporate failure analysis group, a part of corporate reliability engineering. Our ten failure analysis groups were expanded to 16 during 1984 in our ongoing effort to accelerate and improve our understanding of product failure mechanisms.

Reliability Database — This computerized database contains product reliability information collected from around the world. It is updated and published quarterly in the "Signetics Product Reliability Summary".

Many customers use this information in lieu of running their own qualification tests, thereby eliminating time-consuming and costly procedures.

Vendor Certification Program — Our vendors are taking ownership of their own product quality by establishing improved process control and inspection systems. They subscribe to the zero defects philosophy. Progress has been excellent. Through intensive work with vendors, we have improved our lot acceptance rate on incoming materials as shown in Figure 3. Simultaneously, waivers of incoming material have been eliminated. Higher incoming quality material to us ensures higher outgoing quality products for you.

## QUALITY AND RELIABILITY ORGANIZATION

Quality and reliability specialists at the product-line level are involved in all aspects of the product, from design through every step in the manufacturing process, and provide product assurance testing of outgoing product. A separate corporate-level group provides direction and common facilities.

Quality and Reliability Functions

- Manufacturing quality control
- Product assurance testing
- Laboratory facilities — failure analysis, chemical, metallurgy, thin film, oxides
- Environmental stress testing
- Quality and reliability engineering
- Customer liaison

## COMMUNICATING WITH EACH OTHER

For information on Signetics' quality programs or for any question concerning product quality, the field representative in your area will provide you with the quickest access to answers. Or, write on your letterhead directly to the Corporate Director of Quality at the corporate address shown at the back of this data manual.

We are dedicated to preventing defects. When product problems do occur, we want to know about them so we can eliminate their causes. We are committed to zero defects.

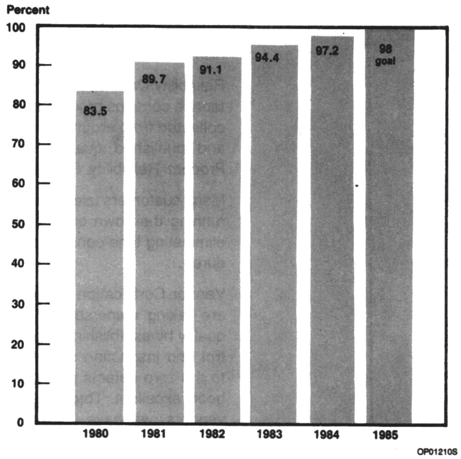

**Figure 3. Lot Acceptance Rate from Signetics Vendors**

Here are some ways we can help each other:

- Provide us with one informed contact within your organization. This will establish continuity and build confidence levels.
- Periodic face-to-face exchanges of data and quality improvement ideas between your engineers and ours can help prevent problems before they occur.
- Test correlation data is very useful. Line-pull information and field failure reports also help us improve product performance.
- Provide us with as much specific data on the problem as soon as possible to speed analysis and enable us to take corrective action.
- An advance sample of the devices in question can start us on the problem resolution before physical return of shipment.

This teamwork with you will allow us to achieve our mutual goal of improved product quality.

## MANUFACTURING: DOING IT RIGHT THE FIRST TIME

In dealing with the standard manufacturing flows, it was recognized that significant improvement would be achieved by "doing every job right the first time", a key concept of the quality improvement program. During the development of the program many profound changes are being made. Key changes include such things as implementing 100% AC testing on all products as well as upgrading test handlers to insure 100% positive binning. Some of the other changes and additions are to tighten the outgoing QA lot acceptance criteria to the tightest in the industry, with zero defect lot acceptance sampling across all three temperatures.

The achievements resulting from the improved process flow have helped Signetics to be recognized as the leading Quality supplier of ECL Logic. These achievements have also led to our participation in Ship-to-Stock programs, which our customers use to eliminate incoming inspection. Such programs reduce the user *cost of ownership* by saving both time and money.

# Section 3
# Testing

**ECL Products**

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# Testing

## ECL Products

## INTRODUCTION

The purpose of this section is to assist personnel involved with testing of ECL by discussing various testing methods and techniques needed in testing ECL devices.

## TEST SEQUENCE

ECL testing is usually done in the following sequence: functional testing, DC testing and AC testing.

### Functional Testing

The purpose of functional testing is to verify that the device is working. Functional testing is done on the automatic tester by simulating in-circuit condition. The inputs are driven using $V_{IH}$ and $V_{IL}$ values. The outputs are compared against $V_{OH}$ and $V_{OL}$ limits.

### DC Testing

After the functional testing, all DC parameters in the DC Characteristics are tested for each input and output on the automatic tester.

It is important to emphasize that the specified limits in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min).

Threshold measurement is the most difficult DC parameter test on the automatic tester. If all inputs are at threshold simultaneously, the device may tend to oscillate when in a test environment.

Make sure that each input and output is terminated through a 50Ω resistor to −2.0V.

Although suggested test conditions are described for $V_{OH}$, $V_{OHT}$, $V_{OL}$, and $V_{OLT}$, they are not necessarily worst case. The following is a recommendation as to what to look for in considering output voltages in the worst case.

$V_{OH}$ and $V_{OL}$ levels on ECL devices are somewhat current path dependent, i.e., the output voltage level can vary depending on how the output is being driven by the internal circuitry. Also, the effect is different for $V_{OH}$ than for $V_{OL}$. This can be explained by analyzing the circuit in Figure 1.

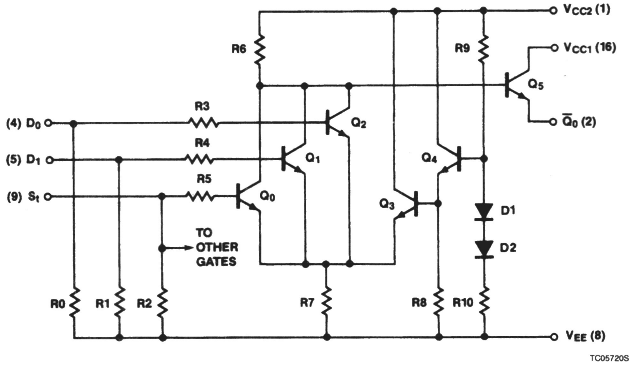

Figure 1

| | | |
|---|---|---|
| Power Supply | Current capability | Since ECL is noted for high current requirements, power supplies of $V_{EE}$ should be capable of supplying current with a 25% reserve over the highest powered part. The power supply must provide well over 1 Ampere. |
| Power Supply | Noise-free power supply current | Since the voltage swing on ECL input and output levels is only about 800mV, it is important that the power supplies be extremely clean and free of spikes, hum, or other types of noise. |
| Pulse Generator | DC resolution | Since the threshold measurements require that input voltage be extremely accurate and repeatable, the driver and the output comparator should have an accuracy of ± 1mV. |
| Pulse Generator | Edge rates | It is important that the rise and fall time of the clock pulses be fast, clean, and free from overshoot. |
| Sampling Scope | Rise time | The Sampling scope should be able to handle rise time of 100ps and preferably should have a digital display for easier readout. |
| Test Fixture | Contact resistance | Contact resistance between device pins and test pins should be kept to less than 50mΩ to avoid oscillation. Free length of contact (portion not matched to 50Ω terminating resistor) should be kept to less than 10mm. |
| Test Fixture | Input | All inputs must be terminated through a 50Ω resistor to ground or through a built-in 50Ω resistor of pulse generator. |
| Test Fixture | Output termination | To minimize reflection, all outputs must be terminated through a 50Ω resistor to Ground, or through a built-in 50Ω resistor of the sampling scope. |
| Test Fixture | Jig delay | Effort should be made to cut down propagation delay due to the fixture (jig) itself. |
| Test Fixture | Decoupling | To avoid oscillations, great care should be taken to decouple the $V_{CC1}$, $V_{CC2}$, $V_{CC3}$, and $V_{EE}$ to Ground. |
| Interconnection | | |

# Testing

Q0, Q1, and Q2 are the input transistors in this simplified schematic of a 10100. Q4, D1 and D2, and R9 and R10 form the voltage reference supply ($V_{BB}$). If the voltage at the base of any or all of the input transistors rises above $V_{BB}$, the transistor will begin to conduct current down through R6, thus diverting most of the base current away from the output transistor, Q5. The voltage at the output pin will drop toward $V_T$ via a 50Ω termination resistor, $R_T$.

If only one input transistor is conducting, all the current that is diverted away from Q5 will flow through it.

If two input transistors are conducting, that same amount of current will be split evenly by each transistor. Since the saturation resistance ($R_{sat}$) of any real transistor is not zero, a smaller voltage drop will result causing a slightly lower voltage at the output.

If all three input transistors are conducting, the current will be split three ways and a still lower voltage will result. Since the most negative output voltage is $V_{OLmin}$, the above condition would represent the worst case for that test. Therefore, if the most positive LOW state is $V_{OLmax}$, the worst-case condition for that would be with only one input transistor conducting. It is advisable then to test $V_{OLmax}$ with each input HIGH, one at a time.

In the case of $V_{OH}$, there is only one possibility — all inputs low — so it is not necessary (or possible) to test anything but that one condition.

It is fairly simple to see from the above example what the worst cases are for most gates (provided a schematic is available). As the circuitry advances into flip-flops and beyond into the even more advanced functions, the worst-case conditions become a little more difficult to determine, although the philosophy remains the same. The easiest way to determine how the output is affected is to start at the base of the output transistor to see what components directly drive it, then determine all of the possible combinations from all of the available inputs. Of course, only the worst possible combinations need to be tested.

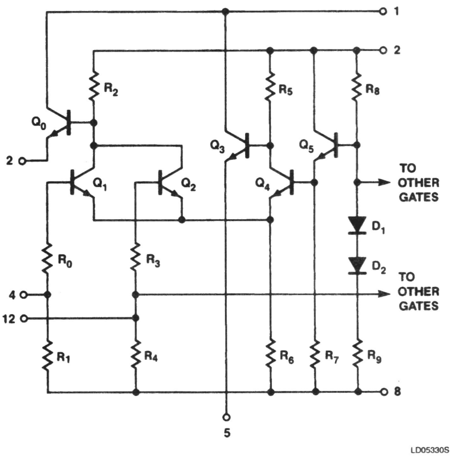

Figure 2

When testing inverting circuits, the parameter that is usually affected is $V_{OL}$; but in non-inverting circuits, $V_{OH}$ is path dependent. Referring to the simplified schematic of a 10101 in Figure 2, the inverting output is affected the same as in the previous example but this device also has a non-inverting output from the emitter of Q3. With both inputs HIGH, Q4 diverts most of the base current away from the base of Q3, thus the output is LOW and that is the only LOW state condition that can exist.

If one input goes HIGH, most of the current from R5 can now flow into the base of Q3 pulling the emitter HIGH. If the other input transistor goes high also, the voltage drop will be shared equally between Q1 and Q2 and the voltage at their emitters could rise a few more millivolts. In turn, the emitter of Q4 will rise along with the collector of Q4, the base of Q3 and therefore the output emitter. So the worst-case $V_{OHmax}$ test for this device would be with both inputs HIGH and the worst-case $V_{OHmin}$ would be with only one input HIGH at a time.

Every effort has been made to include simplified circuit schematics for all devices in the limited space of this databook to aid the in testing and circuit design with Signetics' ECL devices.

## AC Testing

It is important to emphasize that the specified limits in the AC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board.

Since few automatic testers have sufficient accuracy to perform sub-nanosecond testing, AC testing is one of the most difficult tests to accomplish. Depending on the accuracy and repeatability of the automatic tester, a manual bench-type tester may be required for correlation to complement the AC testing with the automatic tester.

Signetics

# Section 4
# ECL User's Guide

ECL Products

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# Chapter 1
# ECL Circuit Basics

## THE ECL GATE

Figure 1.1 shows a basic ECL 10K OR/NOR gate having two inputs and two complementary outputs. The gate's current switching stage is shown in Figure 1.2. The input voltage, $V_{IN}$, controls the current, I. When $V_{IN}$ changes logic levels, I is switched between $Q_2$ and $Q_5$. $V_{BB}$, the reference voltage, is held at a fixed voltage by an internal voltage driver, with the fixed voltage being midway between the input voltage threshold region. As the current is switched, the output voltages $V_{OUT1}$ and $V_{OUT2}$ also change, giving a NOR and an OR logical output, respectively.

The net output voltage swing is determined by $R_3$ and $R_6$ and the magnitude of I. I can be determined from:

$$I = \frac{\text{Max}(V_{IN},\ V_{BB}) - V_{BE} - V_{EE}}{R_7} \qquad \text{Eq. 1.1}$$

where $V_{BE}$ is the base-emitter voltage drop of $Q_2$ or $Q_5$, (on the order of 0.8V).

If $\text{Max}(V_{IN}) > \text{Max}(V_{BB})$, then

$$I = \frac{\text{Max}(V_{IN}) - V_{BE} - V_{EE}}{R_7} \qquad \text{Eq. 1.2}$$

If $\text{Max}(V_{IN}) < \text{Max}(V_{BB})$, then

$$I = \frac{\text{Max}(V_{BB}) - V_{BE} - V_{EE}}{R_7} \qquad \text{Eq. 1.3}$$

I is on the order of several milliamperes (4mA for a 10K gate).

Figure 1.3 gives the switching characteristics of the circuit in Figure 1.2, with the output voltage given as a function of the input voltage. Four operating zones are shown, labeled A, B, C, and D.

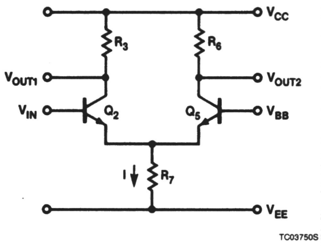
In Zone A, $V_{IN}$ is enough below $V_{BB}$ to turn $Q_2$ off. $V_1$ is

$$V_{CC} - (\text{I leakage } Q_2)(R_3)$$

The current, I, passes almost entirely through $R_6$ creating a voltage drop across $R_6$ of about 1V (the value of $R_6$ is selected specifically to achieve this). $V_{BB}$ is designed to be slightly lower than $V_{CC} - (I)(R_6)$ to avoid saturation of $Q_5$ while maintaining a collector-base voltage > 0. For this purpose, $V_{CC} - V_{BB}$ is selected to be on the order of 1.3V.

In Zone B, the transition region, the $V_{IN}$ is nearly $V_{BB}$. Both transistors, $Q_2$ and $Q_5$, are on and conducting current. In this region the switching stage behaves like a differential amplifier. $Q_2$ and $Q_5$ are designed to be as nearly identical as possible so that when $V_{IN} = V_{BB}$, the current, I, is divided equally between the two, making the voltage drop across both $R_3$ and $R_6$ approximately 0.5V. The width of this zone is approximately 100mV at 25°C. The width varies with temperature by $(4kT)/q$ (where k is the Boltzman constant, q is the charge of an electron, and T is the absolute temperature of the $V_{BE}$ junction) due to the temperature dependence of the emitter-base junctions of $Q_2$ and $Q_5$.

In Zone C, $V_{IN}$ is enough above $V_{BB}$ to turn off $Q_5$. As $V_{IN}$ rises, the emitter voltage, $V_E$, increases (since $V_E = V_{IN} - V_{BE}(Q_2)$ and $V_{BE}(Q_2)$ is approximately constant) while $V_{BB}$ remains constant until the base-emitter voltage drop of $Q_5$ is sufficient to keep $Q_5$ on. In this zone $V_2$ becomes equal to $V_{CC} - (\text{I leakage } Q_5)(R_6)$ and $V_1 = (R_3)(I)$. $R_3$ is designed to make $V_1$ close to $V_{CC} - 1V$. I varies in Zone C due to its dependence on $V_E$. Because of this, $R_7$ is replaced by a current source in many circuits to produce better matched output characteristics, as well as other advantages that will be discussed in a later section.



If $\text{Max}(V_{IN}) > \text{Max}(V_{BB})$, then

$$I = \frac{\text{Max}(V_{IN}) - V_{BE} - V_{EE}}{R_7}$$

If $\text{Max}(V_{IN}) < \text{Max}(V_{BB})$, then

$$I = \frac{\text{Max}(V_{BB}) - V_{BE} - V_{EE}}{R_7}$$

**Figure 1.2. ECL Current Switch**

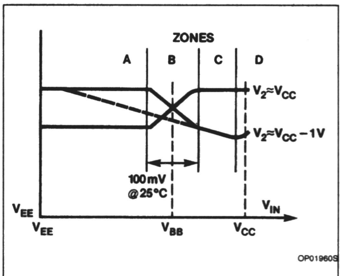


**Figure 1.3. Switching Characteristics of ECL Current Switch**

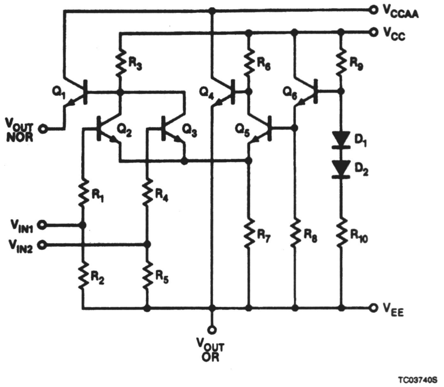


**Figure 1.1. Basic 10K ECL OR/NOR Gate**

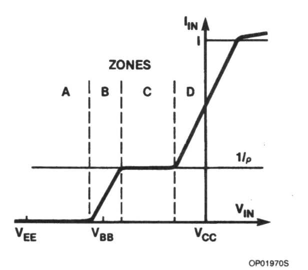


**Figure 1.4. Change in Base Current as a Function of $V_{IN}$**

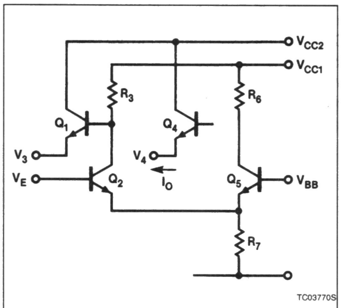


**Figure 1.5. Emitter-Follower Outputs**

In Zone D, $V_E$ is high enough to allow $Q_2$ to saturate. Under this circumstance, the base-collector junction of $Q_2$ is forward-biased and the collector voltage begins to follow the input voltage, creating the upturn in the characteristic curve for $V_1$ in Figure 1.3. Because the current I can no longer be provided completely by the collector of the transistor, the difference is supplied by the base current of $Q_2$, which increases considerably. The change in base current with increased input voltage is shown in Figure 1.4. This current is the input current of the simplified gate. The input voltage of an ECL gate is usually limited to prevent operation in Zone D.

## EMITTER-FOLLOWER BUFFERS — OUTPUT AND TRANSFER CHARACTERISTICS

The $V_1$ and $V_2$ signals of Figure 1.2 could be used directly as the output signals of the gate. However, there are two disadvantages in doing so. First, the voltage values of the logic levels generated by these nodes are not compatible with an input threshold voltage equal to $V_{BB}$, so a downward shift of $V_1$ and $V_2$ is required. Second, $V_1$ and $V_2$ would have a high impedance for values of I in the several milliampere range. The addition of transistors $Q_1$ and $Q_4$, shown in Figure 1.5, eliminates both of these problems. The output voltage level is shifted down by $V_{BE}(on)$. And, because these transistors are configured as emitter-followers, they provide a low output impedance allowing the circuit to drive transmission lines with characteristic impedances of 50Ω or greater.

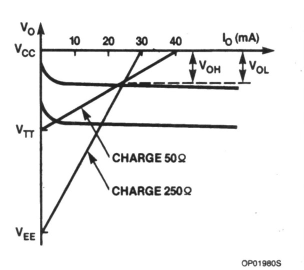


**Figure 1.6. $V_O$ as a Function of $I_O$**

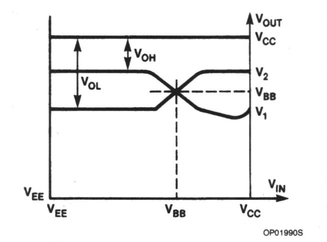


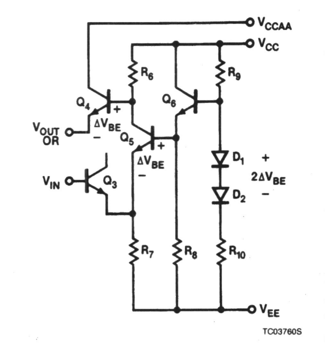
**Figure 1.7. $V_{OUT}$ as a Function of $V_E$ (50Ω Load)**

Figure 1.6 shows the output characteristic, $V_O$ ( $= V_3$ or $V_4$), as a function of the output current, $I_O$, for Zone A or Zone C. Two load lines are shown: 50Ω and 250Ω. The 50Ω load is connected to an intermediate voltage, $V_{TT}$, to limit the output current of the gate. Larger loads can be connected directly to $V_{EE}$.

Figure 1.7 gives the transfer characteristic, $V_O$ ( $= V_3$ or $V_4$) as a function of $V_E$. Note that the logic swing is now almost symmetrical about the reference voltage, $V_{BB}$, due to the voltage-level shifting by the $V_{BE}$ of the emitter-follower transistors, $Q_1$ and $Q_4$.

## INTERNAL THRESHOLD VOLTAGE GENERATOR

In 10K ECL circuits, the threshold voltage, $V_{BB}$, is provided by the internal voltage generator shown in Figure 1.8. (The NOR output circuitry has been excluded for simplicity.) As with other device technologies, the transfer and other characteristics of ECL gates are temperature-dependent. This is mainly due to the temperature dependence of $V_{BE}$.



$(R_{10})(I) = (R_7)(I)$
$(R_9)(I) = \frac{1}{2}(R_6)(I)$

**Figure 1.8. Internal Voltage Generator — 10K ECL**

As stated earlier, the logic HIGH and logic LOW noise margins of ECL gates should be symmetrical about $V_{EE}$. Due to the temperature dependence of $V_{BE}$, this is possible at only a single temperature when the reference voltage, $V_{BB}$, is kept fixed. However, it is possible to maintain the symmetry of the noise margins over a wide temperature range if the reference voltage itself is made to be temperature-dependent. The voltage generator of Figure 1.8 accomplishes this. The reference voltage for the current switch is taken from an emitter-follower, $Q_6$. $D_1$ and $D_2$ help to stabilize the current in the emitters of $Q_3$ and $Q_5$ against variations in temperature in that any change with temperature of the $V_{BE}$ of $Q_6$ and $Q_5$ is compensated by a similar change across $D_1$ and $D_2$.

Assume a temperature change, ΔT. This temperature change will produce a voltage change in each forward-biased $V_{BE}$ junction, the amount of voltage change being $\Delta V_{BE} = -k\Delta T$, where $k = 2mV/°C$. Assuming the gain through $Q_6$ is unity, the change in the reference voltage, $V_{BB}$, due to ΔT is given by

Eq. 1.4

$$\Delta V_{BB} = \frac{2\Delta V_{BE} R_9}{R_9 + R_{10}} - \Delta V_{BE}$$

$$= \Delta V_{BE}\left[\frac{2}{\left(1 + \frac{R_{10}}{R_9}\right)} - 1\right]$$

# User's Guide

When $Q_5$ conducts, $V_{OUT}$ is at logic level $\theta$. The change in $V_{OUT}$ due to $\Delta T$ is given by Eq. 1.5

$$\Delta V_{OUT}(\theta) = -\Delta V_{BB}\left(\frac{R_6}{R_7}\right) + \Delta V_{BE}\left(\frac{R_6}{R_7}\right) - \Delta V_{BE}$$
$$= \left(\frac{R_6}{R_7}\right)\left(-\Delta V_{BB} + \Delta V_{BE}\right) - \Delta V_{BE}$$

Note that in the equations for $\Delta V_{BB}$ and $\Delta V_{OUT}$ only resistor ratios appear. This result is important because it is possible to hold resistor ratios to a much tighter tolerance than absolute values of resistors during device fabrication.

When $Q_5$ is off and $V_{OUT}$ is at logic level 1,

$$\Delta V_{OUT}(1) = -\Delta V_{BE} \qquad \text{Eq. 1.6}$$

Resistor values are chosen so that the "average" $\Delta V_{BE}$ of the two logic levels will equal $\Delta V_{BB}$. Therefore, if the $V_{BE}$ of $Q_4$ and $Q_6$ are equal, then $V_{BB}$ will remain centered between $V_{OH}$ and $V_{OL}$.

## SELECTION OF $V_{CC}$ AS REFERENCE VOLTAGE (GROUND)

Unlike TTL gates, with ECL gates it is common practice to ground the positive end of the voltage supply. One advantage of using this arrangement with ECL gates is that it minimizes external noise transfer.

Figure 1.9 shows our ECL gate with the NOR output omitted for simplification. Usually the output voltage of the gate is the voltage between the emitter of $Q_4$ and $V_{CC}$ ($V_{OUT}$), but we could just as easily consider the output voltage to be that between the emitter of $Q_4$ and $V_{EE}$ ($V'_{OUT}$). As far as the output signal is concerned, the positive and negative sides of the supply are the same electrical point. As Figure 1.9 shows, closed-circuit loops are formed by the connection to $V_{CC}$. A varying magnetic flux can be produced in these loops by the currents in the gate, or by currents in neighboring gates, which produces an electromagnetic field in the loops and in $V_{CC}$. This electromagnetic field, or induced voltage, is referred to as "noise" because it is random and unpredictable. It is represented in Figure 1.10 by the voltage source $V_N$.

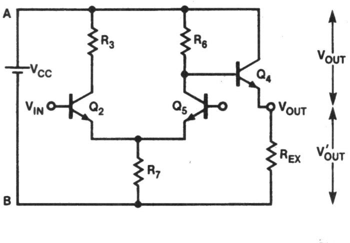


**Figure 1.9. ECL Gate With NOR Output Omitted**

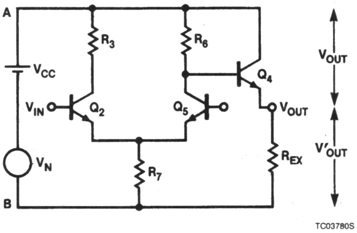


**Figure 1.10. ECL Gate (NOR Output Omitted) With "Noise" Generator, $V_N$**

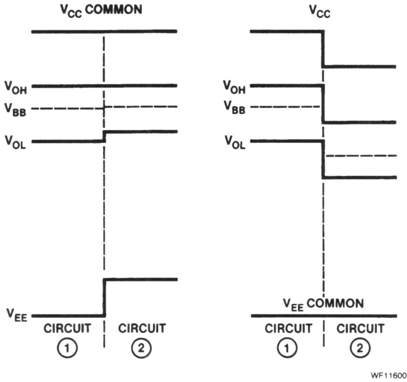


**Figure 1.11. Difference in Output Voltage of ECL Gate When Powered by $V_{CC}$ vs. Powered by $V_{EE}$**

With the inclusion of $V_N$, the two sides of the power supply, A and B, are no longer equivalent and $V_{OUT}$ and $V'_{OUT}$ are also no longer equivalent. Assume $Q_5$ is cut off. Then $V_N$ can be considered across $R_6$, $Q_4$ and $R_{EX}$ only. The impedance between the collector and emitter of $Q_4$ is

$$Z_{CE} = \frac{R_6}{(h_{FE} + 1)} \qquad \text{Eq. 1.7}$$

For $h_{FE} = 99$ and $R_6 = 300\Omega$, $Z_{CE} = 3\Omega$. Then, $V_{OUT} = (3/1{,}500)V_N = 0.002V_N$ while $V'_{OUT} = (1{,}500/1{,}503)V_N \cong V_N$. The advantage lies clearly with using $V_{OUT}$ rather than $V'_{OUT}$.

It is also common practice to have the output terminal of a signal source and the input terminal of a signal measuring device use ground as one signal terminal. This practice is convenient since ground is usually the chassis on the relay rack on which the circuit is built, including the cabinet that houses the unit, if any, and has the advantage that when units are interconnected, the chassis, cabinets, etc., are all joined electrically.

Thus, since it is advantageous to use the positive side of $V_{CC}$ as one of the output terminals, and also advantageous to use ground as one such terminal, the positive side of $V_{CC}$ is grounded.

Another advantage to the grounding arrangement employed with ECL is shown in Figure

1.11 where the output voltages of two gates, one powered by $V_{CC}$ and one powered by $V_{EE}$, is shown. When $V_{CC}$ is common to both gates, $V_{OH}$ varies very little and the $V_{OL}$ of each gate remains compatible with the threshold voltage, $V_{BB}$, of the other. However, when $V_{EE}$ is common to both gates, the output voltages $V_{OH}$ and $V_{OL}$ of both gates can become so different that the threshold of the second gate is no longer compatible with the output voltage of the first gate.

## ECL LOGIC IMPLEMENTATION

An ECL gate incorporating the basic structure of Figure 1.1 is shown in Figure 1.12. The input transistors $Q_2$ and $Q_3$ are shown here in parallel. Additional transistors can be added in parallel to provide for multiple gate inputs.

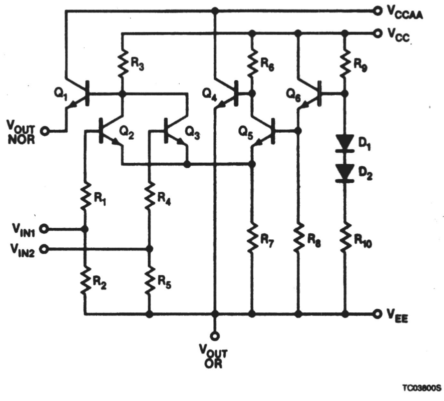
When the input voltages $V_{IN1}$ and $V_{IN2}$ are in the LOW state (i.e. $< V_{BB}$), the input transistors $Q_2$ and $Q_3$ are cut off and $Q_5$ is conducting. This creates a LOW level at the $V_{OUT2}$ output and a HIGH level at the $V_{OUT1}$ output. If either of the input voltages goes to the HIGH state (i.e. $> V_{BB}$), the current will switch to the corresponding input transistor and cut $Q_5$ off. Consequently, the $V_{OUT2}$ output will go to HIGH and the $V_{OUT1}$ output will go LOW. Thus, the circuit performs an OR function

$$V_{O4} = A + B \qquad \text{Eq. 1.8}$$

at the $V_{OUT2}$ output and performs a NOR function

$$V_{O1} = \overline{A + B} \qquad \text{Eq. 1.9}$$

at the $V_{OUT1}$ output.



| $V_{IN1}$ | $V_{IN2}$ | $V_{OUT1}$ |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

| $V_{IN1}$ | $V_{IN2}$ | $V_{OUT2}$ |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

**Figure 1.12. ECL Logic Implementation**

# Chapter 2
# Logic Function Operation

## SERIES GATING

The switching stage described in the previous section behaves like an inverting relay contact and, as with relays where contacts can be cascaded, ECL differential stages can also be cascaded. An example is shown in Figure 2.1. Input transistors A and B have been placed in series to share a common current source, $Q_{10}$, and implement an AND function. It is important to avoid saturating the lower transistors so that the complete benefits of non-saturating logic can be maintained. This can be accomplished by shifting the thresholds of the two differential stages by a voltage comparable to the logic swing on input A. Therefore, a second reference voltage, $V_{B2}$, is added to shift from 1V to 1.6V with respect to $V_{B1}$. An equal shift is implemented for input A by the emitter-follower, $Q_{12}$, shown in Figure 2.2.

This logic block, called "series gating," adds the NAND and AND logic functions to the OR and NOR capability of the basic ECL gate. This technique is so powerful, consumes so little power, and requires so few components that it has become the standard building block for complex circuits in ECL families having two or three levels of current-switching. (The voltage of the 10K family was set at -5.2V to allow three levels of current-switching — two voltage shifts. For a simple gate with only one level of current switching, 2.6V to 3V would certainly have been sufficient.)

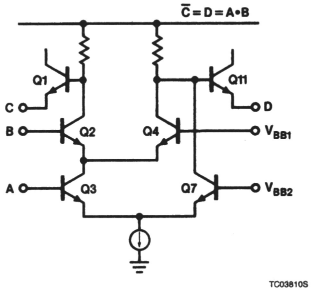


Figure 2.1. ECL AND Gate

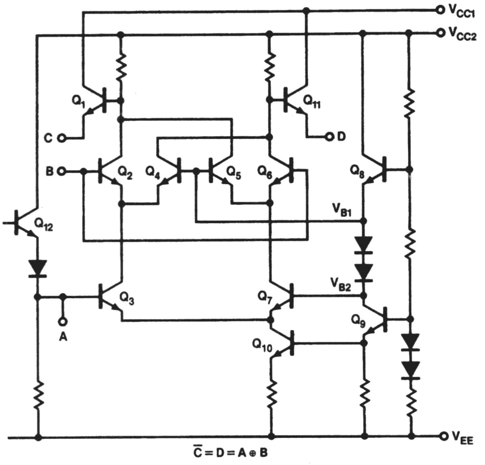


Figure 2.2. Series Gating With ECL

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## FLIP-FLOPS

Flip-flop functions make extensive use of series gating. Figure 2.3 shows a simple flip-flop that, under the control of a clock signal, latches a "data" bit. When the clock is in the LOW state, current from the source transistor, $Q_9$, is switched by $Q_{12}$ to the differential "data" stage formed by $Q_5$ and $Q_{13}$, and from there to the outputs $V_{OUT}$ and $\overline{V_{OUT}}$. During the transition, this current controls the logic state of the "internal outputs," $Q_8$ and $Q_{10}$, which reproduce the state of the data input. When the clock goes HIGH, the current is switched by $Q_7$ to the differential pair formed by $Q_6$ and $Q_{11}$, which is itself controlled by the internal outputs. The circuit is then latched on the data state that preceded the rise in the clock signal, regardless of the subsequent state of the data input.

In this latched state, the data in the flip-flop can be changed by applying a LOW logic state to transistor $Q_4$ or $Q_{14}$, which then forces the output HIGH or LOW, thereby accomplishing a "set-reset" function.

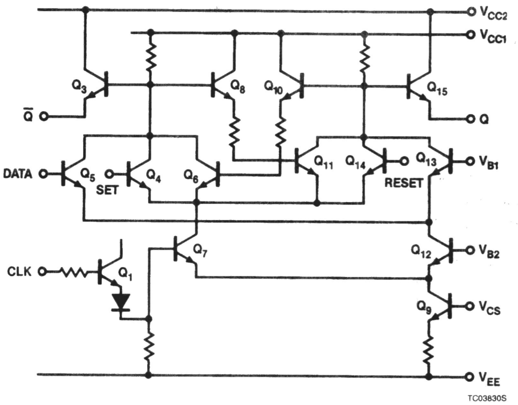

$V_{CC2}$
$V_{CC1}$
$Q_3$
$Q_8$
$Q_{10}$
$Q_{15}$
$\overline{Q}$
Q
DATA
$Q_5$
SET
$Q_4$
$Q_6$
$Q_{11}$
$Q_{14}$
$Q_{13}$
RESET
$V_{B1}$
$Q_7$
$Q_{12}$
$V_{B2}$
CLK
$Q_1$
$Q_9$
$V_{CS}$
$V_{EE}$
TC03830S

Figure 2.3. Basic D-Type Latch

## WIRED-OR FUNCTIONS

Figure 2.4 shows another technique for implementing complex ECL functions: the ability to control several output emitter-followers with the same gate. This makes it very easy to generate supplementary signals.

In Figure 2.4, four independent logic functions are implemented via only two differential stages by combining outputs. Note that for the internal outputs, which need only drive internal inputs having relatively high impedance rather than $50\Omega$ lines, fairly large internal resistors ($R_T$ = 1k to 5k$\Omega$) can be used for $V_{EE}$ connections.

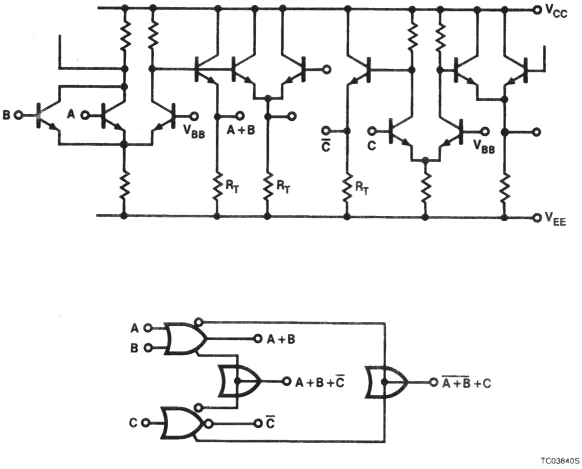

$V_{CC}$
B
A
$V_{BB}$
A+B
$\overline{C}$
C
$V_{BB}$
$R_T$
$R_T$
$R_T$
$V_{EE}$
A
B
A+B
A+B+$\overline{C}$
$\overline{A+B}$+C
C
$\overline{C}$
TC03840S

Figure 2.4. Wired-OR Implementation

# Chapter 3
# ECL Gate — Static Characteristics

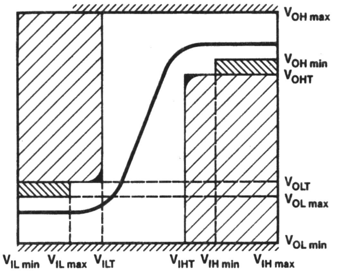
## OUTPUT CHARACTERISTICS

Figure 3.1 shows transfer curve and DC specification test points for a 10K ECL OR gate. Note the two sets of min/max logic level parameters. The first set, $V_{ILmin}/V_{IHmax}$, should cause the output to take a level somewhere within the $V_{OLmax}/V_{OLmin}$ and $V_{OHmax}/V_{OHmin}$ specification. The second set of logic level parameters relates to the switching thresholds. When a voltage $V_{ILT}$ is applied to the input, the OR output should be below the $V_{OLT}$ level; and, when a voltage $V_{IHT}$ is applied to the input, the output should be above the $V_{OHT}$ level.

Since variations in wafer fabrication process parameters can affect a gate's transfer characteristics, device performance is tested at the indicated test points to ensure that:

1. the switching threshold falls within the rectangle defined at the lower left by the $V_{ILT}/V_{OLT}$ corner point and at the upper right by the $V_{IHT}/V_{OHT}$ corner point; i.e. that switching does not begin outside this rectangle;
2. quiescent logic levels fall within the specified min/max ranges.

In 10K ECL, this curve varies with temperature and supply voltage changes. This is explained in detail in a later section.



OP02000S

**Figure 3.1. ECL OR Gate Transfer Curve With DC Specification Test Points**

## NOISE MARGIN

Noise margin is a measure of a circuit's immunity to adverse DC operating conditions. Noise margin is defined for the HIGH state as

$$V_{NH} = V_{OHT} - V_{IHT} \quad \text{Eq. 3.1}$$

and for the LOW state as

$$V_{NL} = V_{ILT} - V_{OLT} \quad \text{Eq. 3.2}$$

Where "T" is used to denote the threshold value for $V_{OH}$, $V_{OL}$, $V_{IH}$ and $V_{IL}$. Figure 3.2a gives noise margins vs. temperature variations for 10K ECL and 3.2b gives noise margins vs. power supply variations for 10K ECL.

"Noise immunity" measures the minimum input noise that will propagate through cascaded gates. This measurement, indicative of a device's immunity to noise during actual AC system operation, is difficult to measure and, therefore, is not specified on datasheets. However, noise immunity of 10K devices is typically at least 40mV greater than the DC noise margin.

Both 10K and 100K ECL device specifications dictate that only one input at a time should be connected to a threshold level ($V_{IHT}$ or $V_{ILT}$) and that all other inputs should be at $V_{IHmax}$ or $V_{ILmin}$ during testing.

| PARAMETER | | -30°C | +25°C | +85°C |
|---|---|---|---|---|
| $V_{IHmin}$ to $V_{OHCmin}$ | $V_{NH}$ (mV) | 125 | 125 | 125 |
| $V_{ILmax}$ to $V_{OLCmax}$ | $V_{NL}$ (mV) | 155 | 155 | 155 |

**a. 10K to 10K**
**Minimum Noise Margin vs. Temperature Variations**

| PARAMETER | | $V_{EE}$ -10% | $V_{EE}$ -5% | $V_{EE}$ +5% |
|---|---|---|---|---|
| $V_{IHmin}$ to $V_{OHmin}$ | $V_{NH}$ (mV) | 127 | 166 | 241 |
| $V_{ILmax}$ to $V_{OLmax}$ | $V_{NL}$ (mV) | 223 | 249 | 301 |

**b. 10K to 10K**
**Minimum Noise Margin vs. $V_{EE}$ Variations**

**Figure 3.2. 10K ECL Minimum Noise Margins**

## INPUT CHARACTERISTICS

As shown in Figure 1.1, gate inputs are not connected directly to the base of their input transistors, but instead are connected through a network of two resistors, $R_1$ and $R_2$ (or $R_4$ and $R_5$). The resistor $R_1$ ($R_4$) guarantees a positive (real) input impedance at all frequencies. High frequency capacitive effects could cause the input current to be put out of phase by more than 90° with regard to the input voltage, causing the appearance of a negative resistance on the base of $Q_2$, if $R_1$ ($R_4$) was not included. The resistor $R_2$ ($R_5$) pulls any unused inputs LOW, eliminating the need for external wiring on these inputs. However, because of large switching transients associated with fast rise and fall times and the sensitivity of clocked devices (flip-flops, counters, etc.), it is advisable to use external components with clocked devices to assure that the unused inputs of such devices are securely tied to a low logic level.

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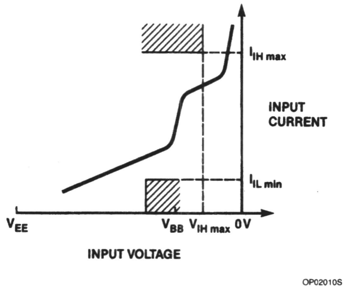
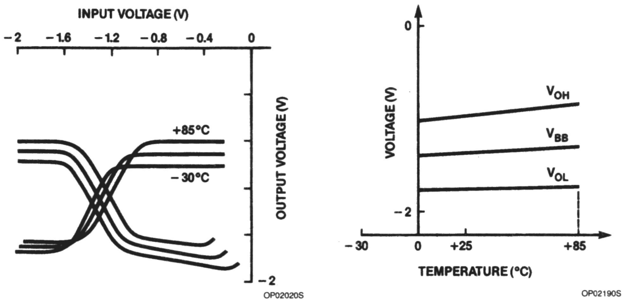


Figure 3.3. ECL Gate Input Characteristics



a. b.

Figure 3.4. Effect of Temperature on Output Voltage

Figure 3.3 shows the input characteristics of an ECL gate. $I_{IHmax}$ is the guaranteed maximum static load that is represented by the gate input. $I_{ILmin}$ guarantees the internal pull-down resistance.

## CURRENT CONSUMPTION

Current consumption is specified as the Power Supply Drain Current, $I_{EE}$, and is the current that is drawn through the supply pin, $V_{EE}$. $I_{EEmax}$ is measured with $V_{CC}$ at 0V and $V_{EE}$ at −5.2V since maximum circuit speed is achieved at this power supply value.

The magnitude of $I_{EE}$ is affected by three separate portions of the ECL gate: the current switch, the reference voltage supply, and the output emitter-followers. $I_{EE}$ limits specified for a particular device reflect the power requirements of the current switch (or switches) and reference voltage supply. However, ECL devices can support a broad range of output termination resistor values, with the particular value chosen depending on individual system performance requirements. Therefore, it is necessary to add power requirements due to input current drain and output loading to the specified power supply drain current limit given in the device's datasheet.

## EFFECT OF TEMPERATURE

10K ECL outputs rise with increasing temperature. This is mainly due to the dependence of $V_{BE}$ on temperature.

Figure 3.4 shows output voltage as a function of temperature. Because of this temperature dependence, DC parameters are generally specified at three ambient temperatures: −30°C, +25°C, and +85°C.

When designing with ECL devices, the following should be kept in mind:

1. Maximum noise immunity is obtained when two connected circuits are at the same temperature;
2. When a circuit is tested, thermal equilibrium must be obtained before any measurements are made.

## EFFECT OF SUPPLY VOLTAGE ON 10K ECL

As explained in Chapter 1, 10K ECL devices are specified with $V_{CC}$ at ground and $V_{EE}$ at −5.2V because maximum noise immunity is achieved with this supply configuration. This convention is not mandatory; and, while not recommended because of loss of noise immunity, it is possible to operate ECL devices from a TTL +5V power supply.

10K ECL devices are specified for $V_{EE} = -5.2 \pm 10\%$. However, the best circuit speed is achieved with $V_{EE} = -5.2V$. As $V_{EE}$ becomes more negative, both noise margin and power dissipation increases. As $V_{EE}$ becomes more positive, power dissipation decreases, but at the expense of a decrease in noise margin.

Most 10K ECL devices have two power supply pins, $V_{CC1}$ and $V_{CC2}$, to reduce cross-coupling between internal device components when the outputs are driving heavy loads. $V_{CC1}$ supplies current to the output transistors and $V_{CC2}$ supplies current to the circuit logic transistors.

# Chapter 4
# ECL Gate — Dynamic Characteristics

## TRANSITION TIME AND PROPAGATION DELAY

The dynamic characteristics of a device are those that define its effect on a specified input signal as that signal travels through the device. They include the time required to change the output from one logic state to another, specified as the output transition time, and the time required for the output of the device to respond to an input signal, specified as the propagation delay.

To accurately measure a device's dynamic performance, an environment very similar to the system environment in which the device will be used should be created. Input voltages applied should represent signals the device will see in the system; i.e., pulses having HIGH and LOW levels that are typical of $V_{OH}$ and $V_{OL}$ and having edges that are representative of the edges generated by the outputs of an interfacing device. An example is shown in Figure 4.1.

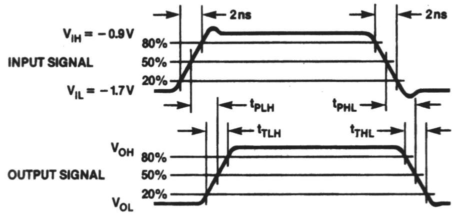


**Figure 4.1. Waveforms for Dynamic Characteristic Measurements**

The output transition time ($t_{TLH}$ and $t_{THL}$) also gives an indication of the maximum operating frequency and of any high-frequency parasitic effects. For ECL devices, both $t_{TLH}$ and $t_{THL}$ are measured between 20% and 80% of the signal amplitude; i.e., in the transition region. Because ECL utilizes current-mode switching to eliminate transistor saturation storage delays and permits the use of differential comparison techniques, transition rise times can, by design, be slowed via internal time constants without sacrificing throughput delays. This is an important advantage of ECL because slower rise times minimize ringing and reflections and, therefore, simplify board design. The typical edge rate for 100K ECL is 1V/ns, 80% of the Schottky TTL edge rate.

Propagation delay ($t_{PD}$) defines the time it takes for a signal to travel internally from the input terminal and the output terminal of a device. Test equipment limitations make it necessary to measure the propagation time of ECL devices at 50% of the amplitude of both signals rather than at $V_{BB}$.

## INTERNAL SWITCHING

Internal switching of the gate takes place in two stages (see Figure 1.10):

1. In the first stage, the input voltage rises to $V_{IH}$. The voltage change at the input of transistor $Q_2$ is delayed, however, because of its input capacitance. When its input voltage enters Zone B in Figure 1.3, $Q_2$ begins to conduct after a given time delay dependent on its cut-off frequency, $f_T$.
2. In the second stage $Q_2$ delivers current into resistor $R_3$. The collector voltage, followed by the output voltage, begins to change. The rate of change of the output voltage depends on the total capacitance on the collector of $Q_2$, and varies inversely with the load resistance of the emitter of $Q_1$.

The transition time is dependent on the second stage, whereas the propagation delay depends on both stages.

## EFFECT OF CAPACITIVE LOAD

The speed of an ECL gate is adversely affected by capacitive loading due to the emitter-followers used at the outputs. When the base voltage of an emitter-follower increases, the emitter follows. Any capacitance across the output charges rapidly through the low output impedance of the emitter-follower. But, when the base voltage decreases, the emitter voltage remains fixed momentarily due to the coupled capacitor. Since the base voltage has dropped, the emitter-follower cuts off and any capacitance must discharge through a relatively large emitter resistance. The voltage difference between logic levels is small in comparison to the difference between the supply voltage and the logic level voltages, however, so the discharge time will not be excessively large with moderate capacitive loads.

As with all extremely fast logic gates, the upper limit on fanout of an ECL gate is not due to the DC loading factor, but rather due to the total capacitive load that a gate can drive in a given time.

## SETUP AND HOLD TIMES

Two additional dynamic characteristics are often important: the setup time ($t_S$) and the hold time ($t_H$). The setup time is the time interval between the active transition of a timing pulse or control input during which the data must be maintained at the input to insure its accurate recognition. A minimum value is specified that is the shortest interval for which correct operation of the device is guaranteed. The setup time can sometimes be a negative value, in which case the minimum limit defines the longest interval between the active transition and the application of the other input signal for which correct operation of the device is guaranteed.

The hold time is the interval during which the data must be retained at a specified input terminal after an active transition of a timing pulse or control input. A minimum value is specified that is the shortest interval for which correct operation of the device is guaranteed. Again, the hold time may have a negative value. In this case the minimum limit then defines the longest interval between the release of data and the active transition for which correct operation of the device is guaranteed.

# Chapter 5
# 100K ECL

## ECL Products

### ADVANTAGES OF 100K ECL

The 100K family provides a 0.75ns typical internal gate delay, higher on-chip integration, and improved immunity to voltage and temperature variations. Subnanosecond speeds are achieved via an oxide lateral isolation process that allows very small transistors with reduced parasitic capacitance (less than 0.2pF) and very high switching speed ($f_T$ = 5GHz). An increased current through the output gates also contributes to faster speed.

A new, smaller flat package with improved propagation and high-frequency characteristics has been developed to support the increased performance offered by the 100K family.

100K ECL devices have better immunity to temperature variations than do 10KH devices. While both 100K and 10KH have internal bias voltage generators that compensate internal thresholds for variations in supply and temperature, only 100K devices offer temperature compensation at device outputs.

### THE BASIC 100K GATE

Figure 5.1 shows a standard 100K gate. Note that the 100K gate is similar to a 10K gate, the essential differences occuring in the voltage and temperature compensation networks.

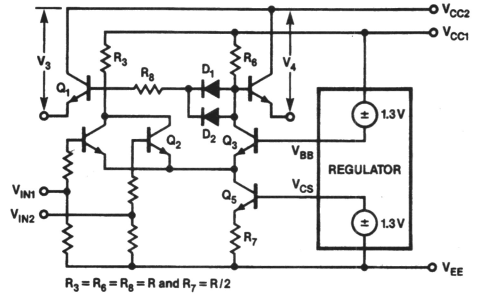
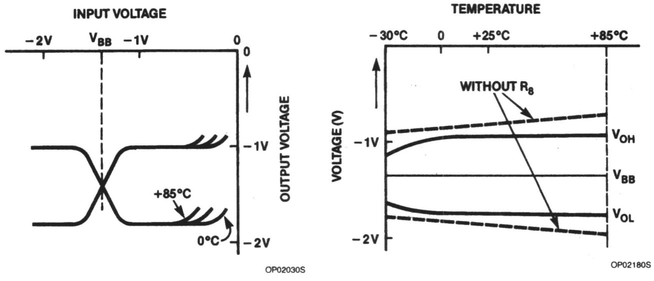


Figure 5.1. Standard Signetics 100K ECL Gate



a.

b.

Figure 5.2. Effect of Temperature on 100K ECL Gate With and Without Compensation

### TEMPERATURE COMPENSATION OF A 100K GATE OUTPUT

Additional temperature compensation at the gate outputs is achieved by adding a current-controlling network ($R_8$, $D_1$, $D_2$) between the collectors of $Q_2$ and $Q_3$ and by a regulator that generates a constant 1.3V control voltage for the current source, $V_{CS}$, regardless of variations in $V_{EE}$ or temperature. $R_7$ and the $V_{BE}$ of $Q_5$ (Figure 5.1) are designed so that when current, I, is passing through the gate, $(R_7)$ (I) + $V_{BE}$ $Q_5$ will be equal to 1.3V. When $V_{IN} = V_{BB} = -1.3V$, current is divided equally between the differential pair formed by $Q_2$ and $Q_3$, $R_8$ is cut off, and the two output voltages are equal: $V_3 = V_4 = (R_3\ (I/2) + V_{BE}\ Q_1$. By design $V_{BE}\ Q_1 = V_{BE}\ Q_5$, $R_7 = R_3/3$, and $V_3 = V_4 = V_{CS} = -1.3V$. The switching threshold (central crossover point in the transfer characteristic) is, therefore, stabilized at $V_{IN} = V_{OUT}$ = 1.3V, regardless of supply voltage and temperature.

The $V_{BE}$ of $Q_5$ decreases with increasing temperature; therefore, for a constant $V_{CS}$, the current in $R_7$ increases with increasing temperature. The network ($R_8$, $D_1$, $D_2$) keeps this increase in current stable during variations in the output levels when the gate is fully switched. It also absorbs an increasingly large portion of the current as temperature increases.

Figure 5.2, shows the behavior of the output voltage levels when the stabilization network is not functioning. Below 0°C, practically no current remains in $R_8$ and the stabilization network ceases to function. Devices can still be utilized below this temperature, but with reduced noise immunity; therefore, 100K ECL device characteristics are not specified below 0°C.

## THRESHOLD REGULATOR

The threshold regulator used in 100K ECL devices is shown in Figure 5.3. $V_{BB}$ is regulated to hold the input voltage threshold constant with temperature. $V_{CS}$ is regulated to hold internal thresholds constant over temperature to help keep the output voltage constant.

Since

$$I_{R9} = \frac{(V_{CS} - V_{BE}\ Q_9)}{R_9} \qquad \text{Eq. 5.1}$$

and

$$I_{R11} = \frac{(V_5 - V_{BE}\ Q_{11})}{R_{11}} \qquad \text{Eq. 5.2}$$

the current density, $J_9$, through $Q_9$ is determined by $R_9$ and $(V_{CS} - V_{BE}\,Q_9)$ and the current density, $J_{10}$, through $Q_{10}$ is determined by $R_{11}$ and $(V_{BE}\,Q_5 - V_{BE}\,Q_{11})$. Also, since $V_{CS}$ and $V_5$ are connected to $V_6$ by $V_{BE}\,Q_7$ and $V_{BE}\,Q_8$, $V_{CS}$ and $V_5$ are almost equal. Therefore, the ratio between $J_9$ and $J_{10}$ is fixed by the ratio between $R_{11}$ and $R_9$.

Due to the physics of semiconductor junctions, $(V_{BE}\,Q_9 - V_{BE}\,Q_{10})$ is proportional to the temperature, resulting in a high positive temperature tracking coefficient across $R_{10}$. The current through $R_{10}$ is the same as that through $R_{11}$ and $R_{13}$; therefore, they also have a high positive temperature tracking coefficient. $R_{11}$ and $R_{13}$ are designed so that the positive temperature coefficient across them exactly cancels the negative diode tracking coefficient of $V_{BE}\,Q_{11}$ and $V_{BE}\,Q_6$. Thus, the voltages $V_5$ and $V_{BB}$ are temperature-independent.

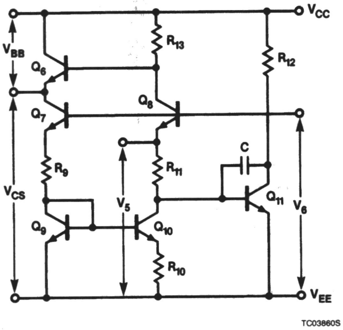


**Figure 5.3. 100K ECL Threshold Regulator**

$Q_{11}$ is a shunt regulator, with $Q_8$ and $R_{11}$ in negative feedback between its collector and base. In the absence of current from $Q_{10}$, $Q_{11}$ sets $V_5$ at 1 $V_{BE}$ and $V_6$ at 2 $V_{BE}$, independent of $V_{CC}$ and any current through $R_{12}$. Additional current from $Q_{10}$ compensates the negative temperature coefficient of $Q_{11}$, and makes it possible to maintain $V_5$ independent of variations in supply voltage and temperature.

The capacitor, C, stabilizes the feedback loop, $Q_{11} - Q_8 - R_{11}$, and prevents oscillations in the regulator when fluctuations occur in current or supply voltage.

This regulator is designed to function across a $V_{EE}$ range of −4.2V to −5.7V.

Figure 5.4 compares the effects of temperature and supply variations on the various ECL logic families.

| PARAMETER | 10K | 10KH | 100K |
|---|---|---|---|
| $t_{PD}$ Variation vs. Temp (ps/°C) | 7.0 | 4.0 | 0.2 |
| $t_{PD}$ Variation vs. Supply (ps/V) | 80 | 0 | 0 |
| $\Delta V_{OH}/\Delta T$ (mV/°C) | 1.50 | 1.50 | 0.06 |
| $\Delta V_{OL}/\Delta T$ (mV/°C) | 0.75 | 0.60 | 0.10 |
| $\Delta V_{BB}/\Delta T$ (mV/°C) | 1.20 | 1.20 | 0.08 |
| $\Delta V_{OH}/\Delta V_{EE}$ (mV/V) | 30 | 20 | 0 |
| $\Delta V_{OL}/\Delta V_{EE}$ (mV/V) | 320 | 50 | 0 |
| $\Delta V_{BB}/\Delta V_{EE}$ (mV/V) | 190 | 25 | 0 |

**Figure 5.4. Effects of Temperature and Supply Variations; DC Tracking Rates for 10K, 10KH and 100K Circuits**

# Chapter 6
# Transmission Lines

## LIMITATIONS OF THE REAL WORLD

Logic functions implemented in the real world must take into account that interconnection wires do not transmit a perfect replica of a theoretical signal, but instead add signal reflections and noise that can cause a system to malfunction. The degree to which noise and reflections will affect a system depends on the speed of the signal being transmitted and the distance the signal has to travel.

The maximum duration of noise or reflections that can be produced on a piece of wire is related to its length, varying between 3 to 4ns/ft of length, depending on the type of insulation used. Therefore, a flip-flop with a minimum setup time of 10ns can be used with interconnections of up to $^{10}\!/_4 = 2.4$ ft. long without much worry while a flip-flop with a minimum setup time of 2ns may experience problems with wires greater than $^{2}\!/_4 = {}^{1}\!/_2$ ft. long.

Simple transmission line concepts allow waveform reflections to be predicted with great accuracy and provides an easy way to look at high-speed system wiring.

## SIGNAL TRANSMISSION

Figure 6.1 shows a fixed voltage source, V, connected to a load, R, through a switch and a pair of wires of length x. When the switch is closed, the voltage does not immediately appear across the load. Instead, the voltage propagates from source to load with a finite velocity. Assuming the lines connecting the source to the load have a uniform cross section, the propagation velocity is given by

$$5v = \frac{1}{\sqrt{\left(\frac{dL}{dx}\right)\left(\frac{dC}{dx}\right)}} \qquad \text{Eq. 6.1}$$

where L and C are the inductance and capacitance, respectively, of both lines. It turns out that even though L and C each depend on geometry, the propagation velocity itself is not dependent on geometry. When a geometry is reduced, L decreases and C increases such that the product, LC, is relatively independent of geometry. Therefore, the propagation velocity of a wave is determined more by the dielectric constant of the material and less by the geometry.

The reciprocal of the propagation velocity is the "delay per unit length," usually referred to as the "propagation delay."

$$t_{PD} = \sqrt{\left(\frac{dL}{dx}\right)\left(\frac{dC}{dx}\right)} \qquad \text{Eq. 6.2}$$

Figures 6.2a and b show the distribution of the voltage along the line at times $t_1 = x_1/v$ and $t_2 = x_2/v$. At $t_1$, the line voltage is V from $x = 0$ to $x = x_1$ and is zero for $x > x_1$. The voltage travels to the right with a velocity v so that at time $t_2 > t_1$ the voltage has propagated to $x - x_2$. As the voltage travels down the line, it is accompanied by a current which charges the capacitance of the line to voltage V. As the current moves a distance dx, the additional capacitance that is charged to voltage V is $C_{dx}$. The charge required to accomplish this is $dQ = VC_{dx}$. Therefore,

$$I = \frac{dQ}{dt} = VC\frac{dx}{dt} = VCv = VC\frac{1}{\sqrt{LC}} = V\sqrt{\frac{C}{L}} = \frac{V}{Z_O} \qquad \text{Eq. 6.3}$$

The parameter $Z_O = \sqrt{(L/C)}$ is called the "characteristic impedance" of the line.

The current, I, in Equation 6.3 above is the magnitude of current flowing from x = 0 up to the point where the voltage front is located. To the right of the voltage front the current is 0. I is positive when current flows to the right on the upper wire of Figure 6.1 and to the left on the lower wire of Figure 6.1.

Let $I_X$ and $V_X$ represent the current and voltage as a function of line distance, x. When the switch closes, a front of voltage, $V_X$ moves to the right on the line with a velocity, v. A current front, $I_X$, accompanies $V_X$. The distribution of current on the line at the times $t_1$ and $t_2$ is shown in Figure 6.2c and d. The voltage and current on the line, up to their respective fronts, is given by

$$\frac{V_X}{I_X} = \frac{V}{I} = Z_O = \sqrt{\frac{L}{C}} \qquad \text{Eq. 6.4}$$

If the locations of source and load in Figure 6.1 were interchanged, then at the closing of the switch a voltage and current front would start moving toward the left. Using the same sign convention as above, this voltage and current is given by

$$\frac{V_X}{I_X} = -Z_O = -\sqrt{\frac{L}{C}} \qquad \text{Eq. 6.5}$$

The inductance and capacitance of a line can be determined from Equations 6.2 and 6.4 when the propagation delay, line length and line impedance are known. For a length i and delay T, d = T/i. And

$$L = d(Z_O) \qquad C = \frac{d}{Z_O}$$

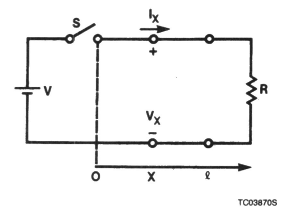
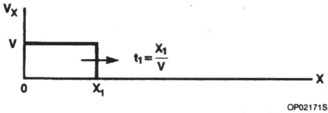
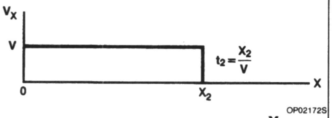


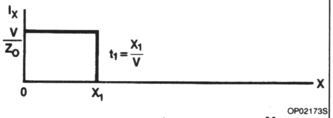
**Figure 6.1. Signal Transmission Line**



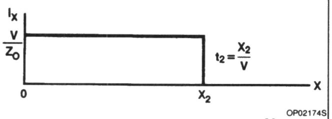
**a. Voltage $V_{X1}$ at Time $t_1 = \frac{X_1}{V}$**



**b. Voltage $V_{X2}$ at Time $t_2 = \frac{X_2}{V}$**



**c. Current $I_{X1}$ at Time $t_1 = \frac{X_1}{V}$**



**d. Current $I_{X2}$ at Time $t_2 = \frac{X_2}{V}$**

**Figure 6.2**

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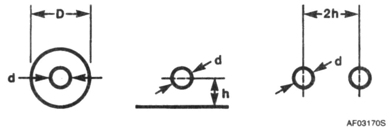
## THE CHARACTERISTIC IMPEDANCE

The characteristic impedance $Z_O = \sqrt{L/C}$ is a function of the geometry of the cross section of the line. The cross sections of three common lines are shown in Figure 6.3, with the expression for their respective capacitances given below each diagram. Since C increases and L decreases with reduced spacing, $Z_O$ will decrease if the spacing between the two parallel wires in Figure 6.3c is reduced. A dielectric introduced between the wires will increase C while L remains unchanged, again decreasing $Z_O$. (However, the propagation velocity is also reduced.)



**a. Coaxial Cable** $C = \dfrac{\pi\epsilon}{\ln {}^{D}/_{d}}$

**b. Wire Over Ground** $C \approx \dfrac{2\pi\epsilon}{\ln {}^{4h}/_{d}}$

**c. Parallel Wires** $C \approx \dfrac{\pi\epsilon}{\ln {}^{4h}/_{d}}$

**Figure 6.3. Three Common Types of Transmission Lines, With Expressions for Capacitance per Meter for Each Type**

While the impedance of the coaxial cable in Figure 6.3a depends on the logarithm of the dimension ratio, the logarithm function varies so slowly with changes of its argument that it is generally not feasible to make very large changes in $Z_O$ by changes in dimension. When attenuation of the line results principally from ohmic losses in the conductors, the loss for a fixed D is a minimum for D/d = 3.6. With D/d = 3.6, using a relative dielectric constant of 2.3, $Z_O = 51\Omega$. Most commercially available coaxial lines have impedances under 100Ω. Parallel-wire lines may have impedances up to several hundred ohms.

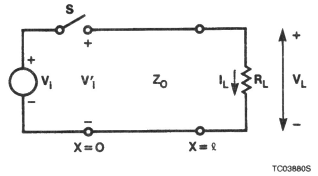


**Figure 6.4. Transmission Line Model**

## REFLECTIONS

Usually a wave incident on a discontinuity is partly reflected and partly transmitted. Any change in characteristic impedance encountered along a transmission line behaves like a discontinuity. This is due to the fact that Ohm's Law, V = IR, must be satisfied at all times at all points along the line. Rearranging Ohm's Law to R = V/I, if $R_1 = R_2$ then $V_1/I_1 = V_2/I_2$, where R is the impedance encountered along the line and V and I are the voltage and current fronts travelling down the line. Therefore, a reflected voltage and current front will develop such that $V_1/I_1$ will equal $V_2/I_2$.

At the moment the switch in Figure 6.4 closes, the voltage source (assumed to have zero internal impedance) applies a voltage V to the line and delivers a current $V/Z_O$ (since the impedance seen by the source looking into the line is the characteristic impedance $Z_O$). If the line is infinitely long so that the fronts of voltage and current never encounter a discontinuity, the fronts would continue indefinitely and there would be a constant impedance $Z_O$ looking into the line.

If the line is not infinitely long, and a resistor $R_L = Z_O$ is bridged across the line to ground, the bridge would look like an infinite extension of the line. Then, when the switch closes, a front of voltage V and current $V/Z_O$ would travel down the line to the right. After a time, t = /v, the fronts will have reached the bridge and from that time on the voltage across the line at any position, as well as the voltage across the bridge, will be V while the current at all points on the line and in the bridge will be $V/Z_O$. In other words, the fronts reach termination and nothing further happens.

If the bridge resistor $R_L$ does not equal $Z_O$, a discontinuity exists. When the fronts arrive at x = they will be related by $V_i/I_i = Z_O$. At x = the impedance is now $R_L$, and the ratio of voltage to current in the initial wave is not equal to the ratio of voltage to current required by $R_L$. Therefore another voltage and current wave is created at x = in order to satisfy Ohm's law at this point; i.e. a reflection will develop and start moving to the left. The amplitude and polarity of the reflected fronts will be such that the sum of the incident and reflected voltage and current will be

$$V_i + V_r = V_L \qquad \text{Eq. 6.6}$$

$$I_i + I_r = I_L \qquad \text{Eq. 6.7}$$

Thus,

$$I_L = \frac{V_L}{R_L} = \frac{V_i + V_r}{R_L} \qquad \text{Eq. 6.8}$$

Also,

$$I_i = \frac{V_i}{Z_O} \text{ and } I_r = \frac{-V_r}{Z_O} \qquad \text{Eqs. 6.9 \& 6.10}$$

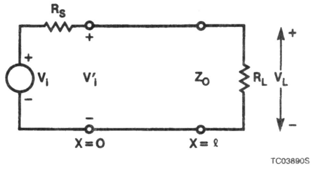


**Figure 6.5. Transmission Line With Source Impedance, $R_S$ and $Z_O \neq R_L$**

Solving for $V_r$,

$$\frac{V_i}{Z_O} - \frac{V_r}{Z_O} = \frac{V_i + V_r}{R_L} = \frac{V_i}{R_L} + \frac{V_r}{R_L}$$

$$= V_i\left(\frac{1}{Z_O} - \frac{1}{R_L}\right)$$

$$= V_r\left(\frac{1}{R_L} + \frac{1}{Z_O}\right)$$

so,

$$V_r = V_i\left(\frac{R_L - Z_O}{R_L + Z_O}\right) = \rho V_i \qquad \text{Eq. 6.11}$$

and

$$I_r = \frac{-V_r}{Z_O} = \frac{-\rho_L V_i}{Z_O} \qquad \text{Eq. 6.12}$$

Where the parameter $\rho_L$ is the "reflection coefficient" at the load end of the line.

Since

$$V_L = V_i + V_r \qquad \text{Eq. 6.13}$$

then

$$V_L = V_i\,(1 + \rho_L) \qquad \text{Eq. 6.14}$$

$V_L$ can also be determined without $\rho$. Using Equation 6.11 above,

$$1 + \rho_L = 1 + \frac{R_L - Z_O}{R_L + Z_O} = 2\left(\frac{R_L}{R_L + Z_O}\right)$$

so

$$V_L = 2\left(\frac{R_L}{R_L + Z_O}\right)V_i \qquad \text{Eq. 6.15}$$

The reflection coefficient lies in the range −1 to +1. When R = $Z_O$, $\rho = 0$; when the end of the line is open, $\rho = 1$; when the end of the line is short-circuited, $\rho = -1$.

A typical situation, where the load is not equal to $Z_O$, is shown in Figure 6.5. A line with impedance $Z_O$ is terminated at the receiving end by $R_L = Z_O$. The source has an impedance $R_S = Z_O$. Let a voltage, $V_L$, of amplitude V be applied at t = 0. The input to the line appears to be a resistance $Z_O$, so at t = 0 + the voltage step at x = 0 is

$$V'_i = \left(\frac{Z_O}{R_S + Z_O}\right) V_i \tag{Eq. 6.16}$$

$V'_i$ travels down the line to the receiving end, where the load would dissipate the entire front and no reflections would occur if $R_L = Z_O$. However, a reflection will develop in this example since $R_L \neq Z_O$. This reflection will again be reflected at the line input, with reflections continuing back and forth. Each time a reflection arrives at the source or receiving ends of the line, its front will be smaller than the incident front so that eventually a steady-state will be established. In the special cases where the reflection coefficients are +1 or −1, excluding the effect of attenuation, a steady-state will theoretically never be attained.

Figure 6.6 shows the effect of the ratio of $R_L$ to $Z_O$. In Figure 6.6a, $R_L > Z_O$ and a positive voltage is reflected back to the source. To the left of $V_r$ the current flowing to the right is $I_i$. To the right of $V_r$ the net current flowing to the right is $I_i - I_r$, a net decrease in current. In Figure 6.6b, $R_L < Z_O$ and a negative voltage is reflected back to the source. To the left of $V_r$ the current flowing to the right is again $I_i$. But to the right of $V_r$ the net current flowing to the right is $I_i + I_r$, a net increase in current.

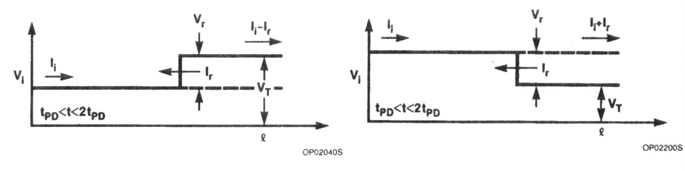
## MULTIPLE REFLECTIONS

The reflection coefficient at the source determines the response to a voltage front reflected back to the source. From Equation 6.11, the reflection coefficient is

$$\rho = \frac{R - Z_O}{R + Z_O} \tag{Eq. 6.17}$$

If the source impedance and line impedance match, the reflected wave will not be reflected back to the load and the voltage and current on the line will be stable with the values given in Equations 6.6 and 6.7. But, if neither the source or load impedance matches the line impedance, multiple reflections will occur.

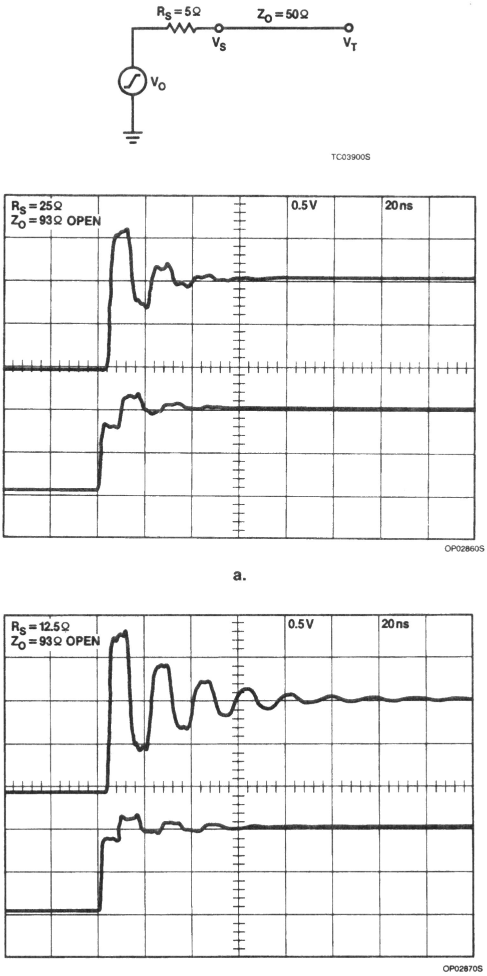
In the presence of multiple reflections, keeping track of the waves on the line and the net voltages and currents at the ends can be very tedious. A systematic method has been de-



a. $R_L > Z_O$

b. $R_L < Z_O$

**Figure 6.6. Effect of the Ratio $\frac{R_L}{Z_O}$**



a.

b.

**Figure 6.7. Multiple Reflections Due to Mismatch at Load and Source**

## User's Guide

veloped to make the job much more convenient. This method combines magnitude, polarity and time into a graph called a lattice diagram. A lattice diagram for the line conditions of Figure 6.7a is shown in Figure 6.8. The vertical lines represent the discontinuities at the ends of the line. A time scale is marked off on each line in increments of 2T, starting at t(o) for $V_S$ and T for $V_T$. The diagonal lines indicate the voltages and currents travelling between the ends of the line.

The reflection coefficient of the unterminated end of the line is +1. Successive reflections tend toward steady-state of zero line current and a line voltage equal to the source voltage. (If the unterminated end of the line were shorted to ground, the reflection coefficient would be −1 and successive reflections would tend toward steady-state of zero voltage and a line current determined by the source voltage and resistance.) A negative coefficient of reflection always reflects voltage in the opposite polarity. A positive coefficient of reflection reflects voltage in the same polarity.

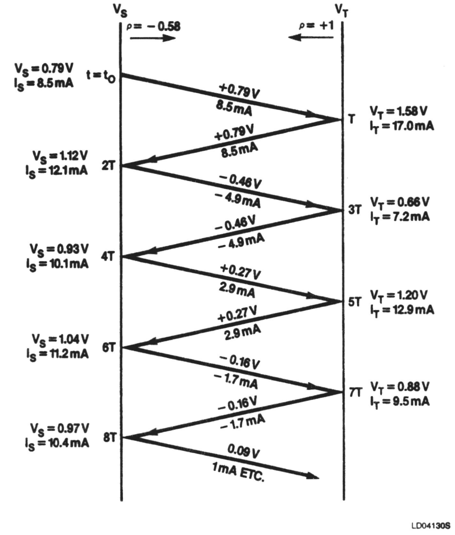
At t = 0, the voltage source switches from 0V to 0.9V. Due to the voltage divider action of $R_S$ and $Z_O$, the voltage at $V_S$ is:

$$V_S = V_{STEP}\left(\frac{Z_O}{Z_O + R_S}\right) = 1V$$

$$= \left(\frac{93}{118}\right) = 0.79V \qquad \text{Eq. 6.18}$$

The voltages and currents at each point on the lattice diagram are determined by summing all the voltages and currents arriving at and leaving from the point. The process continues until the voltage at the end of the line approaches the new steady-state voltage, i.e., 1.0V in this example. Figure 6.7b illustrates the extended ringing when the source, $R_S$, is reduced to 13Ω from 25Ω.

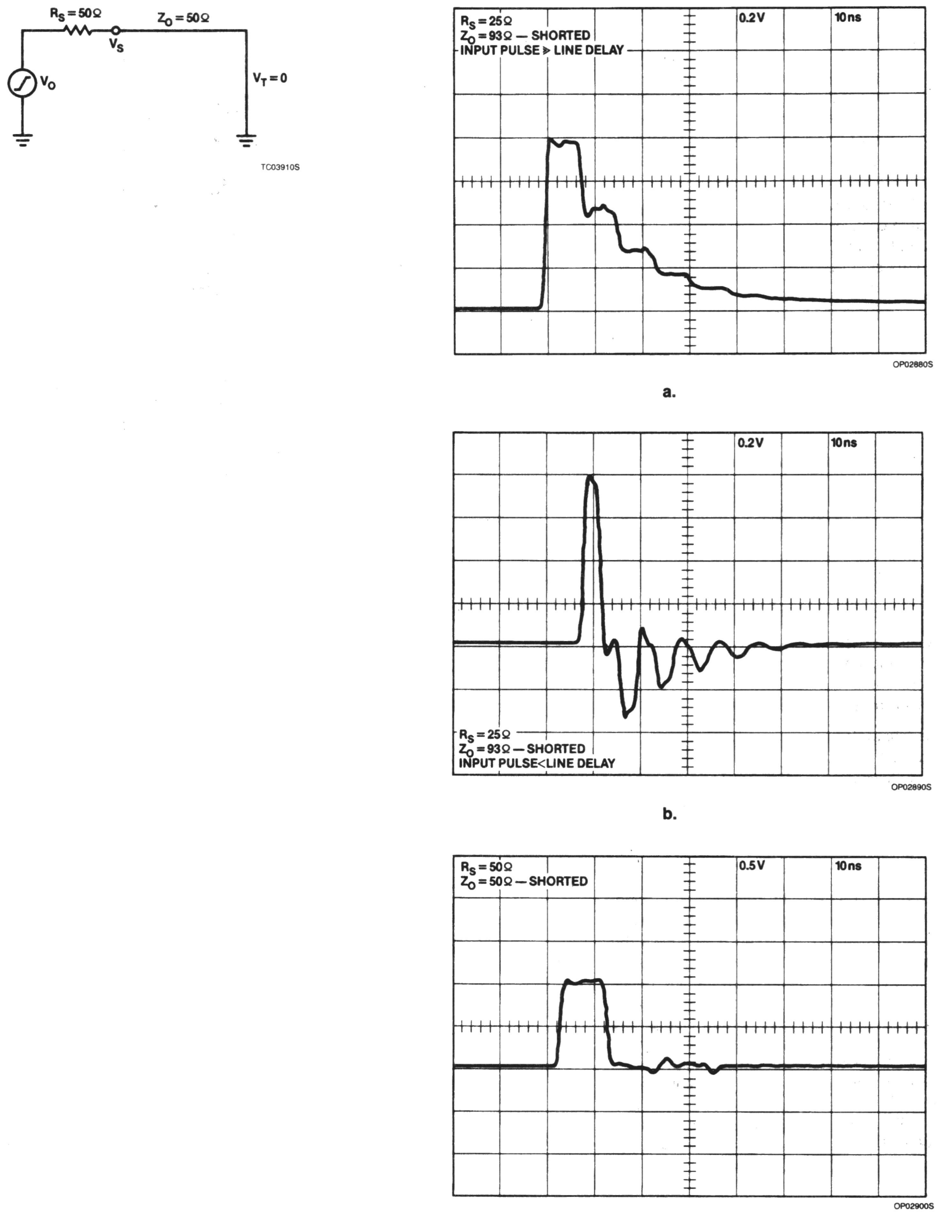
A shorted line, with the reflection coefficient at the source end of the line negative also, is shown in Figure 6.9. Graph 6.9a shows the result when the input step function has a pulse width much longer than the line delay. In this circumstance the reflections constitute a train of positive pulses. Graph 6.9b shows the result when the input step function has a pulse width shorter than the line delay. In this circumstance the reflections constitute a train of positive pulses. Figure 6.9c shows a shorted line for an input pulse duration >> line delay when the source, $R_S$, and the load, $Z_O$, are equal (50Ω in this case).



**NOTES:**

$V_T$ = 0.79V + 0.79V = 1.58V
$I_T$ = 8.5mA + 8.5mA = 17mA
$V_{2T}$ = 0.79V + 0.79V − 0.46V = 1.12V
$I_{2T}$ = 8.5mA + 8.5mA − 4.9mA = 12.1mA
$V_{3T}$ = 1.58V − 0.46V − 0.46V = 0.66V
$I_{3T}$ = 17mA − 4.9mA − 4.9mA = 7.2mA
$V_{4T}$ = 1.12V − 0.46V + 0.27V = 0.93V
$I_{4T}$ = 12.1mA − 4.9mA + 2.9mA = 10.1mA

**Figure 6.8. Lattice Diagram for Circuit of Figure 7.7**



a.

b.

c.

Figure 6.9. Reflections on a Shorted-Line

# Chapter 7
# Interconnections

## PC BOARD INTERCONNECTIONS

Often multilayer PC boards, as shown in Figure 7.1, are used. Interconnections are implemented on one or more layers, with a separate layer (often more) utilized as a ground "plane". The ground plane is a continuous sheet of copper, and the impedance of the ground connection thus becomes so low that the signal appears almost entirely on the signal wire. Therefore, this is a very effective way to reduce ground noise.

The characteristic impedance of a wire over a ground plane is:

$$Z_C = \left(\frac{60}{\sqrt{E_r}}\right) \ln \left(\frac{4h}{d}\right) \qquad \text{Eq. 7.1}$$

where d = wire diameter
h = distance from ground to wire center.

Two common types of PC boards are Microstrip, shown in Figure 7.2, and Stripline, shown in Figure 7.3. Of the two, Microstrip offers easier fabrication and faster signal transmission but complex designs with high packing density will require more design effort. Stripline, providing more interconnect layers, more easily facilitates a high packing density by providing shorter signal paths.

The characteristic impedance of Microstrip, derived from Equation 7.1 above, is given by the following equation:

$$Z_C = \frac{87\Omega}{\sqrt{E_r + 1.41}} \ln \left(\frac{5.98e}{h + 0.8w}\right) \qquad \text{Eq. 7.2}$$

The parameters e, h, and w are defined in Figure 7.2. $E_r$ is the relative dielectric constant of the insulating material.

From Equation 6.2, the propagation delay is a property of the dielectric material rather than line width or spacing, and

$$t_{PD} = 1.016\sqrt{E_r} \ \text{ns/ft.} \qquad \text{Eq. 7.3}$$

where 1.016 is the reciprocal of the velocity of light in free space. The effective dielectric constant can be determined by measuring the propagation delay per unit of length and using Equation 7.3 above.

The characteristic impedance of a Microstrip line, printed in copper on glass-epoxy, is given as a function of dielectric thickness and trace width in Figure 7.4.

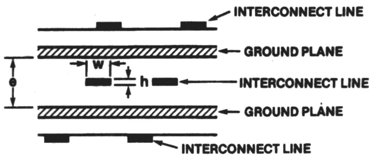


Figure 7.1. Cross-Section of a Multilayer PC Board

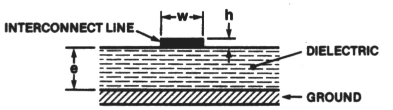


Figure 7.2. Cross-Section of a Microstrip PC Board

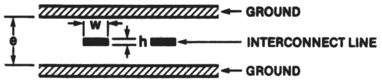


Figure 7.3. Cross-Section of a Stripline PC Board

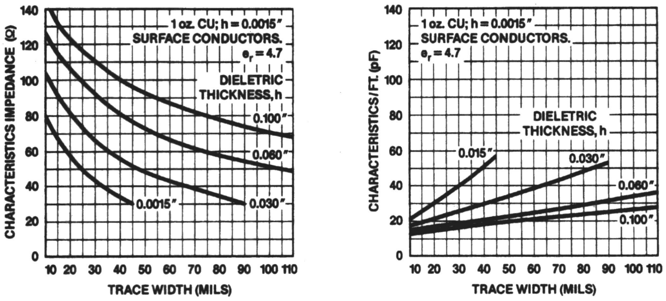


Figure 7.4. Impedance and Capacitance of Microstrip for Various Trace Widths, Printed in Copper on G-10 Epoxy

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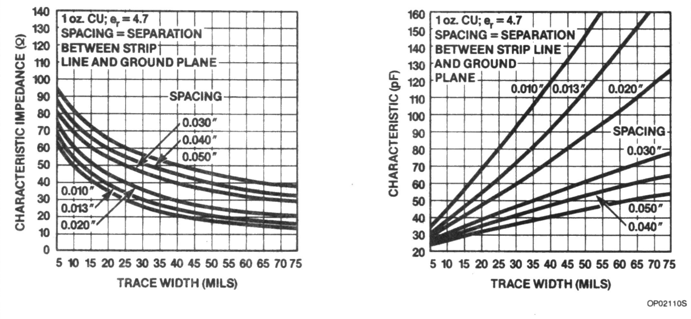


Figure 7.5. Impedance and Capacitance of Stripline, G-10 Epoxy

When the signal line is enclosed between two ground planes, as in Figure 7.3, the board material determines the dielectric constant. G-10 epoxy Stripline boards have a typical propagation delay of 2.26ns/ft. Using Equation 7.3, the characteristic impedance of Stripline is

Eq. 7.4

$$Z_C = \left(\frac{60}{\sqrt{E_r}}\right) \ln \left[\frac{4e}{0.67\pi(0.8\ w + h)}\right]$$

The characteristic impedance of Stripline, printed in copper on glass-filled epoxy, is given as a function of dielectric thickness and trace width in Figure 7.5.

## ECL CIRCUIT INTERCONNECTIONS

Consider the connection of the output of a driving ECL gate to the input of a driven gate. The emitter-follower driver acts like a source. It has a low output impedance ( < 10Ω including the package pin and internal connection). The characteristic impedance of high-speed PC board interconnections is usually in the range of 40 to 60Ω, depending on line width and insulating material used. The line load consists of the input impedance of the gates connected on the line, and any termination resistors that may be present. The input resistance (several kΩ) of gates connected on the line can be ignored because input capacitance, usually several pF, outweighs the effects of input resistance.

A model for the interconnection between ECL gates can be represented by a line of one-way delay, $t_D$, with characteristic impedance, $Z_O$. The sending end termination is $R_S << Z_O$ and the receiving endtermination is $R_L >> Z_O$.

As discussed in the previous chapter on transmission line theory, any change in characteristic impedance encountered along a transmission line behaves like a discontinuity and causes reflections to occur.

## LINE TERMINATION

Let's consider the case where a transmission line has no termination (an "open line"). At $t = 0$, a voltage front, V, starts at $x = 0$ and travels down the line (Figure 7.6). At $t = t_D$, the front reaches $x = 1$ and is reflected with a reflection coefficient of

$$\rho_L = \frac{R_L - Z_O}{R_L + Z_O} = 1 \qquad \text{Eq. 7.5}$$

since the impedance of the load is very high with respect to $Z_O$. At $t = 2t_D$, the reflected front will reach $x = 0$ and be reflected by with a reflection coefficient of

$$\rho_S = \frac{R_S - Z_O}{R_S + Z_O} = -1 \qquad \text{Eq. 7.6}$$

because $R_S$ is very low with respect to $Z_O$. The negative reflection results in a front at $x = 1$ at time $t = 3t_D$ that travels in the opposite direction to the initial front. Positive reflections cause the signal to "overshoot" the initial voltage level, and negative reflections cause the signal to "undershoot" the initial voltage level. When occuring together, these reflections cause a condition known as "ringing."

If the signal line is short, the initial signal will still be rising at $t = t_D$ and the reflection will become part of the rising edge. If the signal line is long, the rise of the signal will be completed before $t - t_D$ and the reflections will act like overshoot and undershoot. Therefore, unterminated lines have a maximum recommended length

$$l_{max} \leqslant \frac{t_R}{2\ t_{PD}} \qquad \text{Eq. 7.7}$$

where $t_R$ = rise time
$t_{PD}$ = propagation delay/unit length.

There are two configurations generally used to terminate transmission lines: (1) terminating the line at the receiving end, which is called "parallel termination;" and (2) driving the line through a resistor inserted at the output of the gate, which is called "series termination." These are shown in Figure 7.7.

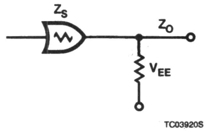
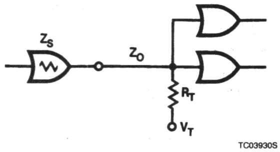
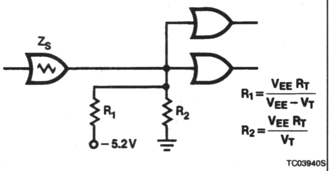


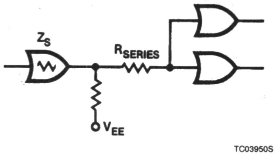
Figure 7.6. Unterminated Transmission Line



a. Parallel Termination Using Auxiliary Supply Voltage


$Z_S$
$R_1$
$R_2$
-5.2V
$R_1 = \frac{V_{EE} R_T}{V_{EE} - V_T}$
$R_2 = \frac{V_{EE} R_T}{V_T}$
TC03940S

b. Parallel Termination Without Auxiliary Supply Voltage



c. Series Termination

Figure 7.7. Termination Configurations

Parallel termination is used for highest speed and for driving distributed loads. Since Signetics' ECL devices do not have internal pull-down resistors on the outputs, the terminating resistor must be returned to a voltage more negative than $V_{OL}$, commonly −2V. No additional pull-down resistors are required at the output of the driving gate.

The configuration shown in Figure 7.7b allows parallel termination without the use of a separate termination supply. In this configuration, a pair of resistors is connected in series between $V_{CC}$ and the $V_{EE}$ supply. The values of $R_1$ and $R_2$ are chosen to provide the Thevenin equivalent of the single resistor to −2V shown in Figure 7.7a.

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There is a trade-off between the two parallel termination configurations. While the latter eliminates the need for a separate $V_T$ supply, its average power dissipation is close to 10 times the power dissipation of the former configuration. Decoupling capacitors are required between the supply and ground for both configurations.

Signetics' ECL output transistors are designed to drive low impedance loads with a maximum output current of 50mA. Using a 50Ω load returned to -2V gives nominal output levels of -0.955V at 20.9mA and -1.705V at 5.9mA. These output levels will vary with load current due to the fact that the transistor's output resistance is nonlinear with load current (the $V_{BE}$ of the emitter-follower is logarithmic with output current). The effective source resistance, using a 50Ω load, is approximately 6Ω in the HIGH state and 8Ω in the LOW state.

The circuit shown in Figure 7.8 can be used to estimate quiescent output levels at various loads. The linearized portion of the output characteristic is given by

$V_{OH}$: $V_{OUT} = -850\text{mV} - (6\Omega)\ (I_{OUT}\ \text{mA})$

$V_{OL}$: $V_{OUT} = -1670\text{mV} - (8\Omega)\ (I_{OUT}\ \text{mA})$

Results are given in Figure 7.9.

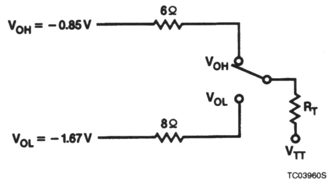


**Figure 7.8. Termination Load Model Circuit**

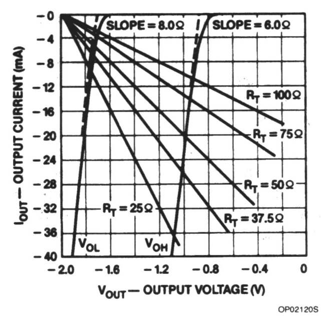


**Figure 7.9. Output Characteristics With Terminating Resistor Returned to $V_{TT} = -2.0V$**

Since ECL outputs can drive two or more lines in parallel (provided the load does not cause the maximum rated current to be exceeded), the effect of load configurations on noise margin should be considered. Using Figure 7.8, two parallel 75Ω terminations provide $V_{OH} = -1.00V$ and $V_{OL} = -1.72V$, approximately. A single 50Ω termination provides $V_{OH} = -0.96V$ and $V_{OL} = -1.73V$, approximately. The single 50Ω termination, therefore, provides 35mV less margin for $V_{OH}$ and 10mV more margin for $V_{OL}$. Two parallel 50Ω terminations provide $V_{OH} = -1.07V$ and $V_{OL} = -1.75V$, 110mV less margin for $V_{OH}$ and 10mV more margin for $V_{OL}$.

When using series termination, a resistor value should be selected such that the driver source resistance plus the series resistor equals the line impedance. The net series resistance and the line impedance act like a voltage divider and cause an incident wave of half amplitude to travel down the line. The coefficient of reflection of an open line is + 1, so when the incident signal arrives at the unterminated end of the line it will double and be restored to its full amplitude. If the combination of the series resistor and drive source resistance equals the line impedance, the reflected wave will be absorbed without further reflection, eliminating any possibility of ringing. The ability to absorb reflected waves makes series termination good for interconnection configurations having impedance discontinuities, such as backplane wiring.

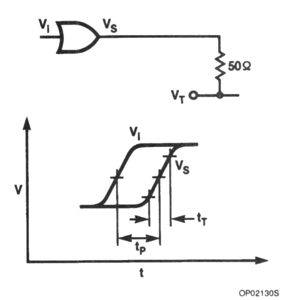


**Figure 7.10. ECL Gate Output Characteristic With 50Ω Load**

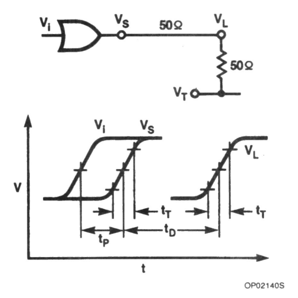


**Figure 7.11. ECL Gate Output Characteristic With Matched Long Line**

A disadvantage of series termination is that driven inputs must be near the end of the line to avoid receiving a 2-step signal. An input will receive a full amplitude signal with a continuous edge provided the distance, l, to the open end of the line is within the recommended length for unterminated lines (Equation 7.7).

## MATCHED LONG LINES

The output signal of an ECL gate with a 50Ω load is shown in Figure 7.10. An applied input voltage, $V_{IN}$, has a corresponding output voltage, $V_S$, characterized by a propagation time, $t_P$, and a transition time $t_T$.

A line having characteristic impedance of 50Ω, terminated by a resistor having the same value, behaves like a pure 50Ω resistor and, therefore, can be used to load the gate without affecting its behavior (Figure 7.11). The output voltage $V_S$ of the gate has the same $t_P$ and $t_T$ as in Figure 7.10. $V_S$ propagates along the line until it reaches the load resistor. The voltage across the 50Ω load resistor will be identical to $V_S$ after a time equal to the propagation delay of the line.

## MISMATCHED LONG LINES

If the load terminating the line is not a 50Ω resistor, as shown in Figure 7.12, the output voltage remains the same as it was in the preceding case and is transmitted over the line in the same manner. However, the voltage will be deformed by the load voltage, $V_L$, when it arrives at the load and will not have the same form as $V_S$. If the load is capacitive, then the edge $t_{T2}$ will be slower than the edge at the gate output $t_{T1}$, and an additional delay will be added to $t_D$. Also, because the resistive portion of the load differs from 50Ω, the amplitude of $V_L$ will be different.

The effect of a load can be calculated from the diagram shown in Figure 7.13. The difference between $V_L$ and the incident wave, $V_S$, will be reflected toward the gate causing a perturbation in the voltage at time $2t_D$.

## SHORT LINES

If the line is short; i.e., if $t_D$ is less than or equal to $t_T$, then it is difficult to separate $V_S$ and $V_L$ at the line terminals. Therefore, it is preferable in this case to discard the transmission line concept and work instead from the equivalent diagram shown in Figure 7.14.

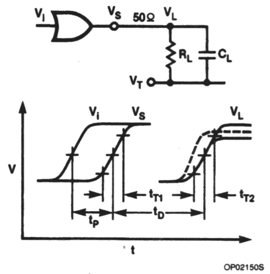


**Figure 7.12. ECL Gate Output Characteristic With Mismatched Long Line**

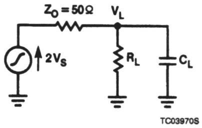


**Figure 7.13. Equivalent Load Circuit**

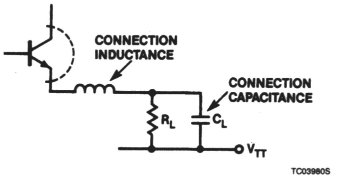


**Figure 7.14. Equivalent Circuit for Short Line**

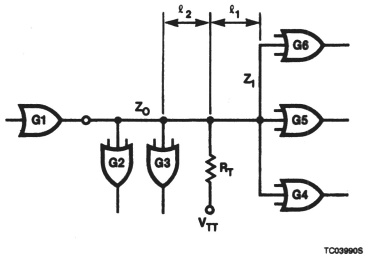


**Figure 7.15. ECL Gate Driving Multiple Lines**

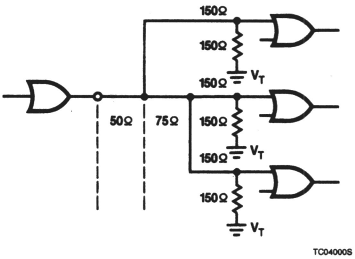


**Figure 7.16. 50Ω Line Branched Into Three 150Ω Lines**

## MULTIPLE LINES

Figure 7.15 shows an ECL circuit driving multiple lines. The signal from gate $G_1$ is distributed successively to gates $G_2$, $G_3$ and to the group of gates, $G_4$ through $G_6$. A matching resistor, $R_T$, is placed as far as possible down the line to minimize the length, $L_1$, of "non-terminated" line.

The effect of the capacitance of this non-terminated, and therefore unmatched, portion is reduced by giving it a high characteristic impedance, $Z_1$. The reflections generated by the input capacitances of gates $G_4$ through $G_6$, and the unmatched line segments that connect them to the main line, should be limited to 15% or 20% of the amplitude of the signal to maintain proper noise immunity between the gates. This factor is usually the main limitation to fanout.

The product ($Z_C \times C_T$), where $C_T$ is the sum of the capacitances loading the line, should not exceed the transition time, $t_T$, of the signal driving the line. Therefore, it is the input capacitance of the other gates that causes the limitation to fanout. Fanout is typically 3 gates, but can exceed 8 gates if the system is well designed.

It is possible to branch a 50Ω line into two 100Ω lines, or three 150Ω lines, as shown in Figure 7.16. In this configuration, each line is terminated by a load corresponding to its characteristic impedance.

## BUS LINES

Bidirectional buses for ECL can be constructed by interconnecting gate outputs and inputs along a matched line terminated at both ends. Each gate output will then appear to be loaded by two lines in parallel; i.e., by $Z_C/2$. In this configuration, a signal can be propagated from one gate to another gate only if the outputs of the non-active gates are in the LOW state.

Bus drivers are available to provide optimum results under these conditions. These devices can generally provide more current and voltage that ordinary gates, and with less sharp edges, to minimize reflections.

# Chapter 8
# Power Supplies

## POWER SUPPLY CONFIGURATIONS

The most common power supply network used in ECL systems consists of three distribution lines (Figure 8.1):

1. the overall $V_{CC}$ line;
2. the termination voltage, $V_T$, line; and
3. the switching-state voltage, $V_{EE}$, line.

Two different voltage sources are used to supply $V_T$ and $V_{EE}$. $V_T$ is on the order of −2V, and $V_{EE}$ is on the order of −4.5V to −5.2V, depending on the family. Thus, the network consists of two interleaved current loops, each with different functions.

The $V_{EE}$ loop supplies the current for the biasing networks, the switching stages, and for some of the internal circuit loads. These currents are relatively constant. As explained in the preceding chapter, gate function is insensitive to the value of $V_{EE}$. The $V_{EE}$ power supply receives almost no high-frequency current components when the gates switch.

The $V_T$ loop supplies the current for the gate output loads. This current is affected by sudden transients. Using a 50Ω output resistor, this current changes from 8mA to 22mA within one or two nanoseconds whenever the gate output switches.

The $V_{CC}$ connection, which serves as a reference potential for the logic signals, receives the sum total of these two currents simultaneously (one with a strong continuous component and the other with a strong alternating component).

## STATIC PARASITIC EFFECTS

The power density distributed on boards implemented in ECL can exceed $10W/cm^2$. This means that currents passing through the board can reach $2A/cm^2$. These currents can cause ohmic voltage drops in the distribution lines, in connectors, in printed circuit traces, and even in the package pins themselves. Therefore, all circuits do not receive exactly the same $V_{CC}$ voltage.

A difference between supply voltages can cause a reduction in noise immunity. For example, if a 20mV loss of noise immunity is acceptable, then the line must represent less than 0.02V/2A = 0.01Ω. A resistance this low requires a large cross-section for $V_{CC}$ connections.

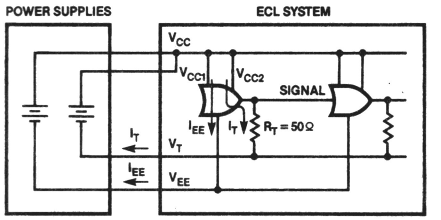


Figure 8.1. ECL Power Supply Network

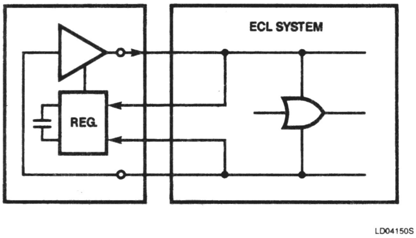


Figure 8.2. Kelvin Connection of Power Supplies

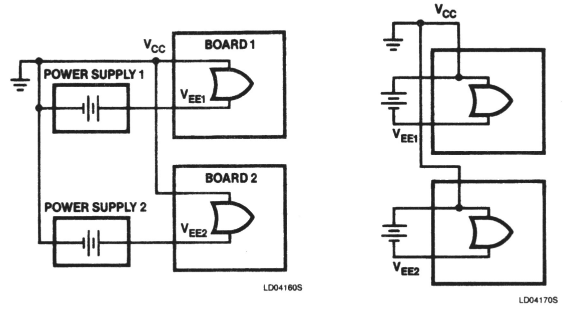
The effect of $V_{CC}$ on noise immunity is four times larger than that of $V_{EE}$ for 10K ECL, and approximately twenty times larger (due to the bias regulator) for 100K ECL. Consequently, a larger distribution resistance is tolerated by $V_{EE}$.

The effect of $V_T$ on output levels and noise immunity depends on the relationship between the load resistances (50Ω) and the gate output resistance (6 to 12Ω). It turns out, therefore, that $V_T$ is just as tolerant of voltage drops as $V_{EE}$ is.

Depending on whether a system consists primarily of simple circuits (with many outputs per gate) or of complex circuits (with many gates per output), either the $V_T$ line or the $V_{EE}$ line will be the more critical from the point of view of static voltage drops. Power supplies that provide both $V_T$ and $V_{EE}$ also reduce static noise immunity as a function of loading. This should be kept in mind when designing a system.

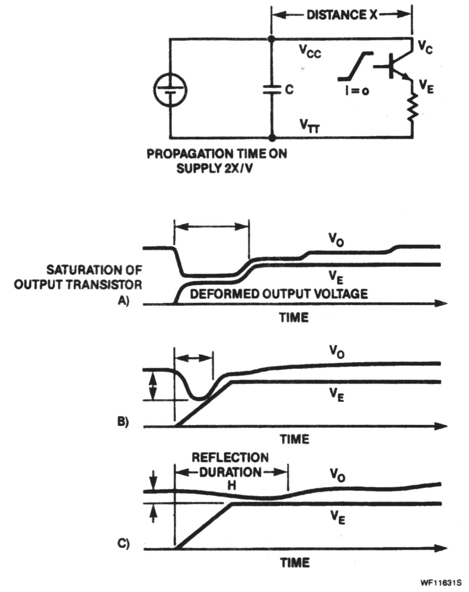
In small systems using one power supply it is advisable that the power supply and its regulator be connected by four separate lines: two to carry the input current, and two for remote voltage sensing. This technique, known as a "Kelvin connection," is shown in Figure 8.2.

When several sub-systems have independent power supplies, a power supply connection, as shown in Figure 8.3b, prevents current passing through the link between the $V_{CC}$ lines and guarantees the supplies will provide equal voltages.



**a. Wrong: Non-Equipotential $V_{CC}$** **b. Right: Equipotential $V_{CC}$**

**Figure 8.3. Coupling of Multiple Power Supplies**



**A) Capacitor too far away**
**B) Capacitor nearby**
**C) Distribution with low characteristic impedance**

**Figure 8.4. Decoupling of an ECL Gate**

## DYNAMIC PARASITIC EFFECTS

Figure 8.4 shows the effect of distance between the decoupling capacitor and output pin of an ECL circuit. The distance, x, acts like an inductance in series with the circuit and limits the effectiveness of the decoupling regardless of the value of the capacitor. Too large a distance between the decoupling capacitor and output pin could allow saturation of the output transistor and create a significant delay in response.

Two methods of decoupling are generally used. One consists of placing a decoupling capacitor at a distance of less than one centimeter from each 100K ECL package, and at a distance of less than five centimeters from each 10K ECL package (as shown in Figure 8.4b). These capacitors should, of course, be suitable for very high-frequency decoupling — several tens of nanofarads in value and constructed with high-quality dielectric material with low absorbtion characteristics.

In the second method, shown in Figure 8.4c, a long duration of reflection is acceptable because the reflection's amplitude is reduced by the power distribution having a very low characteristic impedance, thus providing an equivalent low inductance. This is obtained by means of large capacitors located near one another. In this case, the best solution is to use a multi-layer PC board with separate parallel planes for ground and $V_{TT}$. (If using a single- or dual-layer PC board, capacitance rails can be placed vertically on the PC board.) The impedance of the two parallel plane conductors can be calculated from:

$$Z_C = \frac{120\pi ht}{d\sqrt{E_r}} \qquad \text{Eq. 8.1}$$

where:

h = the thickness of the dielectric between the conductors
d = the width of the smaller conductor
t = the relative dielectric constant of the insulating material
$Z_C$ = the characteristic impedance (expressed in $\Omega$)

With $Z_C < 1\Omega$, currents on the order of 20mA will cause voltage fluctuations of less than 20mV on the power supply lines, which is acceptable. Having $Z_C$ too high risks interaction between two circuits, even in the absence of a signal on their inputs, due to fluctuations of voltage on the $V_{CC}$ line. This in turn creates a risk of oscillation. On isolated circuits, excessively inductive power supplies can cause coupling to occur between inputs and outputs. The resulting oscillations can, over the longterm, destroy some junctions in the input stage or in the regulator.

# Chapter 9
# Packages and Thermal Constraints

Integrated circuits implemented on silicon chips must generally be mounted in a package to be used. This package, located between the circuit and its environment, imposes its own characteristics, or modifies those of the chip. In ECL, this effect is especially important.

## ROLE OF THE PACKAGE

First of all, the silicon chip is very small, mechanically fragile, and difficult to handle. It can be subject to corrosion, especially at the level of its connections to the outside world (metallic interfaces).

Finally, the chip is a major source of heat during operation. This heat must be removed efficiently to avoid the risk of rapid destruction of the chip due to excessive temperatures.

In view of these problems, the package provides greater ease of handling, and mechanical protection for the chip against shocks, scratches, and corrosive atmospheres. It also makes connections to the circuit easier, by connecting the fragile, microscopic areas on the silicon to sturdy metallic pins, which are accessible and easy to solder. This also makes circuit testing easier. On the thermal level, the package conducts the heat of the chip toward a larger surface area, and also makes chip-cooling easier to control.

## THERMAL BEHAVIOR OF THE PACKAGE

The silicon chip acts as a heat generator connected to a heat media (the ambient air) by means of an environment consisting of different substances that present a resistance (depending on their type and size) to the circulation of the thermal flow.

The temperature of the chip is an important parameter, for both the electrical performance of the circuit and its reliability. It should be noted that the lifetime of a component is reduced by half for each 10°C increase in temperature. This is true for all logic families; but ECL circuits require more attention because their power level is generally higher.

The calculation of thermal resistances depends on several factors.

The chip acts as a heat generator which, by means of the Joule effect, provides a power W which it receives in electrical form from its power supplies. This power W has approximately the value of the product $V_{EE} \times I_{EE}$, to which must be added the power dissipated in the output transistors: $(V_O \times I_O)$. The power associated with the inputs can generally be ignored (see Figure 9.1).

In order for this heat to be removed, the temperature of the chip must increase above that of the surrounding environment. The ratio between the difference in temperature (once it has stabilized) and the amount of heat dissipated is termed the "thermal resistance", $\theta$.

Each element in the path of the thermal flow thus presents resistance, and the entire set of resistances is associated, in series or in parallel, to form the overall thermal resistance.

Thus, the package shown schematically in Figure 9.2 behaves thermally in a way that is analogous to the thermal behavior of the network shown in Figure 9.3. The characteristic temperatures are $T_1$ (the temperature of the junctions on the chip), $T_3$ (the temperature of the package wall), and $T_5$ (the initial temperature of the cooling air).

The thermal resistances to be taken into consideration belong to three types:

1) Conduction thermal resistances in solids: such as the silicon of the chip, the ceramic or plastic of the package, the metal of the pins, the glass-epoxy plane and the copper traces of which the printed-circuit board consists, etc.;
2) Convection thermal resistances related to a fluid medium: exchanges between the package wall and the ambient air, and (if applicable) between the wall of a tube and the cooling liquid, heat-transport phenomena within fluids in motion (ventilated air);
3) Radiation thermal resistances related to the heated surfaces. Some of these resistances are determined by the circuit manufacturer, who generally specifies the thermal resistance $\theta_{JC}$ between the internal heat-source (junctions of integrated circuits) and the package wall. On the other hand, the rest of these resistances depend on the user, who defines the mechanical assembly (part of the heat being dissipated via connections) and the ventilation conditions.

Thermal resistances can be calculated based on the specific thermal conductivities of the materials used.

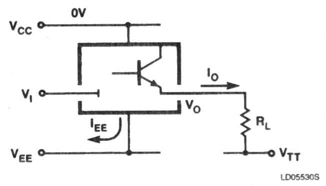


**Figure 9.1. Evaluation of the Power Dissipated**

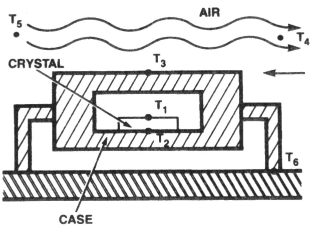


**Figure 9.2. Thermal Analysis of a Flat Pack Package**

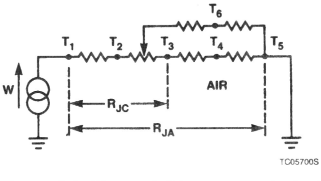


**Figure 9.3. Thermal Diagram Equivalent to the Package Shown in Figure 9.2**

Good thermal conductors, such as gold, aluminum, and copper, have conductivities from 200 to 400W/cm/°C; steel and alumina (of which ordinary packages are made) have lower conductivities, e.g., 15 to 30W/cm/°C. Still air and plastic substances (epoxy, etc.) are bad thermal conductors, typically having conductivities of less than 0.2W/cm/°C.

The standard method of removing heat from the package to the ambient environment is a mixture of convection and radiation, for which the theoretical analysis is very difficult. The power emitted by radiation is proportional to the surface area of the package, and to the fourth power of the absolute temperature of the emitting body (Stefan's Law), and depends greatly on the color of the package and on the condition of its surface.

Surfaces that are matte black in color allow better emission. However, within a system, this phenomenon is very limited, because the energy radiated by a package is essentially re-absorbed by the packages surrounding it, and vice-versa. Overall, this phenomenon does not contribute toward cooling the system.

Therefore, the principal phenomenon is convection, whether natural (air movement caused by the difference in density between the air heated by the package and the surrounding air) or forced (by a fan with a known speed).

Thermal resistance decreases as the air-flow increases, and as the surface area of the package exposed to the flow increases. ECL packages are generally specified for a transverse air-flow of 2.5 meters per second.

For low air-flow speeds (those less than one m/s, or natural convection), thermal resistance is not very well defined, and depends greatly on the environment and on the measurement conditions, inasmuch as the actual air-speed at the level of the package wall can be non-homogeneous, or very different from the measured speed.

Figure 9.4 shows, for a flat ECL 100K package, an example of the variation of the junction-to-ambient-air thermal resistance as a function of the air-flow rate. Therefore, it is important to ensure good ventilation of the circuits, so as to be certain of the measurement conditions and of the operation of the circuits.

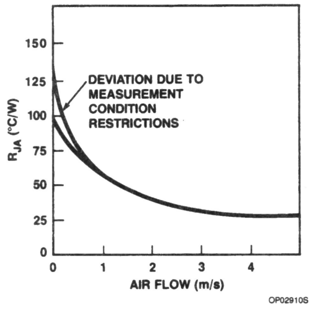


**Figure 9.4. Thermal Resistance of a Flat ECL 100K Package as a Function of the Air-flow Rate**

It should be noted that in very dense ECL systems containing many LSI packages side-by-side, some manufacturers use a cooling liquid (water or freon), because air-cooling is not sufficient to maintain a reasonable temperature at the junction area.

## PRINCIPAL ECL PACKAGES

The ECL logic families, and memories, are available in conventional plastic or ceramic dual-in-line packages (DIPs). ECL 10K comes in 16-pin packages, and ECL 100K in 24-pin packages. The thermal resistance of the 16-pin package is approximately 50°C/W, and that of the 24-pin package is approximately 35°C/W, under normal utilization conditions (transverse air flow of 2.5m/s). In the absence of ventilation, these values can double or triple, which would be harmful to the circuits. The advantage of these packages is their easy insertion into boards, which makes them compatible with the utilization of automatic-insertion equipment. The disadvantage is that electrical performance of extremely fast circuits, such as ECL 100K, is penalized by 200 to 400ps.

For these reasons, another type of package is preferred by some customers: the "flat pack." ECL 100K is available in a flat, square, 4 × 6-pin package, which has a thermal resistance of 30°C/W under normal conditions. Because of the smaller size of this package, the propagation time through the pins is shorter (on the order of 50ps), and parasitic inductances are smaller. The ability to place the packages closer together also makes it possible to reduce the length (and thus the propagation time) of connections between packages. However, these packages are more delicate, requiring greater care in handling and mounting, and are therefore more expensive to use.

When even denser interconnections are necessary, it is also possible to use ECL circuits in micropackages ("mini-DIP") or in leadless chip-carriers. This approach can cause problems for circuits having high power dissipation, but many 10K device types can be put into the SO package and are being offered as customer demand dictates. A ceramic J-lead chip-carrier package has been developed for 100K devices and will be available in the very near future. Contact your Field Applications Engineer or salesman for information.

In the case of highly complex integrated circuits (such as gate arrays), the amount of power dissipation (several watts) and the number of pins (50 to 200) require special attention. Special packages have been designed to solve these two problems, and several types can be utilized, depending on whether the cooling is by air or by a liquid, and depending on the method selected for placing them on the printed circuit board.

# Chapter 10
# Interfacing ECL Families

ECL is sometimes used in a system only in areas in which speed is critical. The rest of the system is implemented in slower technologies. Therefore, it is necessary to know how to interface between ECL circuits and other circuits. Precautions are also necessary when ECL circuits belonging to different families are connected to one another; and even when circuits in the same family, but located on different cards or in different sub-systems, are connected. This section provides several recommendations for implementing these interfaces.

## INTERFACING 10K ECL TO 100K ECL

The problems encountered are mainly due to circuit power supplies and to the different behavior of logic levels depending on the temperature. With regard to the power supply, the ground for the two circuits should be the same. ECL 100K can operate at −5.2V and specification guarantees over this supply range are given in this data book for each Signetics 100K device. On the other hand, generally speaking, ECL 10K cannot operate at −4.5V. Therefore, two methods can be used. First, one could use two separate $V_{EE}$ power supplies, which would be complicated and expensive; or else one could use a single −5.2V power supply. The latter solution is generally preferred when 100K circuits are in the minority in a system.

The diagrams in Figure 10.1 and Figure 10.2 show that direct 10K/100K coupling is functional throughout the temperature range, even though noise-immunity is reduced (mainly when an ECL 100K circuit controls a 10K circuit at high temperature).

In this case, it is recommended that the supply voltage of the 10K circuit be increased slightly (for example, to −5.5V). A more rigorous approach consists of utilizing a special 100K/10K interface circuit (100175), which has 100K input thresholds and 10K output levels. The "buffer register" function of this circuit also facilitates the asynchronous transfer of data between sub-systems, at different speeds.

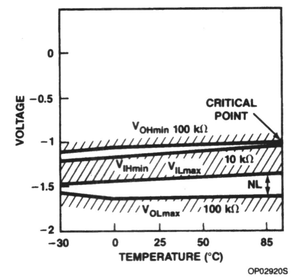


**Figure 10.1. Static Levels — an ECL 100K Output Controlling an ECL 10K Input**

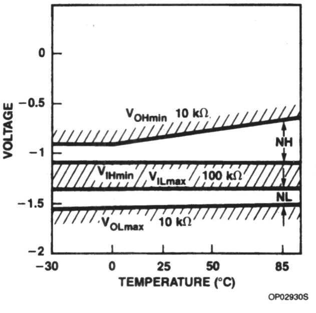


**Figure 10.2. Static Levels — an ECL 10K Output Controlling an ECL 100K Input**

## INTERFACES BETWEEN ECL BOARDS

By utilizing the conventional interconnection system consisting of wires or "wrapped" panels between ECL boards, one risks causing phenomena such as ECL signal reflections at impedance discontinuities, or signal cross-coupling via radiation or by mutual capacitance.

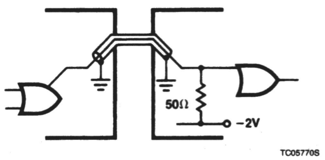


**Figure 10.3. Interconnection Between Boards Via a 50Ω Coaxial Cable**

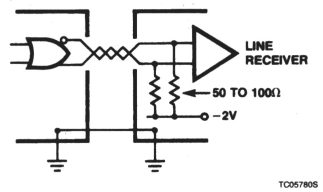


**Figure 10.4. Twisted-Pair Cable Link**

Because the magnitude of these effects increases with the frequencies present in signals transmitted, and therefore with the sharpness of the edges, the simplest solution is to filter the signals as they are output from the boards by utilizing output circuits with especially slow edges (ECL 10K rather than ECL 100K), or special circuits. The outputs can also be slowed by capacitors on the order of 100pF, but the slopes obtained are not symmetrical (faster on the rise).

A radical solution to this type of problem is to implement the interconnections between boards by means of 50Ω coaxial cables.

This method is used when the connections are fairly few, because of the high cost of this technique (see Figure 10.3).

Good results can also be obtained with twisted-pair wire connections driven by complementary signals. These signals can be provided by most ECL gates.

The symmetrical dual-wire line has a regular characteristic impedance, and emits very little radiation. Therefore, its performance is scarcely worse than that of a coaxial cable. It also has the advantage of allowing the use of more conventional connectors. At the end of the line, a special "line receiver" with differential inputs should be used (see Figure 10.4).

This type of link allows great noise immunity, even when the grounds of the boards do not have exactly the same potential.

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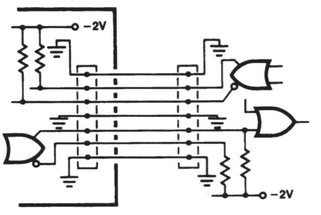


**Figure 10.5. Flat-cable Link**

If absolutely necessary, ECL 10K signals can be transmitted via flat or ribbon cables provided that the signal and its complement are transmitted simultaneously on adjacent lines, so as to reduce radiation and coupling, and to systematically separate the pairs thus formed by ground lines. Thus, structures are obtained whose characteristic impedance is fairly regular, as indicated in Figure 10.5.

For short connections, a line receiver is not necessary. The characteristic impedance of flat cables is generally indicated by the cable manufacturer, so that the termination resistor can be selected.

All of these precautions become less critical when the links are short. Nevertheless, a signal connection should never be placed as far as several millimeters from a ground-plane, or from a connection transmitting the complementary signal. This way most echos and parasitic radiation can be avoided.

## INTERFACE TO TTL CIRCUITS

The following remarks pertaining to TTL circuits also apply to all the circuits that are compatible with TTL levels and power supplies (TTL, TTL-LS, TTL-S, NMOS, and 5V CMOS circuits).

In all large systems in which ECL is utilized extensively, there is a negative power supply ($V_{EE}$) for ECL, and a separate positive power supply ($V_{CC}$) for TTL. These power supplies share a common ground. Translation circuits must be used to transmit signals between the two groups (see Figure 10.6).

There are two types of translation circuits:

1. Unidirectional interfaces, having inputs in one logic family, and outputs in the other. These perform very simple logic functions, as indicated below:

   TTL/10K interface: 10124

   10K/TTL interface: 10125

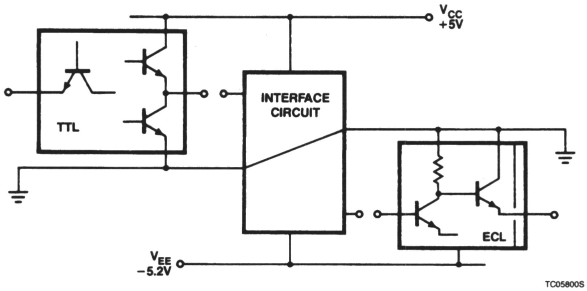


**Figure 10.6. ECL/TTL Interfaces**

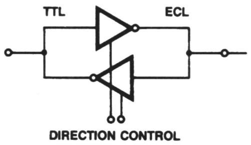


**Figure 10.7. Bidirectional Interface**

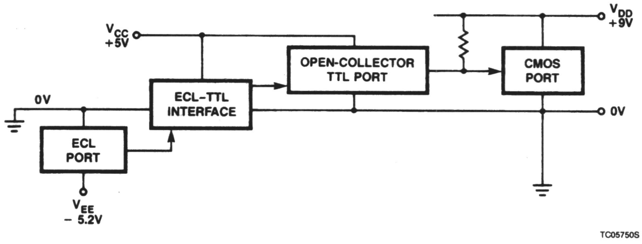


**Figure 10.8. ECL/CMOS Interface Passing Through TTL Levels**

   TTL/100K interface: 100124

   100K/TTL interface: 100125

2. Bidirectional interfaces, allowing transmission in both directions, controlled by auxiliary logic signals, to define the direction of transmission and (in some cases) to improve the signal (see Figure 10.7). For example:

   TTL 100K interface: 100255

## INTERFACE TO CMOS CIRCUITS

Some CMOS circuits require power at 9 to 12V, and have no TTL-compatible levels.

Although direct interfaces with ECL are fairly rare, they are possible by interfacing first via an ECL/TTL translation circuit, and then through a TTL gate with an open-collector output.

This interface is complex to use (see Figure 10.8). Furthermore, if there is no $V_{CC}$ power supply for TTL within the system, it would be wiser to build the interface with discrete components.

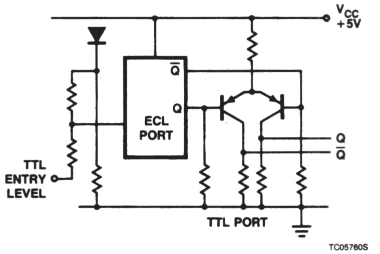


**Figure 10.9. Single-Voltage ECL/TTL Interface**

## SINGLE-SUPPLY TTL INTERFACE

In systems in which a single ECL circuit must be added and interfaced to TTL circuits, it is possible to avoid having to provide a special power supply for ECL by using the circuit with TTL power supplies.

The necessary level translation is achieved by a differential stage (consisting of discrete components) in the ECL-to-TTL direction, and by a diode-resistor network in the other direction (see Figure 10.9).

## ANALOG ECL INTERFACE

High-speed digital signal-processing applications are becoming more and more common. For these purposes, digital-to-analog converters (DACs) and analog-to-digital converters (ADCs) have been developed whose logic is compatible with ECL levels. The ADC converters are the simultaneous parallel conversion type; some of them allow sampling frequencies greater than 50MHz. DAC converters are simpler, utilizing current-source switching controlled by ECL gates.

# Chapter 11
# Circuit Boards

## THERMAL MANAGEMENT

At the board level, local overheating must be avoided. As a general rule, ECL circuit boards are cooled by moving air.

Overheating can be caused by either of two mechanisms:

1. The temperature of the air flow increases from the time it enters the system until it leaves, and the circuits located near the output risk reaching excessively high temperatures;
2. A component that is taller than the others can screen the flow of air from the other circuits.

Components subjected to overheating suffer a modification of their electrical characteristics. Moreover, their lifetime can be shortened considerably.

The board itself can contribute significantly to the removal of heat from the circuits, if care is taken to place it in close contact (via its edges) with the metallic chassis of the equipment. In some cases, the chassis itself can be cooled by a liquid (water or freon).

## BOARD PRECAUTIONS

Generally speaking, the use of sockets is not recommended. On the contrary, circuits should be soldered directly onto the boards. This applies even to prototypes. Doing so avoids problems with oscillations or signal deformations caused by unsuitable connections. When it is absolutely necessary (as in the case of a test board, or of accelerated aging), a connection length less than 6mm should be used.

With regard to accelerated-aging boards (i.e. "burn-in"), it is important that all pins have electrical conditions that reflect normal operation, and that the power supply and environmental conditions respect the *maximum junction temperature* specified. (Somewhat paradoxically, this means cooling of the burn-in chamber, more often it means heating of the chamber!)

It is recommended that specially-designed burn-in chambers be used for ECL circuits because standard chambers risk insufficient temperature and air-flow control.

The section on interconnections explained why careless or semi-accurate implementation could lead to erratic operation and to reduced immunity to system noise. As an example, the use of wired-OR connections causes variations in the static and dynamic characteristics of the outputs connected between them. Because each output carries a smaller average current, it sees its static voltage levels $V_{OH}$ and $V_{OL}$ increase by several tens of millivolts. With regard to dynamic characteristics, the switching gate sees a line loaded by the outputs of other gates. If these gates are located too far from one another for the signal to reach them before it has completed its transition, then multiple echos will occur and the resulting signal will have undesirable oscillations.

Another necessary precaution concerns unused inputs or outputs. All outputs, *even those not used*, must be connected to $V_T$ via a load resistor. If this precaution is not taken, then (1) the internal voltage drops of the circuit will be affected, significantly affecting the other outputs, and (2) for circuits with fast edges, having complementary outputs, a break in the load symmetry will cause irregular current "calls" on the auxiliary $V_{CC}$, possibly causing significant perturbations of the shape and duration of the (waveform) edges of the gate.

It is wise to connect all unused inputs to $V_T$ (if they are in the LOW state). This procedure is a must for some circuits, like line receivers or certain memories, which do not have internal pull-down resistors on all their pins. For inputs that must be kept in the HIGH state, a small auxiliary source (on the order of $-0.8V$) should be used, formed by a diode and a resistor located between $V_{CC}$ and $V_T$. These inputs can also be connected to a HIGH output of an unused gate. Some circuit inputs may be connected directly to $V_{CC}$, but this is not generally the case. Use of this method requires prior consultation with the vendor.

Furthermore, very long lines on the board can capture parasitic signals arising from a local electromagnetic field. It is possible to reduce this interference by interposing lines, or zones, connected to ground between the lines, driving the signals over a given distance.

Care should be taken to implement all ground connections (such as the bottom ends of load resistors or of decoupling capacitors, and the shielding of coaxial cables) by means of a short, wide conductor, to limit parasitic inductances. In fact, any loop, even one that appears small, presents an inductance and can radiate a high-frequency signal.

## DEVICE PRECAUTIONS

High-speed components require very small dimensions, which limit the breakdown voltages of the transistors, allowing them to be destroyed by relatively small energies. Therefore, it is very important that the limit values for voltages, currents, and power recommended by the vendor be respected, even when the equipment is turned on and off.

In particular, care should be taken not to apply $V_T = -2V$ to the inputs and outputs before $V_{EE}$ is applied.

Likewise, short-circuiting an output directly to $V_{EE}$ or to $V_T$ should be avoided.

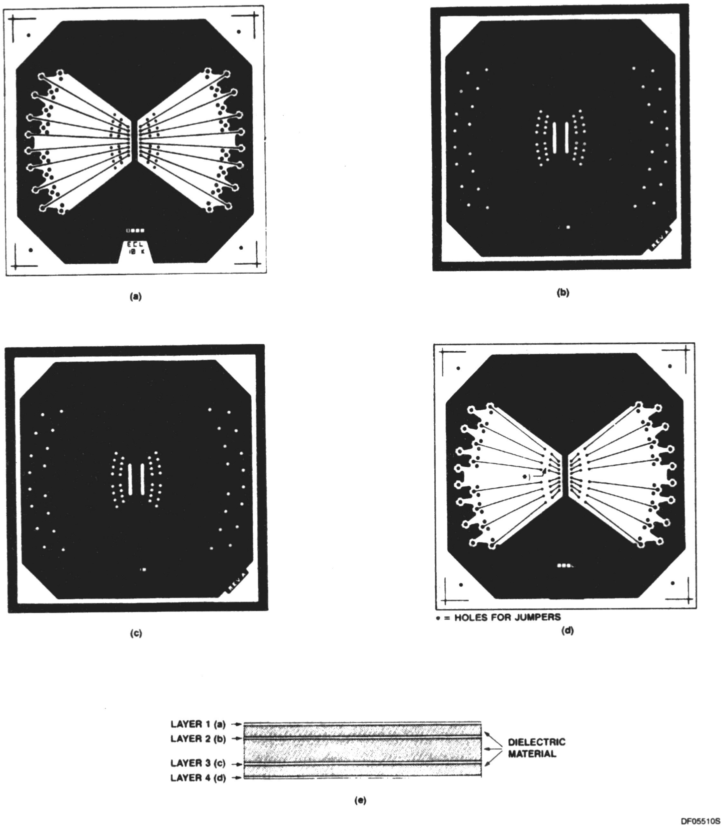
In systems in which other supply voltages are present (e.g., TTL at +5V), care should be taken not to connect the inputs to these voltages. Unfortunately, this is a frequent mishap when boards are tested or when maintenance is performed, through contact with a screwdriver or with the probes of a measurement device.

# Chapter 12
# Manual AC Testing

## TEST PHILOSOPHY

One of the primary concerns when testing ECL devices on a manual or bench setup is the accuracy and repeatability of measurements. The largest contributing factor in this accuracy and repeatability is the ability of the operator to precisely duplicate the amplitude and offset values of the pulse generator waveforms every time a new setup is made or when checking for equipment drift.

The procedure outlined in this section provides a method by which an operator can make these pulse generator waveform adjustments consistently identical between test sessions by eliminating as many variables as possible. Note: At this writing, a few digitally-controlled pulse generators do exist which can automatically provide very repeatable waveforms setups, but these are still quite expensive and are not widely available in the industry. This information is provided for users who are still equipped with the older, analog adjustment-type pulse generators.



(a) (b) (c) (d) (e)

**Figure 12.1. Sample AC Test Fixture Fabricated as a 4-Layer PC Board to Produce a 50Ω Environment. Top Traces of Layer 1 (a) Produce a 50Ω Micro-Stripline With Layer 2 (b), the Ground Plane, and are Used as Output Lines From the DUT. Layer 3 (c) is the Ground Plane for the Bottom Traces of Layer 4 (d) Which are Used as Inputs to the DUT (Notice the Holes for the Jumpers). In the Cross-Sectional View (e), the Space between Layers 2 and 3 is Non-Functional Except to Provide Rigidity to the Overall Fixture**

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## TEST FIXTURES

One major variable in manual AC testing is the test fixture. Every test engineer has his own idea of what the ideal test jig should be and it is difficult to say which method is better than another. The thing to keep in mind, however, is eliminating variables. Things like maintaining a continuous 50Ω environment to reduce reflections and therefore reduce waveform anomalies. This includes eliminating any unterminated stubs that are longer than about ¼″, since at ECL speeds a reflection can be generated with sufficient amplitude and phase characteristics to distort the wavefront and reduce measurement accuracy.

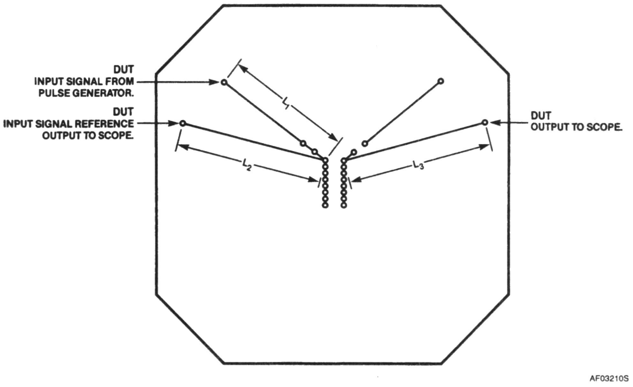
DUT
INPUT SIGNAL FROM PULSE GENERATOR.
DUT
INPUT SIGNAL REFERENCE OUTPUT TO SCOPE.
DUT
OUTPUT TO SCOPE.
$L_1$
$L_2$
$L_3$
AF03210S

**Figure 12.2. The Reference for the Input Signal is Taken at the DUT Pin After Length $L_1$. Since the Length of the Two Output Traces ($L_2$ and $L_3$) are Equal, Fixture Delay Cancels Out Leaving Only the Delay Through the DUT Package and Circuitry.**

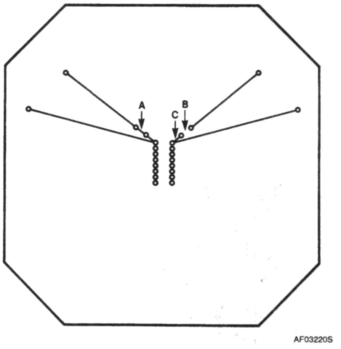

**Figure 12.3. Trace Used as an Input has Jumper (A) Installed but Trace Used as an Output has no Jumper (B), Leaving a Stub (C) of Less Than ¼″ Long.**

Another variable is jig delay or the delay that is added by the test fixture itself over and above that of the DUT (Device Under Test). A jig that cancels the effects of its own internal delay is quite simple to design and build but must be dedicated to one part type or group of part types having their input and output pins located in the same places. This makes fixturing rather expensive. However, certain compromises can be made with results that are completely satisfactory as far as cost effectiveness and test integrity are concerned.

Figure 12.1 shows an example of such a test fixture. The PC Board consists of four layers and incorporates micro-stripline techniques to achieve a consistent 50Ω environment. Jig delay cancellation is accomplished by returning the input signal reference to the sampling scope directly from the DUT input pin under test. Since the length of the PCB trace from the DUT input pin to the reference output connector is the same length as the trace from the DUT output pin to the measured output connector (see Figure 12.2), and the length of each coax cable from the jig to the sampling scope inputs are also equal, the jig delay is virtually transparent.

The only problem now is that there is an unterminated stub also connected to the DUT output pin which is two or three inches long, causing abberations on the output waveform which may or may not be visible on the scope display, depending on their amplitude and phase relationship to the actual output signal. These abberations may appear as a slight overshoot or undershoot or subtle roll-off of the rising or falling edge. The signal may be grossly distorted or no distortion may be apparent at all except that the measured propagation delay may vary from its true value by a few hundred picoseconds.

This stub could be removed by cutting the trace, but this would prevent the jig from being used for any other device whose input pin is in that particular location. Therefore, a compromise will need to be made. In Figure 12.3, the input traces have been designed so that a jumper may be installed, if needed, or removed, if not needed, for a given part. With the jumper removed (as in the case of an output pin), the unterminated stub is less than ¼″ long. Even at 100K ECL speeds this length does not create enough delay in the reflected signal to significantly distort the waveform, i.e., the roundtrip delay in the stub is considerably shorter than the transition time of the output signal.

With the jumper installed (as in the case of an input pin), the line is now terminated via the scope input, and although there is a short length (less than ¼″) of discontinuity in the 50Ω microstrip, it is not significantly different in impedance to cause anything but a minor distortion in the signal that reaches the DUT input pin. Since the input signal's reference to the scope is taken after the jumper, both the scope and the DUT will see the same signal and the DUT itself will tend to ignore these minor abberations at its input.

One other very important thing to remember is to use adequate power supply bypass and filtering capacitance. Because of the extremely fast edge rates associated with ECL, the instantaneous power factors during transition times are almost astronomical. These capacitors need to be placed as close to the DUT power and ground leads as physically possible. Bypass (or decoupling) capacitors should be selected for their integrity at ultrahigh frequencies, i.e., their dielectric absorp-

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**Table 1. Input Parameters for Manual AC Measurement of ECL Devices at Room Temperature (25°C)**

| PARAMETER | FAMILY | |
|---|---|---|
| | 10K | 100K |
| Amplitude | 800mV | 740mV |
| Offset | 310mV | 310mV |
| $t_R$, $t_F$ | 2ns | 700ps |
| Rep. Rate | 1MHz | 1MHz |
| Duty Cycle | 50% | 50% |

tion characteristics should be as low as possible.

### PULSE SOURCE ADJUSTMENTS

As mentioned earlier, the pulse generator waveform adjustments are probably the single biggest variable in ECL AC measurements and also the most difficult to control because of the inability of the operator to accurately repeat exactly the same setup at each test session. The procedure outlined below is suggested in order to eliminate as many of the human and mechanical variables as possible so as to reduce this art closer to the science that it should be.

### THE HUMAN FACTOR

In many of today's test labs, most of the sampling scopes that can be found which include built-in digital readout capability which can display the precise value of a signal's amplitude, transition times, and propagation delay, do not have a provision for digitizing its DC offset from ground. Because of the CRT display size, the graticule resolution, and parallax error, the human eye is incapable of consistently resolving the offset measurement to any better than 10 to 20mV. But a difference of even 2 or 3mV in the signal offset will alter the propagation delay measurement of an ECL device by several tens of picoseconds.

The repeatability of this offset measurement can be increased significantly with the use of a few other pieces of standard laboratory equipment, including a high-quality DVM (Digital Volt Meter) with resolution down to at least 1mV.

### DC OFFSET MEASUREMENT

To accurately measure the input signal's DC offset using a DVM, a few assumptions have to be made. First, it is assumed that a squarewave of amplitude A and exactly 50% duty cycle will generate a display of A/2 on a DVM that is set to measure DC volts, provided that there is no DC offset on the signal. Second, it is assumed that any DC offset added to the signal will merely add to the A/2 value. And third, it is assumed that the bandwidth of the DVM is wide enough to prevent significant roll-off of the squarewave signal which could introduce non-linearities into the measurement. This, however, will decrease the accuracy of the measurement but not the repeatability of it as long as the same DVM is used each time.

Keeping these assumptions in mind, the DC offset adjustment is made as follows:

1. Set the pulse generator output signal to a repetition rate of approximately 1MHz and exactly 50% duty cycle (a frequency counter should be used for this).
2. Using a sampling scope with a digital readout set to measure volts, adjust the signal amplitude of the pulse generator to 800mV (for 10K ECL).
3. Adjust $t_R$ and $t_F$ to 2ns, 20 to 80% (for 10K ECL).
4. Recheck steps 2 and 3 until satisfied with the adjustment accuracy (the amplitude and transition time adjustments might interact with each other).
5. Disconnect the 50Ω coax cable from the input of the sampling scope and connect it to the input of a DVM whose input is terminated in 50Ω. The 50Ω termination should be as physically close as possible to the DVM input connector. With the DC offset of the pulse generator set at 0V, i.e., the negative swing of the signal is at 0V and the positive swing is at 800mV, the DVM should read 800mV divided by 2, or 400mV.
6. The standard DC offset for a 10K ECL input signal is 310mV (see Figure 12.4). Therefore, the DC offset control of the pulse generator should be adjusted so that the DVM reads 710mV, which is one half the amplitude or 400mV plus 310mV of offset.

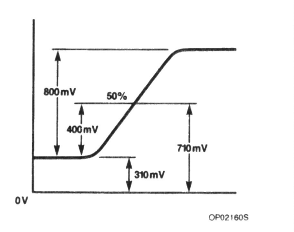

**Figure 12.4. 800mV/2 + 310mV = 710mV**

The input signal is now set up and may be connected to the test fixture but it should be checked periodically during a test session to make sure it has not drifted. Variations of this method will need to be developed to suit individual test requirements, but if the basic principle is followed, one of the major variables in ECL AC testing will be brought under control.

### AC MEASUREMENTS OVER TEMPERATURE RANGE

In 10K ECL devices, $V_{BB}$ drifts with temperature. The amount of drift varies between part types due to internal power dissipation and various other characteristics but is approximately equal to 1.1mV/°C. This affects the amount of DC offset to be used when measuring AC parameters at other than room temperature. For example: At room temperature (25°C), a part would normally require a 310mV offset. If the part were to be tested at 85°C, the offset would have to be increased by 1.1mV/°C times 60° (ΔT) or 66mV. A total offset of 376mV would be required. Using the formula from step 6 above, one-half the signal amplitude (400mV) plus 376mV of offset would produce a reading on the DVM of 776mV.

100K ECL devices are designed with internal compensation which virtually eliminates any drift due to operating temperature. Therefore, the same offset value may be used over the entire temperature range. However, the input signal conditions for 100K devices differ slightly from those used for 10K, but the same principles apply to either family and the same procedures and precautions should be used (refer to Table 1 for input pulse parameters).

Signetics

ECL Products

# Section 5
# Data Sheet Specification Guide

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# Data Sheet Specification Guide

## INTRODUCTION

Signetics' 10K and 100K ECL data sheets have been configured for quick usability. They are self-contained and should require minimum reference to other sections for further information.

## FEATURES AND DESCRIPTION

Features and/or Descriptions are shown on the left column starting at the top of the first page of the data sheets for quick reference.

## TYPICAL PROPAGATION DELAY AND SUPPLY CURRENT

The typical propagation delays listed at the top of the data sheets are the average between $t_{PLH}$ and $t_{PHL}$ for the most significant data path through the part.

The typical $I_{EE}$ current shown in that same specification block is the average current. It represents the total current through the package, not the current through the individual functions.

## LOGIC SYMBOLS

There are two types of logic symbols. The conventional one, "Logic Symbol," explicitly shows the internal logic (except for complex logic). The other is "Logic Symbol (IEEE/IEC)" as developed by the IEC and IEEE. The Logic Symbol by IEEE/IEC is described in

IEEE Standard
Graphic Symbols for Logic Functions
ANSI/IEEE Std 91-1984
(Review of ANSI/IEEE Std 91-1973
[ANSI Y32.14-1973])

and can be ordered through

IEEE Service Center
445 Hoes Lane
Piscataway, New Jersey 08854
Phone: 201-981-0060

## ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to all 10K and 100K devices, which should not be exceeded under the worst probable conditions.

These values are chosen by Signetics to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The user should design so that, initially and throughout life, no absolute maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices.

Absolute maximum ratings imply that any transient voltages, currents, and temperatures should not exceed the maximum ratings.

Input voltage, $V_{IN}$, should never be more negative than $V_{EE}$ at any time.

Output current should never exceed the maximum value in either HIGH level or LOW level state.

Family Specifications for Absolute Maximum Ratings for 10K and 100K families are shown in Tables 1 and 2, respectively.

## DC OPERATING CONDITIONS

The DC Operating Conditions table has a dual purpose. In one sense, it sets some environmental conditions (operating case temperature), and in another, it sets the conditions under which the limits set forth in the DC Electrical Characteristics table and AC Electrical Characteristics table will be met. Another way of looking at this table is to think of it not as a set of limits guaranteed by Signetics, but as the conditions Signetics uses to test the parts and guarantee that they will then meet the limits set forth in the DC and AC Electrical Characteristics tables.

10K ECL circuits are characterized with $V_{CC1}$ and $V_{CC2}$ at ground level and $V_{EE}$ at $-5.2V$. This arrangement gives the best noise immunity. $V_{EE}$ at $-5.2$ results in the best circuit speed. A more negative $V_{EE}$ will increase noise margins at the expense of increased power consumption. Other values of $V_{EE}$ are possible but DC and AC parameters will differ slightly from the specified values.

100K ECL circuits are characterized with $V_{CC1}$ and $V_{CC2}$ at ground level and $V_{EE}$ at $-4.2V$, $-4.5V$, and $-4.8V$. This arrangement also gives the best noise immunity. Other values of $V_{EE}$ are possible but DC and AC parameters will slightly differ from the specified values.

Family Specifications for DC Operating Conditions for 10K and 100K families are shown in Tables 3 and 4, respectively.

## DC CHARACTERISTICS

Family Specifications for DC Characteristics for 10K and 100K ECL families are shown in Tables 5 and 6, respectively. However, $I_{IH}$, $I_{IL}$, and $I_{EE}$ vary from device to device for 10K ECL families and similarly $I_{IH}$, $I_{IL}$, $I_{EE}$, $\Delta V_{OH}/\Delta V_{EE}$, $\Delta V_{OL}/\Delta V_{EE}$, $\Delta V_{BB}/\Delta V_{EE}$ vary from device to device for 100K ECL families.

It must be emphasized that the specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board.

Make sure that each output is terminated via a 50Ω resistor to $-2.0V$.

Although it is not recommended to use $V_{EE}$ other than $-5.2V$, if $V_{EE}$ other than $-5.2V$ is used, changes in $V_{OL}$, $V_{OH}$, and $V_{BB}$ level must be taken into consideration.

Although suggested test conditions are described for $V_{OH}$, $V_{OHT}$, $V_{OL}$, and $V_{OLT}$, refer to Section 3 Testing, DC testing for what to look for in considering output voltages in the worst cases.

The test values for DC Characteristics are defined and given in the Family Specifications for Transfer Characteristics for 10K and 100K ECL families and shown in Figures 1 and 2, respectively.

The conditions for the Transfer Characteristics for the 10K ECL families are $T_A = +25°C$, $V_{EE} = -5.2V$, $V_{CC1} = V_{CC2} = GND$; and 50Ω matched inputs and outputs.

The conditions for the Transfer Characteristics for the 100K ECL family are $T_A = 25°C$; $V_{EE} = -4.5V$, $V_{CC1} = V_{CC2} = GND$; and 50Ω matched inputs and outputs.

# Data Sheet Specification Guide

**Table 1. Family Specification for Absolute Maximum Ratings for 10K ECL Families**

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating case temperature range.)

| PARAMETER | | | 10K ECL | UNIT |
|---|---|---|---|---|
| $V_{EE}$ | Supply voltage | | −8.0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | | 0 to $V_{EE}$ | V |
| $I_O$ | Output source current | | −50 | mA |
| $T_S$ | Storage temperature | | −55 to +125 | °C |
| $T_J$ | Maximum junction temperature | Ceramic package | +165 | °C |
| | | Plastic package | +150 | °C |

**Table 2. Family Specification for Absolute Maximum Ratings for 100K ECL Families**

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating case temperature range.)

| PARAMETER | | 100K ECL | UNIT |
|---|---|---|---|
| $V_{EE}$ | Supply voltage (negative) | −7.0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | 0 to −6.0 | V |
| $I_O$ | Output source current | −55 | mA |
| $T_S$ | Storage temperature | −55 to +125 | °C |
| $T_J$ | Maximum junction temperature | +150 | °C |

# Data Sheet Specification Guide

**Table 3. DC Operating Conditions (Family Specification for 10K ECL Families)**

| PARAMETER | | | 10K ECL | | | |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Unit |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | | -5.2 | V |
| $V_{IH}$ | HIGH level input voltage | $T_A = -30°C$ | | | -890 | mV |
| | | $T_A = +25°C$ | | | -810 | mV |
| | | $T_A = +85°C$ | | | -700 | mV |
| $V_{IHT}$ | HIGH level input threshold voltage | $T_A = -30°C$ | -1205 | | | mV |
| | | $T_A = +25°C$ | -1105 | | | mV |
| | | $T_A = +85°C$ | -1035 | | | mV |
| $V_{ILT}$ | LOW level input threshold voltage | $T_A = -30°C$ | | | -1500 | mV |
| | | $T_A = +25°C$ | | | -1475 | mV |
| | | $T_A = +85°C$ | | | -1440 | mV |
| $V_{IL}$ | LOW level input voltage | $T_A = -30°C$ | -1890 | | | mV |
| | | $T_A = +25°C$ | -1850 | | | mV |
| | | $T_A = +85°C$ | -1825 | | | mV |
| $T_A$ | Ambient temperature | | -30 | +25 | +85 | °C |

**Table 4. DC Operating Conditions (Family Specification for 100K ECL Families)**

| PARAMETER | | | | 100K ECL | | | |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Unit |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | -4.2 | -4.5 | -4.8 | V |
| $V_{EE}$ | Supply voltage (negative) When operating with 10K ECL Family. | | | | | -5.7 | V |
| $V_{IH}$ | HIGH level input voltage | $V_{CC1} = V_{CC2} = GND$<br>$T_A = 0°C$ to $+85°C$ | $V_{EE} = -4.2V$ | -1150 | | -880 | mV |
| | | | $V_{EE} = -4.5V$ | -1165 | | | |
| | | | $V_{EE} = -4.8V$ | | | | |
| $V_{IHT}$ | HIGH level input threshold voltage | | $V_{EE} = -4.2V$ | -1150 | | | mV |
| | | | $V_{EE} = -4.5V$ | -1165 | | | mV |
| | | | $V_{EE} = -4.8V$ | | | | |
| $V_{ILT}$ | LOW level input threshold voltage | | $V_{EE} = -4.2V$ | | | -1475 | mV |
| | | | $V_{EE} = -4.5V$ | | | | |
| | | | $V_{EE} = -4.8V$ | | | -1490 | mV |
| $V_{IL}$ | LOW level input voltage | | $V_{EE} = -4.2V$ | -1810 | | -1475 | mV |
| | | | $V_{EE} = -4.5V$ | | | | |
| | | | $V_{EE} = -4.8V$ | | | -1490 | |
| $T_A$ | Ambient temperature | | | 0 | | +85 | °C |

**NOTE:**
When operating at other than specified voltages (-4.2V, -4.5V, -4.8V) DC & AC Characteristics may vary slightly from specified values.

### Table 5. DC Characteristics (Family Specification for 10K Families)

$V_{CC1} = V_{CC2} =$ GND, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$, Output loading with 50Ω to −2.0V ±0.010V, unless otherwise specified[1,3]

| PARAMETER | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | $T_A = -30°C$ | −1060 | | −890 | mV | |
| | | $T_A = +25°C$ | −960 | | −810 | mV | |
| | | $T_A = +85°C$ | −890 | | −700 | mV | |
| $V_{OHT}$ | HIGH level output threshold voltage | $T_A = -30°C$ | −1080 | | | mV | |
| | | $T_A = +25°C$ | −980 | | | mV | |
| | | $T_A = +85°C$ | −910 | | | mV | |
| $V_{OLT}$ | LOW level output threshold voltage | $T_A = -30°C$ | | | −1655 | mV | |
| | | $T_A = +25°C$ | | | −1630 | mV | |
| | | $T_A = +85°C$ | | | −1595 | mV | |
| | LOW level output voltage | $T_A = -30°C$ | −1890 | | −1675 | mV | |
| | | $T_A = +25°C$ | −1850 | | −1650 | mV | |
| | | $T_A = +85°C$ | −1825 | | −1615 | mV | |
| $I_{IH}$ | HIGH level input current | $T_A = -30°C$ | | | | μA | |
| | | $T_A = +25°C$ | | | | μA | |
| | | $T_A = +85°C$ | | | | μA | |
| | | $T_A = -30°C$ | | | | μA | |
| | | $T_A = +25°C$ | | | | μA | |
| | | $T_A = +85°C$ | | | | μA | |
| $I_{IL}$ | LOW level input current | $T_A = -30°C$ | | | | μA | |
| | | $T_A = +25°C$ | | | | μA | |
| | | $T_A = +85°C$ | | | | μA | |
| $-I_{EE}$ | $V_{EE}$ supply current | $T_A = -30°C$ | | | | mA | |
| | | $T_A = +25°C$ | | | | mA | |
| | | $T_A = +85°C$ | | | | mA | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | $T_A = +25°C$ | | 0.016 | | V/V | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | 0.250 | | V/V | |
| $\frac{\Delta V_{BB}}{\Delta V_{EE}}$ | Reference bias voltage compensation | | | 0.148 | | V/V | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 1.

**Table 6. DC Characteristics (Family Specification for 100K Families)**

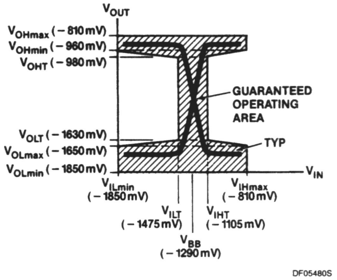
$V_{CC1} = V_{CC2} =$ GND, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$, $T_A = 0°C$ to $+85°C$, unless otherwise specified[1, 3]

| PARAMETER | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | $V_{EE} = -4.2V$ | -1025 | | -870 | mV | |
| | | $V_{EE} = -4.5V$ | -1025 | -955 | -880 | mV | |
| | | $V_{EE} = -4.8V$ | -1035 | | -880 | mV | |
| $V_{OHT}$ | HIGH level output threshold voltage | $V_{EE} = -4.2V$ | -1035 | | | mV | |
| | | $V_{EE} = -4.5V$ | -1035 | | | mV | |
| | | $V_{EE} = -4.8V$ | -1045 | | | mV | |
| $V_{OLT}$ | LOW level output threshold voltage | $V_{EE} = -4.2V$ | | | -1590 | mV | |
| | | $V_{EE} = -4.5V$ | | | -1610 | mV | |
| | | $V_{EE} = -4.8V$ | | | -1610 | mV | |
| $V_{OL}$ | LOW level output voltage | $V_{EE} = -4.2V$ | -1810 | | -1605 | mV | |
| | | $V_{EE} = -4.5V$ | -1810 | -1705 | -1620 | mV | |
| | | $V_{EE} = -4.8V$ | -1830 | | -1620 | mV | |
| $I_{IH}$ | HIGH level input current | | | | | μA | |
| | | | | | | μA | |
| $I_{IL}$ | LOW level input current | | | | | μA | |
| $-I_{EE}$ | $V_{EE}$ supply current | | | | | μA | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 2.

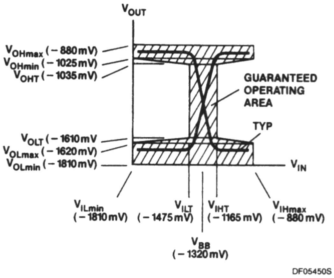
# Data Sheet Specification Guide


$V_{OUT}$
$V_{OHmax}$ (−810mV)
$V_{OHmin}$ (−960mV)
$V_{OHT}$ (−980mV)
GUARANTEED OPERATING AREA
$V_{OLT}$ (−1630mV)
$V_{OLmax}$ (−1650mV)
$V_{OLmin}$ (−1850mV)
TYP
$V_{IN}$
$V_{ILmin}$ (−1850mV)
$V_{IHmax}$ (−810mV)
$V_{ILT}$ (−1475mV)
$V_{IHT}$ (−1105mV)
$V_{BB}$ (−1290mV)
DF05480S

**NOTES:**

$V_{IHmax}$ – Maximum HIGH level input voltage (the most positive $V_{IH}$).
$V_{IHT}$ – HIGH level input threshold voltage.
$V_{ILT}$ – LOW level input threshold voltage.
$V_{ILmin}$ – Minimum LOW level input voltage (the most negative $V_{IL}$).
$V_{OHmax}$ – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition.
$V_{OHmin}$ – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition.
$V_{OHT}$ – HIGH level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLT}$ – LOW level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLmax}$ – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions.
$V_{OLmin}$ – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions.
$V_{BB}$ – Reference bias voltage (the internally generated reference voltage which is used to set the input and output threshold level).

**Figure 1. Transfer Characteristics Family Specification for 10K ECL**


$V_{OUT}$
$V_{OHmax}$ (−880mV)
$V_{OHmin}$ (−1025mV)
$V_{OHT}$ (−1035mV)
GUARANTEED OPERATING AREA
TYP
$V_{OLT}$ (−1610mV
$V_{OLmax}$ (−1620mV)
$V_{OLmin}$ (−1810mV)
$V_{IN}$
$V_{ILmin}$ (−1810mV)
$V_{ILT}$ (−1475mV)
$V_{IHT}$ (−1165mV)
$V_{IHmax}$ (−880mV)
$V_{BB}$ (−1320mV)
DF05450S

**NOTES:**

$V_{IHmax}$ – Maximum HIGH level input voltage (the most positive $V_{IH}$).
$V_{IHT}$ – HIGH level input threshold voltage (also $V_{IHmin}$).
$V_{ILT}$ – LOW level input threshold voltage (also $V_{ILmax}$).
$V_{ILmin}$ – Minimum LOW level input voltage (the most negative $V_{IL}$).
$V_{OHmax}$ – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition.
$V_{OHmin}$ – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition.
$V_{OHT}$ – HIGH level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLT}$ – LOW level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLmax}$ – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions.
$V_{OLmin}$ – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions.
$V_{BB}$ – Reference Bias voltage. The internally generated reference voltage which is used to set the input and output threshold level.

**Figure 2. Transfer Characteristics Family Specification for 100K ECL**

# Data Sheet Specification Guide

## AC CHARACTERISTICS

Since AC Characteristics vary from device to device there is no family specifications as such.

It must be emphasized that the specified limits shown in the AC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. AC Characteristics may be tested either in non-offset bias condition or in offset bias condition. For 10K ECL, the non-offset bias condition is $V_{CC1} = V_{CC2} = 0V$ and $V_{EE} = -5.2V \pm 0.010V$ and the offset condition is $V_{CC1} = V_{CC2} = +2V \pm 0.010V$ and $V_{EE} = -3.2V \pm 0.010V$. For 100K ECL, the non-offset bias condition is $V_{CC1} = V_{CC2} = 0V$, and $V_{EE} = -4.2V$ to $-4.8V$ ($\pm 0.010V$), and the offset condition is $V_{CC1} = V_{CC2} = +2V \pm 0.010V$ and $V_{EE} = -2.2V$ to $-2.8V$ ($\pm 0.010V$). The offset bias condition is for bench-type tester to accommodate the oscilloscope ground configuration. Of course, the specified limits remain the same for the non-offset and the offset condition.

## AC WAVEFORMS

AC test conditions for 10K and 100K ECL are described in AC Waveforms, Test Circuit, and Input Pulse Definition in each individual data sheet.

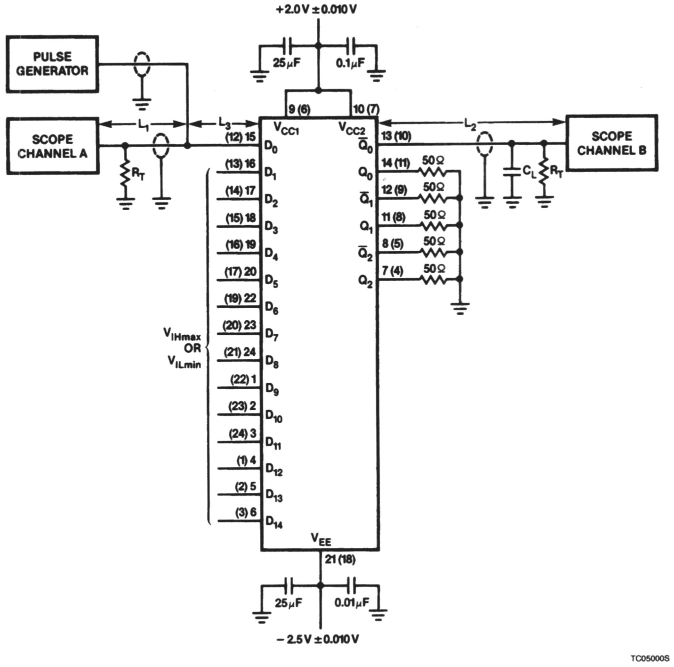
There is no Family Specification for AC Waveforms. However, Typical AC Waveforms describing the Propagation Delay ($t_{PLH}$, $t_{PHL}$), Transition Time ($t_{TLH}$, $t_{THL}$), Setup Time, Hold Time, and Release Time are shown for your reference. Since AC Waveforms vary from device to device, refer to each individual data sheet.

## AC TEST CIRCUIT

The AC test circuit shows how to arrange the test circuit for each device with pulse generator, sampling scope, and power supplies. A simplified arrangement for 10K and 100K families are shown in Figure 7. However, since AC test circuits vary from device to device, refer to each individual data sheet.

Since AC Characteristics are difficult to test, a whole section is devoted to Testing including a whole section describing the bench-type testing for AC Characteristics (Refer to Section 3 Testing, AC Testing).

## AC TEST CIRCUIT FOR 10K AND 100K ECL



**NOTES:**

1. $V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1μF and 25μF from GND to $V_{CC}$, 0.01μF from GND to $V_{EE}$(0.01 and 0.1uF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than ¼ inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the logic function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin and the junction of the cable from the Pulse Generator and the cable to the scope, should not exceed ¼ inch (6mm).
6. $R_T = 50\Omega$ terminator internal to scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than ¼ inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance $\leqslant 3pF$.
9. Any unterminated stubs connected anywhere along the transmission line between the pulse generator and the DUT or between the DUT and the scope should not exceed ¼ inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.

Figure 3

# Data Sheet Specification Guide

## INPUT PULSE DEFINITION

The Input Pulse definition defines the input pulse requirements such as pulse amplitude, repetition rate, pulse width, and Transition Time ($t_{TLH}$, $t_{THL}$) together with the input pulse waveform.

The Family Specification for 10K and 100K for Input Pulse Definition and Requirement is as follows:

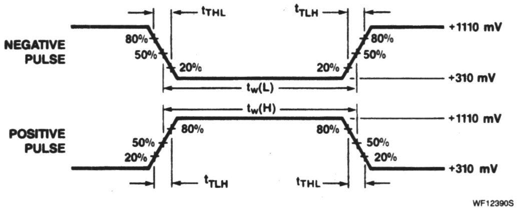


Figure 4. Input Pulse Definition

Table 7. Input Pulse Requirements for 10K and 100K Families

| INPUT PULSE REQUIREMENTS<br>$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$, $V_T = GND$ (0V) for 10K ECL<br>$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -2.5V \pm 0.010V$, $V_T = GND$ (0V) for 100K ECL | | | | | |
|---|---|---|---|---|---|
| FAMILY | AMPLITUDE | REP RATE | PULSE WIDTH | $t_{TLH}$ | $t_{THL}$ |
| 10K ECL | 800 mVp-p | 1MHz | 500ns | 2.0 ±0.2ns | 2.0 ±0.2ns |
| 100K ECL | 740 mVp-p | 1MHz | 500ns | 0.7 ±0.1ns | 0.7 ±0.1ns |

# Data Sheet Specification Guide

## DC SYMBOLS AND DEFINITIONS

### Voltages

All voltages are referenced to $V_{CC}$ ($V_{CC1}$ and $V_{CC2}$) which is usually ground (common) and the most positive potential in an ECL system.

| | |
|---|---|
| $V_{BB}$ | **Reference Bias voltage:** The internally-generated reference voltage which is used to set the input and output threshold level. |
| $V_{BBmax}$ | **Maximum Reference Bias voltage** |
| $V_{BBmin}$ | **Minimum Reference Bias voltage** |
| $V_{BIN}$ (TTL) | **Input breakdown voltage:** Reverse breakdown voltage of the input diodes of a TTL/ECL Translator with 1.0 mA flowing into the input pin. |
| $V_{BE}$ | **Base to Emitter voltage** |
| $V_{CB}$ | **Collector to Base voltage** |
| $V_{CC}$ | **Circuit Ground:** This is the most positive potential in the ECL system and it is used as the reference for other voltages and is usually ground except for the TTL/ECL or ECL/TTL system such as translator and interface circuits. |
| $V_{CC1}$ | **Circuit Ground:** Usually ground in the ECL system (Output reference). |
| $V_{CC2}$ | **Circuit Ground:** Usually ground in the ECL system (Internal circuit reference). |
| $V_{CS}$ | **Current source voltage:** An internally-generated reference potential in an ECL system. |
| $V_{EE}$ | **Power supply voltage:** This potential is the ECL system power supply voltage and it is the most negative potential in the ECL system. |
| $V_F$ (TTL) | **Forward voltage:** Input voltage for measuring $I_F$ on TTL/ECL translators. |
| $V_{IH}$ | **HIGH level input voltage:** An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables. A logical "1" (nominal value). |
| $V_{IHmax}$ | **Maximum HIGH level input voltage:** The most positive $V_{IH}$ |
| $V_{IHH}$ | $V_{IHmax}$ + 1.0V ($V_{IHmax}$ shifted positive one volt for CMR test) |
| $V_{IHL}$ | $V_{IHmax}$ − 1.0V ($V_{IHmax}$ shifted negative one volt for CMR test) |
| $V_{IHT}$ | **HIGH level input threshold voltage:** The guaranteed HIGH level input threshold voltage |
| $V_{IHT}''$ (TTL) | **Hysteresis Mode HIGH level input threshold voltage:** $V_{IHT}$ for HIGH to LOW level transition in Hysteresis mode. |
| $V_{IHT}'''$ (TTL) | **Hysteresis Mode HIGH level input threshold voltage:** $V_{IHT}$ for LOW to HIGH level transition in Hysteresis mode. |
| $V_{IK}$ | **Input clamp voltage:** The input voltage level across the input clamping diode in a region of relatively low differential resistance that serves to limit the input voltage swing. |
| $V_{IKmax}$ | **Maximum input clamp diode voltage:** The most negative voltage at an input when the specified current is forced out of that input terminal. This parameter guarantees the integrity of the input diode intended to clamp negative ringing at the input terminal. |
| $V_{IL}$ | **LOW level input voltage:** An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables. A logical "0" (nominal level). |
| $V_{ILT}$ | **LOW level input threshold voltage:** The guaranteed LOW level input threshold voltage. |
| $V_{ILT}''$ (TTL) | **Hysteresis Mode LOW level input threshold voltage:** $V_{IHT}$ for HIGH to LOW level transition in Hysteresis mode. |
| $V_{ILT}'''$ (TTL) | **Hysteresis Mode LOW level input threshold voltage:** $V_{IHT}$ for LOW to HIGH level transition in Hysteresis mode. |
| $V_{ILmin}$ | **Minimum LOW level input voltage:** The most negative $V_{IL}$. |
| $V_{ILH}$ | $V_{ILmin}$ +1.0V ($V_{ILmin}$ shifted positive one volt for CMR tests.) |
| $V_{ILL}$ | $V_{ILmin}$ −1.0V ($V_{ILmin}$ shifted negative one volt for CMR tests.) |
| $V_{IN}$ | **Input Voltage** |
| $V_{NH}$ | **HIGH level Noise Margin:** Noise margin between the output HIGH level of a driving circuit and the input HIGH threshold level of its driven load. A conservative value for $V_{NH}$ is the difference between $V_{OHT}$ and $V_{IHmin}$. |
| $V_{NL}$ | **LOW level Noise Margin:** Noise margin between the output LOW level of a driving circuit and the input LOW threshold level of its drive load. A conservative value for $V_{NL}$ is the difference between $V_{ILmax}$ and $V_{OLT}$. |
| $V_{OH}$ | **HIGH level output voltage:** The voltage at an output terminal with input conditions applied that, according to the product specification, will establish a HIGH level at the output (nominal output "1" state). |
| $V_{OHmax}$ | **Maximum HIGH level output voltage:** The most positive $V_{OH}$ under the specified input and loading conditions. |
| $V_{OHmin}$ | **Minimum HIGH level output voltage:** The most negative $V_{OH}$ under the specified input and loading condition. |
| $V_{OHT}$ | **HIGH level output threshold voltage:** The guaranteed HIGH level threshold output voltage with the inputs set to their respective threshold levels, one at a time. |
| $V_{OL}$ | **LOW level output voltage:** The voltage at an output terminal with input conditions applied that, according to the product specification, will establish a LOW level at the output (nominal output "0" state). |
| $V_{OLmax}$ | **Maximum LOW level output voltage:** The most positive $V_{OL}$ under the specified input and loading conditions. |
| $V_{OLmin}$ | **Minimum LOW level output voltage:** The most negative $V_{OL}$ under the specified input and loading conditions. |
| $V_{OLT}$ | **LOW level output threshold voltage:** The guaranteed LOW level output threshold voltage with the inputs set to their respective threshold levels, one at a time. |

# Data Sheet Specification Guide

## DC SYMBOLS AND DEFINITIONS (Continued)

| | |
|---|---|
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | **LOW level output voltage compensation:** The ratio of the change in the LOW level output voltage to the change in the supply voltage. |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | **HIGH level output voltage compensation:** The ratio of the change in the HIGH level output voltage to the change in the supply voltage. |
| $\frac{\Delta V_{BB}}{\Delta V_{EE}}$ | **Reference Bias voltage compensation:** The ratio of the change in the input reference voltage to the change in the supply voltage. |
| $V_{OLS1}$ (TTL) | LOW level output voltage on 10K ECL/TTL translator with all inputs at $V_{EE}$ voltage to check indeterminate input level. |
| $V_{OLS2}$ (TTL) | LOW level output voltage on 10K ECL/TTL translator with all inputs open to check indeterminate input level. |
| $V_{OUT}$ | **Output Voltage** |
| $V_R$ (TTL) | **Reverse input voltage:** Input voltage for measuring $I_R$ on TTL/ECL Translator. |
| $V_T$ | **Line load-resistor terminating voltage,** positive or negative. |
| GND | **Ground (Common):** The reference point from which all voltages in the system are measured. In a TTL/ECL or ECL/TTL translator, or other interface circuits, it is the common point to which all other voltage supplies are referenced. |

### Currents

Positive current is defined as conventional current (Hole) flow into a device. Negative current is defined as conventional current flow out of a device.

| | |
|---|---|
| $I_{CC}$ | **Supply current:** The current flowing into the $V_{CC}$ supply terminal of the circuit with specified input conditions and open outputs. Input conditions are chosen to guarantee worst-case operations unless specified. Current out of a terminal is given as a negative value. |
| $I_{CBO}$ | **Input (Collector to Base) leakage current:** Leakage current flowing out of an input on devices without pull-down resistors when test voltage is applied. |
| $I_{CCH}$ (TTL) | **Supply current, outputs HIGH:** The current into the $V_{CC}$ supply terminal of an integrated circuit when all (or a specified number) of the outputs are at the HIGH level. Current out of a terminal is given as a negative value. |
| $I_{CCL}$ (TTL) | **Supply current, outputs LOW:** The current into the $V_{CC}$ supply terminal of an integrated circuit when all (or a specified number) of the outputs are at the LOW level. Current out of a terminal is given as a negative value. |
| $I_{EE}$ | **Power supply current:** The current required by each device from the $V_{EE}$ supply. This value represents only the internal current required by the specified device and does not include the current required for loads or termination. |
| $I_F$ (TTL) | **Input forward current:** The forward conduction current out of the input diode of a TTL/ECL Translator with the input voltage at a LOW logic level ($V_F$). |
| $I_I$ (TTL) | **Input leakage current:** The current flowing into an input when the maximum allowed voltage is applied to the input. This parameter guarantees the minimum breakdown voltage for the input. |
| $I_{IH}$ | **HIGH level input current:** The current flowing into an input when a specified HIGH level voltage is applied to the input. Current out of the input is given as a negative value. |
| $I_{IHmax}$ | **Maximum HIGH level input current:** The most positive $I_{IH}$. |
| $I_{IHmin}$ | **Minimum HIGH level input current:** The most negative $I_{IH}$. |
| $I_{IL}$ | **LOW level input current:** The current flowing into an input when a LOW level input voltage is applied to that input. In ECL devices, this is a measurement of the current flowing into the input pull-down resistor. |
| $I_{ILmax}$ | **Maximum LOW level input current:** The most positive $I_{IL}$. |
| $I_{ILmin}$ | **Minimum LOW level input current:** The most negative $I_{IL}$. |
| $I_{OH}$ | **HIGH level output current:** The current into an output with input conditions applied that, according to the product specification, will establish a HIGH level at the output. Current out of the output is given as a negative value. |
| $I_{OHT}$ | **HIGH level output threshold current:** The guaranteed maximum HIGH level output current of an ECL Bus Driver with current switch mode outputs with the inputs at their respective threshold levels, one at a time. |
| $I_{OL}$ | **LOW level output current:** The current into an output with input conditions applied that, according to the product specification, will establish a LOW level at the output. Current out of the output is given as a negative value. |
| $I_{OLT}$ | **LOW level output threshold current:** The guaranteed maximum LOW level output current of an ECL Bus Driver with current switch mode outputs with the inputs at their respective threshold levels, one at a time. |
| $I_O$ | **Output source current (Absolute Maximum Rating):** The maximum current that may flow out of an output without causing permanent damage to the device. This is a function of the external Load Resistance and the Terminating Voltage ($V_T$) to which it is referenced and logic state of the output ($V_{OHmax}$ is worst-case). |
| $I_{OS}$ | **Short circuit output current:** The current out of an output of an ECL/TTL translator when the output is short-circuited to ground with input conditions applied to establish a HIGH state output logic level. Only one output should be shorted to ground at a time. |
| $I_R$ (TTL) | **Reverse input current:** Reverse (leakage) current flowing into the input diodes of a TTL/ECL Translator when the input is at a HIGH logic level ($V_R$). |
| $I_T$ | **Line Terminating (Load) current** |

# Data Sheet Specification Guide

## AC SYMBOLS AND DEFINITIONS

| | |
|---|---|
| $f_{MAX}$ | **Maximum clock frequency:** The maximum input frequency at a clock input for which predictable performance is guaranteed. Above this frequency the device may cease to function. (Specified as a limit.) |
| $t_h$ | **Hold time:** The time interval during which a signal must be retained at a specified input terminal after an active transition occurs at another specified input terminal.<br>**NOTES:**<br>1. The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operated. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.<br>2. The hold time may have a negative value, in which case the minimum limit defines the longest interval (between the release of the signal and active transition) for which correct operation of the digital circuit is guaranteed. |
| $t_{PD}$ | **Propagation delay time** |
| $t_{PLH}$ | **Propagation delay time, LOW to HIGH:** The time between the specified reference points on the input and output waveforms with the output changing from the defined LOW level to the defined HIGH level. |
| $t_{PHL}$ | **Propagation delay time, HIGH to LOW:** The time between the specified reference points on the input and output waveforms with the output changing from the defined HIGH level to the defined LOW level. |
| $t_r$ | **Release time:** The interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which the master set or reset must be released (inactive) to ensure valid data is recognized. |
| $t_s$ | **Setup time:** The time interval prior to an active transition applied to a specified input terminal that a signal at another specified input terminal must be applied in order to achieve the desired operation of the device.<br>**NOTES:**<br>1. The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operated. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.<br>2. The setup time may have a negative value, in which case the minimum limit defines the longest interval (between the release of the signal and active transition) for which correct operation of the digital circuit is guaranteed. |
| $t_{TLH}$ | **Transition time, LOW to HIGH:** The time between two specified reference points on a waveform, normally 20% and 80% points, that is changing from LOW to HIGH. |
| $t_{THL}$ | **Transition time, HIGH to LOW:** The time between two specified reference points on a waveform, normally 80% and 20% points, that is changing from HIGH to LOW. |
| $t_W$ | **Pulse width:** The time between the specified reference points on the leading and trailing edges of a pulse. |

## ANALOG SYMBOLS AND DEFINITIONS

| | |
|---|---|
| CMR | **Common-Mode Rejection:** Ratio of common-mode voltage to common-mode error voltage where common-mode voltage is defined as the voltage above or below the reference level at each input when both inputs are at the same potential and common-mode error voltage is defined as the resultant error voltage measured at the input. |
| dBm | Power level relative to 1mW. dBm (Power level) = $10 \log_{10} \frac{\text{power level (mW)}}{1\text{mW}}$. |
| $f_I$ | **Input frequency** |
| $f_{Imax}$ | **Maximum input frequency** |
| $f_{Imin}$ | **Minimum input frequency** |
| SR | **Slew rate:** Maximum rate of change of output voltage for a large step change. |
| $V_{CM}$ | **Common-mode voltage:** The voltage above or below ground at each input when both inputs are at the same voltage. |
| $V_{ID}$ | **Differential input voltage:** The voltage applied between two input terminals of a circuit. |
| $V_L$ | **Load voltage** |

## THERMAL SYMBOLS AND DEFINITIONS

| | |
|---|---|
| $\theta$ | **Thermal resistance** |
| $\theta_{JC}$ | **Thermal resistance, junction to case** |
| $\theta_{JA}$ | **Thermal resistance, junction to ambient** |
| $t_C$ | **Case temperature:** Case temperature of an integrated circuit package. |
| $t_J$ | **Junction temperature (absolute maximum rating):** The absolute maximum allowable temperature at the junction of any P and N type material on the silicon chip. Temperatures exceeding this value will cause a permanent migration of the materials and therefore damage the junction. |
| $t_S$ | **Storage temperature (absolute maximum rating):** Maximum temperature at which device may be stored without damage or performance degradation. |

# Section 6
# 10K Series Data Sheets

**ECL Products**

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**Signetics**

# 10100
## Gate

**Quad 2-Input NOR Gate With Strobe**
***Product Specification***

**ECL Products**

## DESCRIPTION

The 10100 is a Quad 2-Input NOR Gate with another input common to all gates. All unused inputs can be left open due to integrated pull-down resistors, which avoid the need for a supply voltage.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (−$I_{EE}$) |
|---|---|---|
| 10100 | 2.0ns | 21mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} = GND$; $V_{EE} = -5.2V$<br>$T_A = -30°C$ to $+85°C$ |
|---|---|
| Plastic DIP | 10100N |
| Ceramic DIP | 10100F |

## PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_0 - D_7$ | Data Inputs |
| $S_t$ | Strobe Input |
| $\overline{Q}_0 - \overline{Q}_3$ | Data Outputs |

## PIN CONFIGURATION

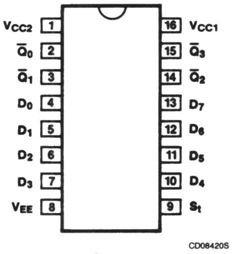

VCC2 1
Q̄0 2
Q̄1 3
D0 4
D1 5
D2 6
D3 7
VEE 8
16 VCC1
15 Q̄3
14 Q̄2
13 D7
12 D6
11 D5
10 D4
9 St
CD08420S

Figure 1

## LOGIC SYMBOL

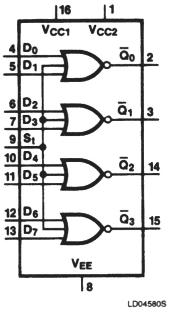

16
1
VCC1
VCC2
4 D0
5 D1
Q̄0 2
6 D2
7 D3
9 St
Q̄1 3
10 D4
11 D5
Q̄2 14
12 D6
13 D7
Q̄3 15
VEE
8
LD04580S

Figure 2

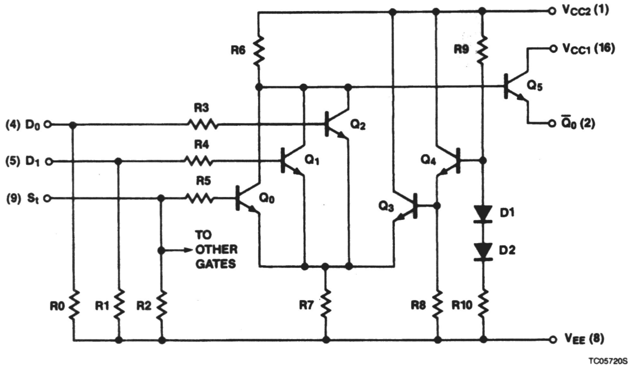
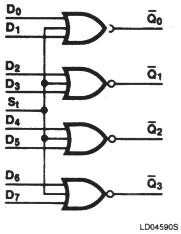

V_CC2 (1)
R6
R9
V_CC1 (16)
Q5
(4) D0
R3
Q2
Q̄0 (2)
(5) D1
R4
Q1
Q4
(9) St
R5
Q0
Q3
D1
TO OTHER GATES
D2
R0
R1
R2
R7
R8
R10
V_EE (8)
TC05720S

Figure 3. Circuit Diagram (One Gate)


D0
D1
Q̄0
D2
D3
Q̄1
St
D4
D5
Q̄2
D6
D7
Q̄3
LD04590S

$Q_0 = \overline{D_0 + D_1 + S_t}$
$Q_1 = \overline{D_2 + D_3 + S_t}$
$Q_2 = \overline{D_4 + D_5 + S_t}$
$Q_3 = \overline{D_6 + D_7 + S_t}$

**Positive Logic:** HIGH state = 1
LOW state = 0

Figure 4. Logic Diagram

## ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | | 10K ECL | UNIT |
|---|---|---|---|---|
| $V_{EE}$ | Supply voltage | | −8.0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | | 0 to $V_{EE}$ | V |
| $I_O$ | Output current | | −50 | mA |
| $T_S$ | Storage temperature | | −55 to +150 | °C |
| $T_J$ | Maximum junction temperature | Ceramic package | +165 | °C |
| | | Plastic package | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | 10K ECL | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | −5.2 | | V |
| $V_{IH}$ | HIGH level input voltage | $T_A = -30°C$ | | | −890 | mV |
| | | $T_A = +25°C$ | | | −810 | mV |
| | | $T_A = +85°C$ | | | −700 | mV |
| $V_{IHT}$ | HIGH level input threshold voltage | $T_A = -30°C$ | −1205 | | | mV |
| | | $T_A = +25°C$ | −1105 | | | mV |
| | | $T_A = +85°C$ | −1035 | | | mV |
| $V_{ILT}$ | LOW level input threshold voltage | $T_A = -30°C$ | | | −1500 | mV |
| | | $T_A = +25°C$ | | | −1475 | mV |
| | | $T_A = +85°C$ | | | −1440 | mV |
| $V_{IL}$ | LOW level input voltage | $T_A = -30°C$ | −1890 | | | mV |
| | | $T_A = +25°C$ | −1850 | | | mV |
| | | $T_A = +85°C$ | −1825 | | | mV |
| $T_A$ | Operating ambient temperature | | −30 | +25 | +85 | °C |

**NOTE:**
When operating at $V_{EE}$ other than specified voltage (−5.2V), the DC and AC Characteristics will vary slightly from specified values.
(See table of DC Electrical Characteristics)

## DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2} = \text{GND}$, $V_{EE} = -5.2\text{V} \pm 0.010\text{V}$, $T_A = -30°\text{C}$ to $+85°\text{C}$, output loading with $50\Omega$ to $-2.0\text{V} \pm 0.010\text{V}$ unless otherwise specified[1,3]

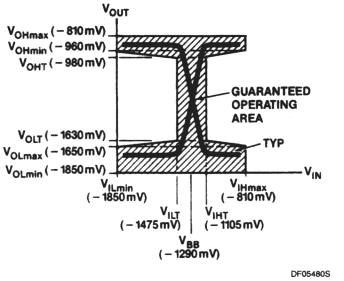
| PARAMETER | | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | | $T_A = -30°\text{C}$ | -1060 | | -890 | mV | Apply $V_{ILmin}$ to all inputs. |
| | | | $T_A = +25°\text{C}$ | -960 | | -810 | mV | |
| | | | $T_A = +85°\text{C}$ | -890 | | -700 | mV | |
| $V_{OHT}$ | HIGH level output threshold voltage | | $T_A = -30°\text{C}$ | -1080 | | | mV | Apply $V_{ILT}$ to $S_t$ input with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25°\text{C}$ | -980 | | | mV | |
| | | | $T_A = +85°\text{C}$ | -910 | | | mV | |
| $V_{OLT}$ | LOW level output threshold voltage | | $T_A = -30°\text{C}$ | | | -1655 | mV | Apply $V_{IHT}$ to each input, one at a time, with $V_{ILmin}$ applied to all oth er inputs. |
| | | | $T_A = +25°\text{C}$ | | | -1630 | mV | |
| | | | $T_A = +85°\text{C}$ | | | -1595 | mV | |
| $V_{OL}$ | LOW level output voltage | | $T_A = -30°\text{C}$ | -1890 | | -1675 | mV | Apply $V_{IHmax}$ to all inputs. |
| | | | $T_A = +25°\text{C}$ | -1850 | | -1650 | mV | |
| | | | $T_A = +85°\text{C}$ | -1825 | | -1615 | mV | |
| $I_{IH}$ | HIGH level input current | $D_n$ inputs | $T_A = -30°\text{C}$ | | | 390 | µA | Apply $V_{IHmax}$ to each input under test, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25°\text{C}$ | | | 245 | µA | |
| | | | $T_A = +85°\text{C}$ | | | 245 | µA | |
| | | $S_t$ input | $T_A = -30°\text{C}$ | | | 750 | µA | Apply $V_{IHmax}$ to $S_t$ input with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25°\text{C}$ | | | 470 | µA | |
| | | | $T_A = +85°\text{C}$ | | | 470 | µA | |
| $I_{IL}$ | LOW level input current | | $T_A = -30°\text{C}$ | 0.5 | | | µA | Apply $V_{ILmin}$ to each input under test, one at a time, with $V_{IHmax}$ applied to all other inputs. |
| | | | $T_A = +25°\text{C}$ | 0.5 | | | µA | |
| | | | $T_A = +85°\text{C}$ | 0.3 | | | µA | |
| $-I_{EE}$ | $V_{EE}$ supply current | | $T_A = -30°\text{C}$ | | | 29 | mA | |
| | | | $T_A = +25°\text{C}$ | | 21 | 26 | mA | |
| | | | $T_A = +85°\text{C}$ | | | 29 | mA | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | | $T_A = +25°\text{C}$ | | 0.016 | | V/V | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | | 0.250 | | V/V | |
| $\frac{\Delta V_{BB}}{\Delta V_{EE}}$ | Reference bias voltage compensation | | | | 0.148 | | V/V | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst-case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 5.

## Gate

## 10100



**NOTES:**

$V_{IHmax}$ – Maximum HIGH level input voltage (the most positive $V_{IH}$).
$V_{IHT}$ – HIGH level input threshold voltage.
$V_{ILT}$ – LOW level input threshold voltage.
$V_{ILmin}$ – Minimum LOW level input voltage (the most negative $V_{IL}$).
$V_{OHmax}$ – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition.
$V_{OHmin}$ – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition.
$V_{OHT}$ – HIGH level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLT}$ – LOW level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLmax}$ – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions.
$V_{OLmin}$ – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions.
$V_{BB}$ – Reference bias voltage (the internally generated reference voltage which is used to set the input and output threshold level).

Figure 5. Transfer Characteristics

## AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$

| PARAMETER | $T_A = -30°C$ | | $T_A = +25°C$ | | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Typ | Max | Min | Max | | |
| $t_{PLH}$ Propagation delay | 1.0 | 3.1 | 1.0 | 2.0 | 2.9 | 1.0 | 3.3 | ns | Figs. 6, 7, 8 |
| $t_{PHL}$ $D_n$ to $\overline{Q}_n$ | 1.0 | 3.1 | 1.0 | 2.0 | 2.9 | 1.0 | 3.3 | ns | |
| $t_{TLH}$ Transition time | 1.1 | 3.6 | 1.1 | 2.0 | 3.3 | 1.1 | 3.7 | ns | Figs. 6, 7, 8 |
| $t_{THL}$ 20% to 80%, 80% to 20% | 1.1 | 3.6 | 1.1 | 2.0 | 3.3 | 1.1 | 3.7 | ns | |

## AC WAVEFORMS

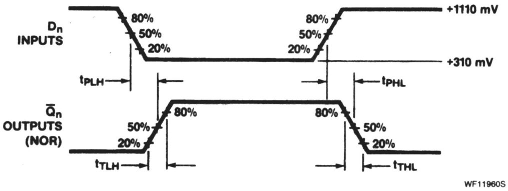
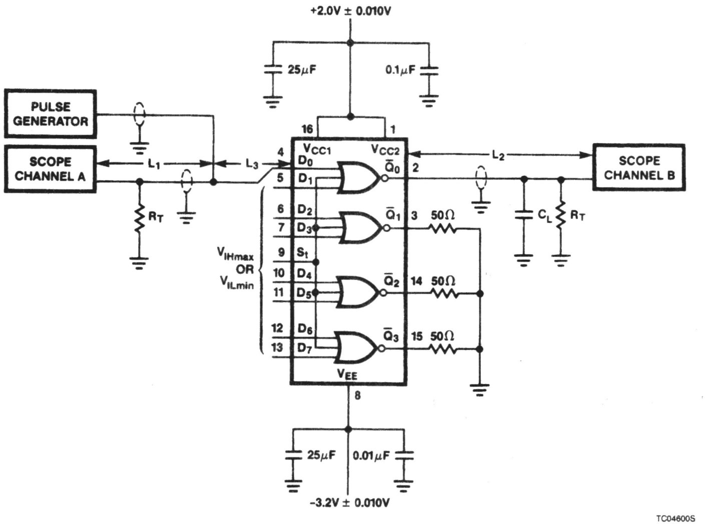


Figure 6. Propagation Delay and Transition Times

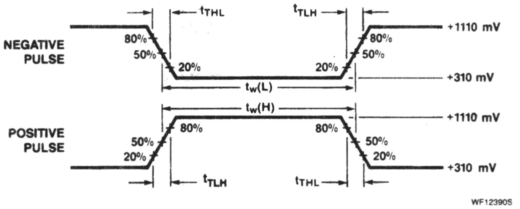
## TEST CIRCUITS AND WAVEFORMS


+2.0V ± 0.010V
25μF
0.1μF
PULSE GENERATOR
SCOPE CHANNEL A
L1
L3
16
1
4
VCC1
VCC2
D0
Q̄0
2
5
D1
6
D2
Q̄1
3
50Ω
7
D3
9
S1
VIHmax OR VILmin
10
D4
Q̄2
14
50Ω
11
D5
12
D6
Q̄3
15
50Ω
13
D7
VEE
8
L2
SCOPE CHANNEL B
CL
RT
RT
25μF
0.01μF
-3.2V ± 0.010V
TC04600S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$
2. Decoupling 0.1μF and 25μF from GND to $V_{CC}$, 0.01μF and 25μF from GND to $V_{EE}$. (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance $\leqslant$ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.

Figure 7. AC Test Circuit for 10100


NEGATIVE PULSE
POSITIVE PULSE
tTHL
tTLH
80%
50%
20%
20%
80%
50%
+1110 mV
+310 mV
tw(L)
tw(H)
+1110 mV
80%
80%
50%
20%
50%
20%
+310 mV
tTLH
tTHL
WF12390S

| INPUT PULSE REQUIREMENTS<br>$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$, $V_T$ = GND (0V) | | | | | |
|---|---|---|---|---|---|
| **Family** | **Amplitude** | **Rep Rate** | **Pulse Width** | **$t_{TLH}$** | **$t_{THL}$** |
| 10K ECL | 800mVp-p | 1MHz | 500ns | 2.0 ±0.2ns | 2.0 ±0.2ns |

Figure 8. Input Pulse Definition

**Signetics**

# 10101
## Gate

**Quad 2-Input OR/NOR Gate With Strobe**
***Product Specification***

**ECL Products**

### DESCRIPTION

The 10101 is a Quad 2-Input OR/NOR gate with one input from each gate common to pin 12. All unused inputs can be left open due to integrated pull-down resistors, which avoid the need for a supply voltage.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 10101 | 20ns | 20mA |

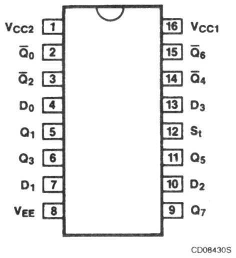
### ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} = GND$; $V_{EE} = -5.2V$<br>$T_A = -30°C$ to $+85°C$ |
|---|---|
| Plastic DIP | 10101N |
| Ceramic DIP | 10101F |

### PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_0 - D_3$ | Data Inputs |
| $S_t$ | Strobe Input |
| $Q_n$, $\overline{Q}_n$ | Data Outputs (OR/NOR) |

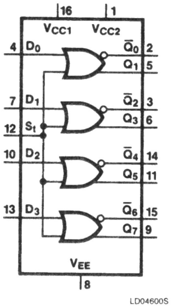
### PIN CONFIGURATION



$V_{CC2}$ 1
$\overline{Q}_0$ 2
$\overline{Q}_2$ 3
$D_0$ 4
$Q_1$ 5
$Q_3$ 6
$D_1$ 7
$V_{EE}$ 8
16 $V_{CC1}$
15 $\overline{Q}_6$
14 $\overline{Q}_4$
13 $D_3$
12 $S_t$
11 $Q_5$
10 $D_2$
9 $Q_7$
CD08430S

Figure 1

### LOGIC SYMBOL



16
1
$V_{CC1}$
$V_{CC2}$
4 $D_0$
$\overline{Q}_0$ 2
$Q_1$ 5
7 $D_1$
$\overline{Q}_2$ 3
$Q_3$ 6
12 $S_t$
10 $D_2$
$\overline{Q}_4$ 14
$Q_5$ 11
13 $D_3$
$\overline{Q}_6$ 15
$Q_7$ 9
$V_{EE}$
8
LD04600S

Figure 2

## Gate

## 10101

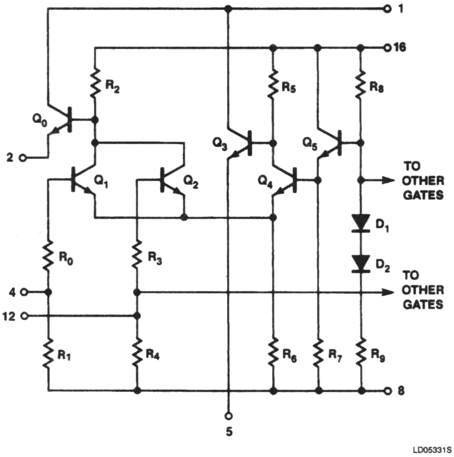
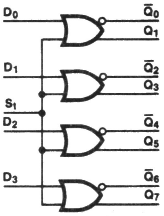

1
16
R2
R5
R8
Q0
Q3
Q5
2
Q1
Q2
Q4
TO OTHER GATES
D1
R0
R3
D2
TO OTHER GATES
4
12
R1
R4
R6
R7
R9
8
5
LD05331S

**Figure 3. Circuit Diagram (One Gate)**


D0
$\overline{Q}_0$
$Q_1$
D1
$\overline{Q}_2$
$Q_3$
St
D2
$\overline{Q}_4$
$Q_5$
D3
$\overline{Q}_6$
$Q_7$

$Q_0 = \overline{D_0 + S_t}$ $Q_4 = \overline{D_2 + S_t}$
$Q_1 = D_0 + S_t$ $Q_5 = D_2 + S_t$
$Q_2 = \overline{D_1 + S_t}$ $Q_6 = \overline{D_3 + S_t}$
$Q_3 = D_1 + S_t$ $Q_7 = D_3 + S_t$

POSITIVE LOGIC: HIGH state = 1
LOW state = 0

LD04610S

**Figure 4. Logic Diagram**

# Gate

# 10101

## ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | | 10K ECL | UNIT |
|---|---|---|---|---|
| $V_{EE}$ | Supply voltage | | −8.0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | | 0 to $V_{EE}$ | V |
| $I_O$ | Output current | | −50 | mA |
| $T_S$ | Storage temperature | | −55 to +150 | °C |
| $T_J$ | Maximum junction temperature | Ceramic package | +165 | °C |
| | | Plastic package | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | 10K ECL | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage | | | −5.2 | | V |
| $V_{IH}$ | HIGH level input voltage | $T_A$ = −30°C | | | −890 | mV |
| | | $T_A$ = +25°C | | | −810 | mV |
| | | $T_A$ = +85°C | | | −700 | mV |
| $V_{IHT}$ | HIGH level input threshold voltage | $T_A$ = −30°C | −1205 | | | mV |
| | | $T_A$ = +25°C | −1105 | | | mV |
| | | $T_A$ = +85°C | −1035 | | | mV |
| $V_{ILT}$ | LOW level input threshold voltage | $T_A$ = −30°C | | | −1500 | mV |
| | | $T_A$ = +25°C | | | −1475 | mV |
| | | $T_A$ = +85°C | | | −1440 | mV |
| $V_{IL}$ | LOW level input voltage | $T_A$ = −30°C | −1890 | | | mV |
| | | $T_A$ = +25°C | −1850 | | | mV |
| | | $T_A$ = +85°C | −1825 | | | mV |
| $T_A$ | Operating ambient temperature | | −30 | +25 | +85 | °C |

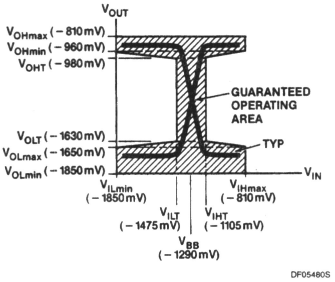
**NOTE:**
When operating at $V_{EE}$ other than specified voltage (−5.2V), the DC and AC Characteristics will vary slightly from specified values.
(See table of DC Electrical Characteristics.)

**DC ELECTRICAL CHARACTERISTICS** $V_{CC1} = V_{CC2} = \text{GND}$, $V_{EE} = -5.2\text{V} \pm 0.010\text{V}$, $T_A = -30°\text{C}$ to $+85°\text{C}$, output loading with 50Ω to −2.0V ±0.010V unless otherwise specified[1,3]

| PARAMETER | | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | | $T_A = -30°C$ | −1060 | | −890 | mV | For $Q_n$ outputs, apply $V_{IHmax}$ to all inputs. For $\overline{Q}_n$ outputs, apply $V_{ILmin}$ to all inputs. |
| | | | $T_A = +25°C$ | −960 | | −810 | mV | |
| | | | $T_A = +85°C$ | −890 | | −700 | mV | |
| $V_{OHT}$ | HIGH level output threshold voltage | | $T_A = -30°C$ | −1080 | | | mV | For $Q_n$ outputs, apply $V_{IHT}$ to $S_t$ input and $V_{ILmin}$ to all other inputs. For $\overline{Q}_n$ outputs, apply $V_{ILT}$ to $S_t$ input and $V_{ILmin}$ to all other inputs. |
| | | | $T_A = +25°C$ | −980 | | | mV | |
| | | | $T_A = +85°C$ | −910 | | | mV | |
| $V_{OLT}$ | LOW level output threshold voltage | | $T_A = -30°C$ | | | −1655 | mV | For $Q_n$ outputs, apply $V_{ILT}$ to $S_t$ input and $V_{ILmin}$ to all other inputs. For $\overline{Q}_n$ outputs, apply $V_{IHT}$ to $S_t$ input and $V_{ILmin}$ to all other inputs. |
| | | | $T_A = +25°C$ | | | −1630 | mV | |
| | | | $T_A = +85°C$ | | | −1595 | mV | |
| $V_{OL}$ | LOW level output voltage | | $T_A = -30°C$ | −1890 | | −1675 | mV | For $Q_n$ outputs, apply $V_{ILmin}$ to all inputs. For $\overline{Q}_n$ outputs, apply $V_{IHmax}$ to all inputs. |
| | | | $T_A = +25°C$ | −1850 | | −1650 | mV | |
| | | | $T_A = +85°C$ | −1825 | | −1615 | mV | |
| $I_{IH}$ | HIGH level input current | $D_n$ inputs | $T_A = -30°C$ | | | 425 | μA | Apply $V_{IHmax}$ to each input under test, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | | | 265 | μA | |
| | | | $T_A = +85°C$ | | | 265 | μA | |
| | | $S_t$ input | $T_A = -30°C$ | | | 850 | μA | Apply $V_{IHmax}$ to $S_t$ input with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | | | 535 | μA | |
| | | | $T_A = +85°C$ | | | 535 | μA | |
| $I_{IL}$ | LOW level input current | | $T_A = -30°C$ | 0.5 | | | μA | Apply $V_{ILmin}$ to each input under test, one at a time, with $V_{IHmax}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | 0.5 | | | μA | |
| | | | $T_A = +85°C$ | 0.3 | | | μA | |
| $-I_{EE}$ | $V_{EE}$ supply current | | $T_A = -30°C$ | | | 29 | mA | |
| | | | $T_A = +25°C$ | | 20 | 26 | mA | |
| | | | $T_A = +85°C$ | | | 29 | mA | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | | $T_A = +25°C$ | | 0.016 | | V/V | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | | 0.250 | | V/V | |
| $\frac{\Delta V_{BB}}{\Delta V_{EE}}$ | Reference bias voltage compensation | | | | 0.148 | | V/V | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst-case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 5.


$V_{OUT}$
$V_{OHmax}$ (−810mV)
$V_{OHmin}$ (−960mV)
$V_{OHT}$ (−980mV)
GUARANTEED OPERATING AREA
$V_{OLT}$ (−1630mV)
$V_{OLmax}$ (−1650mV)
$V_{OLmin}$ (−1850mV)
TYP
$V_{IN}$
$V_{ILmin}$ (−1850mV)
$V_{IHmax}$ (−810mV)
$V_{ILT}$ (−1475mV)
$V_{IHT}$ (−1105mV)
$V_{BB}$ (−1290mV)
DF05480S

**NOTES:**

$V_{IHmax}$ – Maximum HIGH level input voltage (the most positive $V_{IH}$).
$V_{IHT}$ – HIGH level input threshold voltage.
$V_{ILT}$ – LOW level input threshold voltage.
$V_{ILmin}$ – Minimum LOW level input voltage (the most negative $V_{IL}$).
$V_{OHmax}$ – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition.
$V_{OHmin}$ – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition.
$V_{OHT}$ – HIGH level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLT}$ – LOW level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLmax}$ – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions.
$V_{OLmin}$ – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions.
$V_{BB}$ – Reference bias voltage (the internally generated reference voltage which is used to set the input and output threshold level).

**Figure 5. Transfer Characteristics**

## AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$

| PARAMETER | $T_A = -30°C$ | | $T_A = +25°C$ | | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Typ | Max | Min | Max | | |
| $t_{PLH}$ Propagation delay | 1.0 | 3.1 | 1.0 | 2.0 | 2.9 | 1.0 | 3.3 | ns | Figs. 6, 7, 8 |
| $t_{PHL}$ $D_n$ to $Q_n$, $\overline{Q}_n$ | 1.0 | 3.1 | 1.0 | 2.0 | 2.9 | 1.0 | 3.3 | ns | |
| $t_{TLH}$ Transition time | 1.1 | 3.6 | 1.1 | 2.0 | 3.3 | 1.1 | 3.7 | ns | Figs. 6, 7, 8 |
| $t_{THL}$ 20% to 80%, 80% to 20% | 1.1 | 3.6 | 1.1 | 2.0 | 3.3 | 1.1 | 3.7 | ns | |

## AC WAVEFORMS

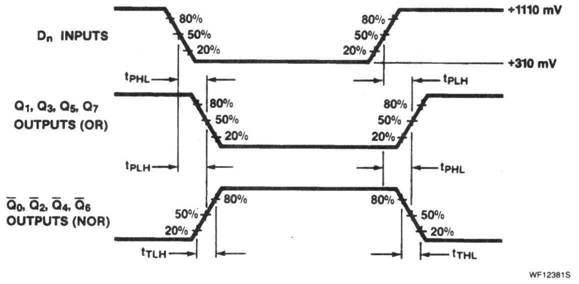
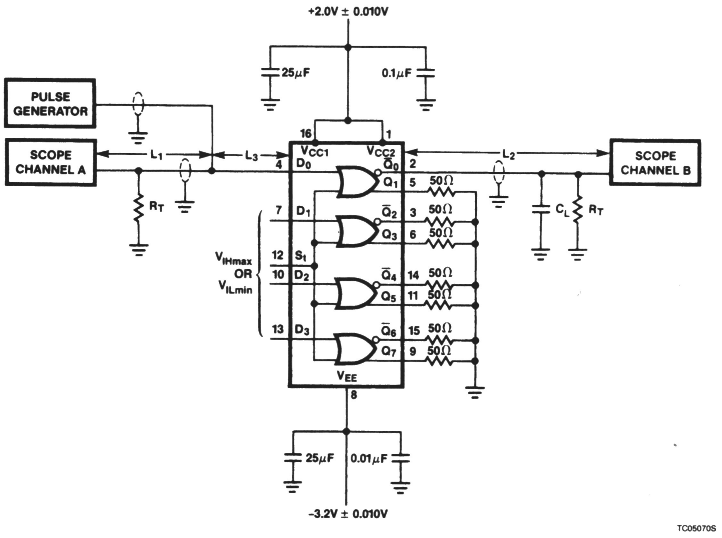

$D_n$ INPUTS
80%
50%
20%
+1110 mV
+310 mV
$t_{PHL}$
$t_{PLH}$
$Q_1, Q_3, Q_5, Q_7$ OUTPUTS (OR)
80%
50%
20%
$t_{PLH}$
$t_{PHL}$
$\overline{Q}_0, \overline{Q}_2, \overline{Q}_4, \overline{Q}_6$ OUTPUTS (NOR)
80%
50%
20%
$t_{TLH}$
$t_{THL}$
WF12381S

**Figure 6. Propagation Delay and Transition Times**

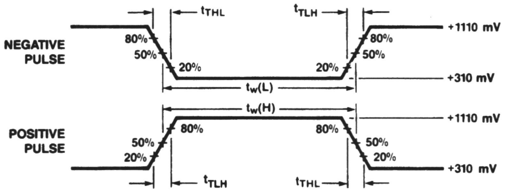
## TEST CIRCUITS AND WAVEFORMS


+2.0V ± 0.010V
25μF
0.1μF
PULSE GENERATOR
SCOPE CHANNEL A
L1
L3
RT
16
1
VCC1
VCC2
4
D0
Q̄0
2
Q1
5
50Ω
7
D1
Q̄2
3
Q3
6
12
S1
10
D2
Q̄4
14
Q5
11
13
D3
Q̄6
15
Q7
9
VIHmax OR VILmin
VEE
8
25μF
0.01μF
-3.2V ± 0.010V
L2
SCOPE CHANNEL B
CL
RT
TC05070S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1μF and 25μF from GND to $V_{CC}$, 0.01μF and 25μF from GND to $V_{EE}$. (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance $\leq$ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ±1% or better.

**Figure 7. AC Test Circuit for 10101**


NEGATIVE PULSE
POSITIVE PULSE
tTHL
tTLH
80%
50%
20%
+1110 mV
+310 mV
tw(L)
tw(H)
WF12390S

| INPUT PULSE REQUIREMENTS<br>$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$, $V_T$ = GND (0V) | | | | | |
|---|---|---|---|---|---|
| **Family** | **Amplitude** | **Rep Rate** | **Pulse Width** | $t_{TLH}$ | $t_{THL}$ |
| 10K ECL | 800mVp-p | 1MHz | 500ns | 2.0 ±0.2ns | 2.0 ±0.2ns |

**Figure 8. Input Pulse Definition**

Signetics

# 10102
## Gate

**Quad 2-Input NOR (3 NOR and 1 OR/NOR) Gate**
***Product Specification***

**ECL Products**

### DESCRIPTION

The 10102 is a Quad 2-Input NOR gate. All unused inputs can be left open due to integrated pull-down resistors, which avoid the need for a supply voltage.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 10102 | 2.0ns | 20mA |

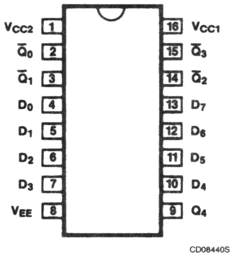
### ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} = GND$; $V_{EE} = -5.2V$<br>$T_A = -30°C$ to $+85°C$ |
|---|---|
| Plastic DIP | 10102N |
| Ceramic DIP | 10102F |

### PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_0$–$D_7$ | Data Inputs |
| $Q_4$ | Data Output (OR) |
| $\overline{Q}_0$–$\overline{Q}_3$ | Data Outputs (NOR) |

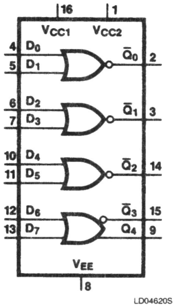
### PIN CONFIGURATION



$V_{CC2}$ 1
$\overline{Q}_0$ 2
$\overline{Q}_1$ 3
$D_0$ 4
$D_1$ 5
$D_2$ 6
$D_3$ 7
$V_{EE}$ 8
16 $V_{CC1}$
15 $\overline{Q}_3$
14 $\overline{Q}_2$
13 $D_7$
12 $D_6$
11 $D_5$
10 $D_4$
9 $Q_4$
CD08440S

Figure 1

### LOGIC SYMBOL

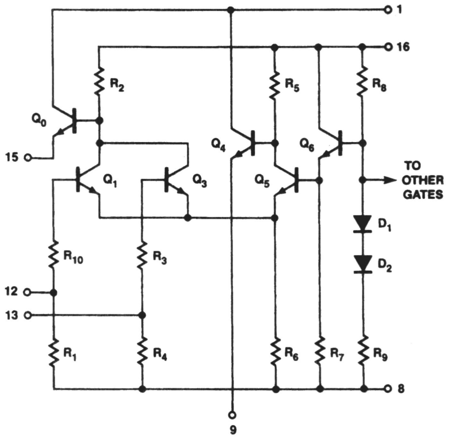


16
1
$V_{CC1}$
$V_{CC2}$
4 $D_0$
5 $D_1$
$\overline{Q}_0$ 2
6 $D_2$
7 $D_3$
$\overline{Q}_1$ 3
10 $D_4$
11 $D_5$
$\overline{Q}_2$ 14
12 $D_6$
13 $D_7$
$\overline{Q}_3$ 15
$Q_4$ 9
$V_{EE}$
8
LD04620S

Figure 2

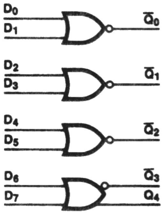
## Gate

## 10102


1
16
R2
Q0
15
R5
R8
Q4
Q6
Q1
Q3
Q5
TO
OTHER
GATES
D1
D2
R10
R3
12
13
R1
R4
R6
R7
R9
8
9

TC04620S

Figure 3. Circuit Diagram (One Gate)


D0
D1
Q̅0
D2
D3
Q̅1
D4
D5
Q̅2
D6
D7
Q̅3
Q4

LD04630S

$Q_0 = \overline{D_0 + D_1}$
$Q_1 = \overline{D_2 + D_3}$
$Q_2 = \overline{D_4 + D_5}$
$Q_3 = \overline{D_6 + D_7}$
$Q_4 = D_6 + D_7$

POSITIVE LOGIC: HIGH STATE = 1
LOW STATE = 0

Figure 4. Logic Diagram

## ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | | 10K ECL | UNIT |
|---|---|---|---|---|
| $V_{EE}$ | Supply voltage | | -8.0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | | 0 to $V_{EE}$ | V |
| $I_O$ | Output current | | -50 | mA |
| $T_S$ | Storage temperature | | -55 to +150 | °C |
| $T_J$ | Maximum junction temperature | Ceramic package | +165 | °C |
| | | Plastic package | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | 10K ECL | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | -5.2 | | V |
| $V_{IH}$ | HIGH level input voltage | $T_A = -30°C$ | | | -890 | mV |
| | | $T_A = +25°C$ | | | -810 | mV |
| | | $T_A = +85°C$ | | | -700 | mV |
| $V_{IHT}$ | HIGH level input threshold voltage | $T_A = -30°C$ | -1205 | | | mV |
| | | $T_A = +25°C$ | -1105 | | | mV |
| | | $T_A = +85°C$ | -1035 | | | mV |
| $V_{ILT}$ | LOW level input threshold voltage | $T_A = -30°C$ | | | -1500 | mV |
| | | $T_A = +25°C$ | | | -1475 | mV |
| | | $T_A = +85°C$ | | | -1440 | mV |
| $V_{IL}$ | LOW level input voltage | $T_A = -30°C$ | -1890 | | | mV |
| | | $T_A = +25°C$ | -1850 | | | mV |
| | | $T_A = +85°C$ | -1825 | | | mV |
| $T_A$ | Operating ambient temperature | | -30 | +25 | +85 | °C |

**NOTE:**
When operating at $V_{EE}$ other than specified voltage (-5.2V), the DC and AC Characteristics will vary slightly from specified values.
(See table of DC Electrical Characteristics)

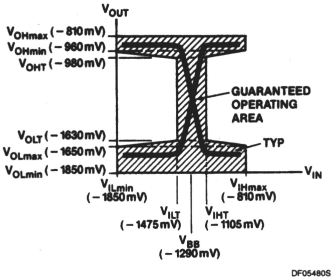
**DC ELECTRICAL CHARACTERISTICS** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$, loading with $50\Omega$ to $-2.0V \pm 0.010V$ unless otherwise specified[1,3]

| PARAMETER | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | $T_A = -30°C$ | -1060 | | -890 | mV | For $\overline{Q}_n$ outputs, apply $V_{ILmin}$ to all inputs. For $Q_4$ output, apply $V_{IHmax}$ to all inputs. |
| | | $T_A = +25°C$ | -960 | | -810 | mV | |
| | | $T_A = +85°C$ | -890 | | -700 | mV | |
| $V_{OHT}$ | HIGH level output threshold voltage | $T_A = -30°C$ | -1080 | | | mV | For $\overline{Q}_n$ outputs, apply $V_{ILT}$ to one gate input with $V_{ILmin}$ applied to the other gate input. For $Q_4$ output, apply $V_{IHT}$ to one gate input with $V_{ILmin}$ applied to the other gate input. |
| | | $T_A = +25°C$ | -980 | | | mV | |
| | | $T_A = +85°C$ | -910 | | | mV | |
| $V_{OLT}$ | LOW level output threshold voltage | $T_A = -30°C$ | | | -1655 | mV | For $\overline{Q}_n$ outputs, apply $V_{IHT}$ to one gate input with $V_{ILmin}$ applied to the other gate input. For $Q_4$ output, apply $V_{ILT}$ to one gate input with $V_{ILmin}$ applied to the other gate input. |
| | | $T_A = +25°C$ | | | -1630 | mV | |
| | | $T_A = +85°C$ | | | -1595 | mV | |
| $V_{OL}$ | LOW level output voltage | $T_A = -30°C$ | -1890 | | -1675 | mV | For $\overline{Q}_n$ outputs, apply $V_{IHmax}$ to all inputs. For $Q_4$ output apply $V_{ILmin}$ to all inputs. |
| | | $T_A = +25°C$ | -1850 | | -1650 | mV | |
| | | $T_A = +85°C$ | -1825 | | -1615 | mV | |
| $I_{IH}$ | HIGH level input current | $T_A = -30°C$ | | | 425 | µA | Apply $V_{IHmax}$ to each input under test, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | $T_A = +25°C$ | | | 265 | µA | |
| | | $T_A = +85°C$ | | | 265 | µA | |
| $I_{IL}$ | LOW level input current | $T_A = -30°C$ | 0.5 | | | µA | Apply $V_{ILmin}$ to each input under test, one at a time, with $V_{IHmax}$ applied to all other inputs. |
| | | $T_A = +25°C$ | 0.5 | | | µA | |
| | | $T_A = +85°C$ | 0.3 | | | µA | |
| $-I_{EE}$ | $V_{EE}$ supply current | $T_A = -30°C$ | | | 29 | mA | |
| | | $T_A = +25°C$ | | 20 | 26 | mA | |
| | | $T_A = +85°C$ | | | 29 | mA | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | $T_A = +25°C$ | | 0.016 | | V/V | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | 0.250 | | V/V | |
| $\frac{\Delta V_{BB}}{\Delta V_{EE}}$ | Reference bias voltage compensation | | | 0.148 | | V/V | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst-case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 5.

# Gate 10102



**NOTES:**

| | |
|---|---|
| $V_{IHmax}$ | – Maximum HIGH level input voltage (the most positive $V_{IH}$). |
| $V_{IHT}$ | – HIGH level input threshold voltage. |
| $V_{ILT}$ | – LOW level input threshold voltage. |
| $V_{ILmin}$ | – Minimum LOW level input voltage (the most negative $V_{IL}$). |
| $V_{OHmax}$ | – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition. |
| $V_{OHmin}$ | – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition. |
| $V_{OHT}$ | – HIGH level output threshold voltage with the inputs set to their respective threshold levels. |
| $V_{OLT}$ | – LOW level output threshold voltage with the inputs set to their respective threshold levels. |
| $V_{OLmax}$ | – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions. |
| $V_{OLmin}$ | – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions. |
| $V_{BB}$ | – Reference bias voltage (the internally generated reference voltage which is used to set the input and output threshold level). |

Figure 5. Transfer Characteristics

## AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$

| PARAMETER | $T_A = -30°C$ | | $T_A = +25°C$ | | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Typ | Max | Min | Max | | |
| $t_{PLH}$ Propagation delay<br>$t_{PHL}$ $D_n$ to $\overline{Q}_n$, $Q_4$ | 1.0<br>1.0 | 3.1<br>3.1 | 1.0<br>1.0 | 2.0<br>2.0 | 2.9<br>2.9 | 1.0<br>1.0 | 3.3<br>3.3 | ns<br>ns | Figs. 6, 7, 8 |
| $t_{TLH}$ Transition time<br>$t_{THL}$ 20% to 80%, 80% to 20% | 1.1<br>1.1 | 3.6<br>3.6 | 1.1<br>1.1 | 2.0<br>2.0 | 3.3<br>3.3 | 1.1<br>1.1 | 3.7<br>3.7 | ns<br>ns | Figs. 6, 7, 8 |

## AC WAVEFORMS

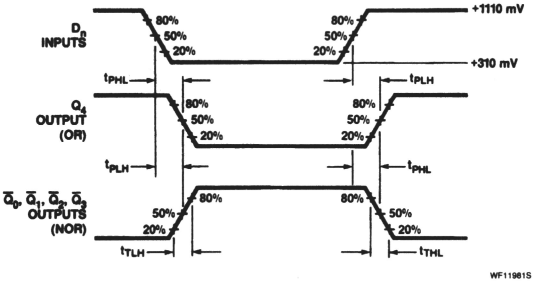
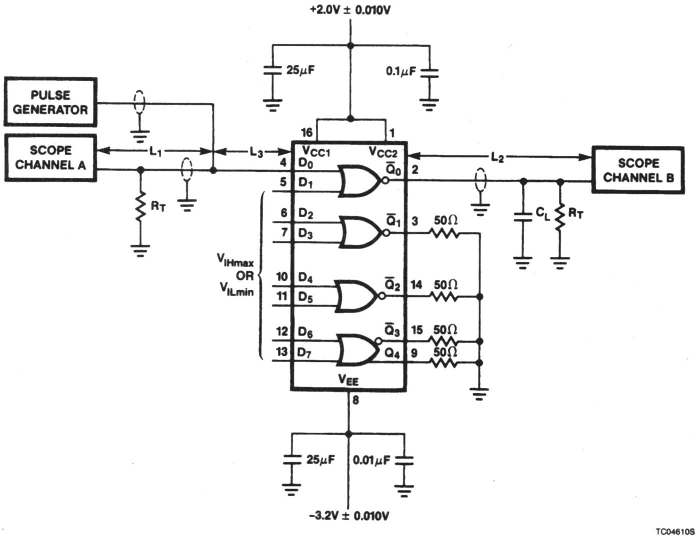


Figure 6. Propagation Delay and Transition Times

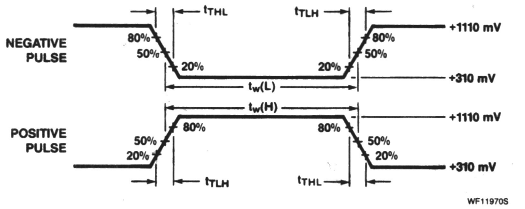
## TEST CIRCUITS AND WAVEFORMS


+2.0V ± 0.010V
25µF
0.1µF
PULSE GENERATOR
SCOPE CHANNEL A
L1
L3
L2
SCOPE CHANNEL B
RT
CL
16
1
VCC1
VCC2
4 D0
5 D1
6 D2
7 D3
10 D4
11 D5
12 D6
13 D7
Q̄0 2
Q̄1 3
Q̄2 14
Q̄3 15
Q4 9
50Ω
VIHmax OR VILmin
VEE
8
25µF
0.01µF
-3.2V ± 0.010V
TC04610S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$
2. Decoupling 0.1µF and 25µF from GND to $V_{CC}$, 0.01µF and 25µF from GND to $V_{EE}$. (0.01 and 0.1µF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance ≤ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ±1% or better.

**Figure 7. AC Test Circuit for 10102**


NEGATIVE PULSE
POSITIVE PULSE
tTHL
tTLH
80%
50%
20%
tw(L)
tw(H)
+1110 mV
+310 mV
WF11970S

| INPUT PULSE REQUIREMENTS<br>$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$, $V_T$ = GND (0V) | | | | | |
|---|---|---|---|---|---|
| **Family** | **Amplitude** | **Rep Rate** | **Pulse Width** | **$t_{TLH}$** | **$t_{THL}$** |
| 10K ECL | 800mVp-p | 1MHz | 500ns | 2.0 ±0.2ns | 2.0 ±0.2ns |

**Figure 8. Input Pulse Definition**

**Signetics**

# 10103
## Gate

**Quad 2-Input OR (3 OR and 1 OR/NOR) Gate**
***Product Specification***

**ECL Products**

### DESCRIPTION

The 10103 is a Quad 2-Input 3 OR and 1 OR/NOR gate. All unused inputs can be left open due to integrated pull-down resistors which avoid the need for a supply voltage.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT $(-I_{EE})$ |
|---|---|---|
| 10103 | 2.0ns | 21mA |

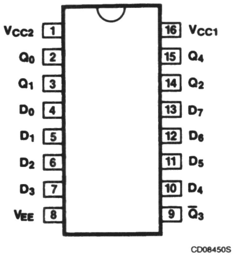
### ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} = GND$; $V_{EE} = -5.2V$<br>$T_A = -30°C$ to $+85°C$ |
|---|---|
| Plastic DIP | 10103N |
| Ceramic DIP | 10103F |

### PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_0$–$D_7$ | Data Inputs |
| $Q_0$, $Q_1$, $Q_2$, $Q_4$ | Data Outputs (OR) |
| $\overline{Q}_3$ | Data Output (NOR) |

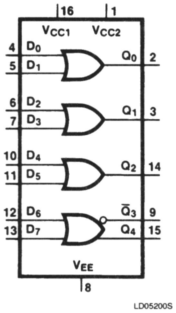
### PIN CONFIGURATION



VCC2 1
Q0 2
Q1 3
D0 4
D1 5
D2 6
D3 7
VEE 8
16 VCC1
15 Q4
14 Q2
13 D7
12 D6
11 D5
10 D4
9 Q̄3
CD08450S

Figure 1

### LOGIC SYMBOL



16
1
VCC1
VCC2
4 D0
5 D1
Q0 2
6 D2
7 D3
Q1 3
10 D4
11 D5
Q2 14
12 D6
13 D7
Q̄3 9
Q4 15
VEE
8
LD05200S

Figure 2

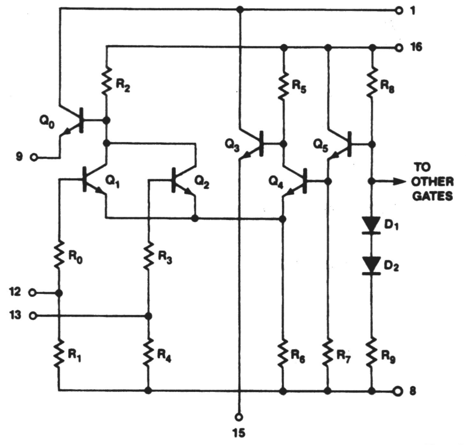
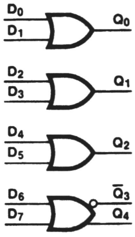

1
16
R2
R5
R8
Q0
9
Q1
Q2
Q3
Q4
Q5
TO OTHER GATES
D1
D2
R0
R3
12
13
R1
R4
R6
R7
R9
8
15
TC04630S

Figure 3. Circuit Diagram (One Gate)


D0
D1
Q0
D2
D3
Q1
D4
D5
Q2
D6
D7
Q̄3
Q4

$Q_0=D_0+D_1$

$Q_1=D_2+D_3$

$Q_2=D_4+D_5$

$Q_4=D_6+D_7$

$Q_3=\overline{Q}_4$

Positive logic: HIGH state = 1
LOW state = 0

LD04641S

Figure 4. Logic Diagram

# Gate 10103

## ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | | 10K ECL | UNIT |
|---|---|---|---|---|
| $V_{EE}$ | Supply voltage | | -8.0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | | 0 to $V_{EE}$ | V |
| $I_O$ | Output current | | -50 | mA |
| $T_S$ | Storage temperature | | -55 to +150 | °C |
| $T_J$ | Maximum junction temperature | Ceramic package | +165 | °C |
| | | Plastic package | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | 10K ECL | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | -5.2 | | V |
| $V_{IH}$ | HIGH level input voltage | $T_A = -30°C$ | | | -890 | mV |
| | | $T_A = +25°C$ | | | -810 | mV |
| | | $T_A = +85°C$ | | | -700 | mV |
| $V_{IHT}$ | HIGH level input threshold voltage | $T_A = -30°C$ | -1205 | | | mV |
| | | $T_A = +25°C$ | -1105 | | | mV |
| | | $T_A = +85°C$ | -1035 | | | mV |
| $V_{ILT}$ | LOW level input threshold voltage | $T_A = -30°C$ | | | -1500 | mV |
| | | $T_A = +25°C$ | | | -1475 | mV |
| | | $T_A = +85°C$ | | | -1440 | mV |
| $V_{IL}$ | LOW level input voltage | $T_A = -30°C$ | -1890 | | | mV |
| | | $T_A = +25°C$ | -1850 | | | mV |
| | | $T_A = +85°C$ | -1825 | | | mV |
| $T_A$ | Operating ambient temperature | | -30 | +25 | +85 | °C |

**NOTE:**
When operating at $V_{EE}$ other than specified voltage (-5.2V), the DC and AC Characteristics will vary slightly from specified values. (See table of DC Electrical Characteristics)

6

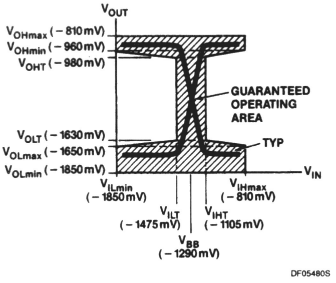
# Gate 10103

**DC ELECTRICAL CHARACTERISTICS** $V_{CC1} = V_{CC2} =$ GND, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$, output loading with 50Ω to $-2.0V \pm 0.010V$ unless otherwise specified[1,3]

| PARAMETER | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | $T_A = -30°C$ | -1060 | | -890 | mV | For $Q_n$ outputs, apply $V_{IHmax}$ to all inputs.<br>For $\overline{Q}_3$ output, apply $V_{ILmin}$ to all inputs. |
| | | $T_A = +25°C$ | -960 | | -810 | mV | |
| | | $T_A = +85°C$ | -890 | | -700 | mV | |
| $V_{OHT}$ | HIGH level output threshold voltage | $T_A = -30°C$ | -1080 | | | mV | For $Q_n$ outputs, apply $V_{IHT}$ to one gate input with $V_{ILmin}$ applied to the other gate input.<br>For $\overline{Q}_3$ output, apply $V_{ILT}$ to one gate input with $V_{ILmin}$ applied to the other gate input. |
| | | $T_A = +25°C$ | -980 | | | mV | |
| | | $T_A = +85°C$ | -910 | | | mV | |
| $V_{OLT}$ | LOW level output threshold voltage | $T_A = -30°C$ | | | -1655 | mV | For $Q_n$ outputs, apply $V_{ILT}$ to one gate input with $V_{ILmin}$ applied to the other gate input.<br>For $\overline{Q}_3$ output, apply $V_{IHT}$ to one gate input with $V_{ILmin}$ applied to the other gate input. |
| | | $T_A = +25°C$ | | | -1630 | mV | |
| | | $T_A = +85°C$ | | | -1595 | mV | |
| $V_{OL}$ | LOW level output voltage | $T_A = -30°C$ | -1890 | | -1675 | mV | For $Q_n$ outputs, apply $V_{ILmin}$ to all inputs.<br>For $\overline{Q}_3$ output, apply $V_{IHmax}$ to all inputs. |
| | | $T_A = +25°C$ | -1850 | | -1650 | mV | |
| | | $T_A = +85°C$ | -1825 | | -1615 | mV | |
| $I_{IH}$ | HIGH level input current | $T_A = -30°C$ | | | 390 | μA | Apply $V_{IHmax}$ to each input under test, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | $T_A = +25°C$ | | | 245 | μA | |
| | | $T_A = +85°C$ | | | 245 | μA | |
| $I_{IL}$ | LOW level input current | $T_A = -30°C$ | 0.5 | | | μA | Apply $V_{ILmin}$ to each input under test, one at a time, with $V_{IHmax}$ applied to all other inputs. |
| | | $T_A = +25°C$ | 0.5 | | | μA | |
| | | $T_A = +85°C$ | 0.3 | | | μA | |
| $-I_{EE}$ | $V_{EE}$ supply current | $T_A = -30°C$ | | | 29 | mA | |
| | | $T_A = +25°C$ | | 21 | 26 | mA | |
| | | $T_A = +85°C$ | | | 29 | mA | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | $T_A = +25°C$ | | 0.016 | | V/V | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | 0.250 | | V/V | |
| $\frac{\Delta V_{BB}}{\Delta V_{EE}}$ | Reference bias voltage compensation | | | 0.148 | | V/V | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst-case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 5.



**NOTES:**

$V_{IHmax}$ – Maximum HIGH level input voltage (the most positive $V_{IH}$).
$V_{IHT}$ – HIGH level input threshold voltage.
$V_{ILT}$ – LOW level input threshold voltage.
$V_{ILmin}$ – Minimum LOW level input voltage (the most negative $V_{IL}$).
$V_{OHmax}$ – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition.
$V_{OHmin}$ – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition.
$V_{OHT}$ – HIGH level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLT}$ – LOW level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLmax}$ – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions.
$V_{OLmin}$ – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions.
$V_{BB}$ – Reference bias voltage (the internally generated reference voltage which is used to set the input and output threshold level).

**Figure 5. Transfer Characteristics**

## AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$

| PARAMETER | $T_A = -30°C$ | | $T_A = +25°C$ | | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Typ | Max | Min | Max | | |
| $t_{PLH}$ Propagation delay | 1.0 | 3.1 | 1.0 | 2.0 | 2.9 | 1.0 | 3.3 | ns | Figs. 6, 7, 8 |
| $t_{PHL}$ $D_n$ to $Q_n$, $\overline{Q}_3$ | 1.0 | 3.1 | 1.0 | 2.0 | 2.9 | 1.0 | 3.3 | ns | |
| $t_{TLH}$ Transition time | 1.1 | 3.6 | 1.1 | 2.0 | 3.3 | 1.1 | 3.7 | ns | Figs. 6, 7, 8 |
| $t_{THL}$ 20% to 80%, 80% to 20% | 1.1 | 3.6 | 1.1 | 2.0 | 3.3 | 1.1 | 3.7 | ns | |

## AC WAVEFORMS

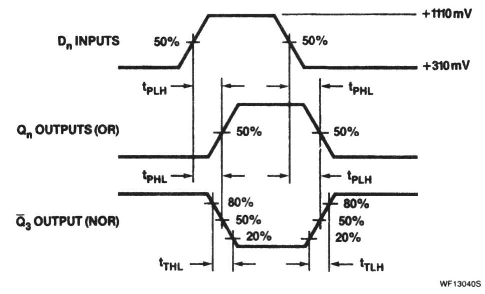
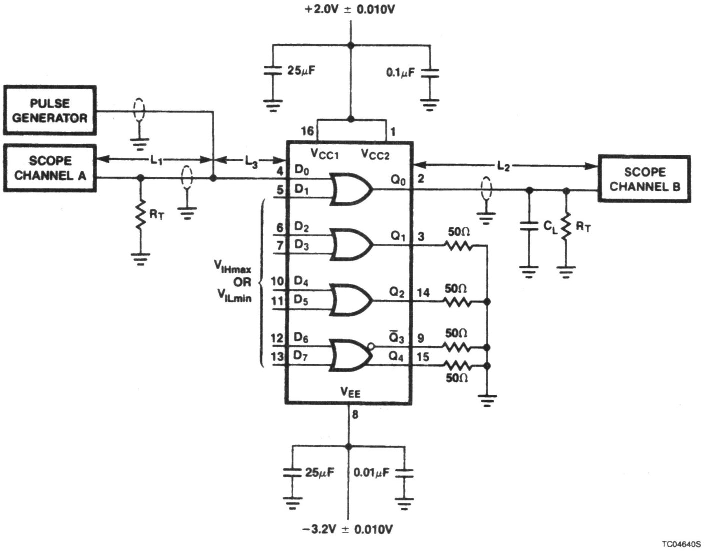


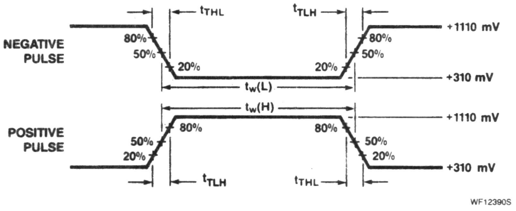
**Figure 6. Propagation Delay and Transition Times**

## TEST CIRCUITS AND WAVEFORMS


+2.0V ± 0.010V
25μF
0.1μF
PULSE GENERATOR
SCOPE CHANNEL A
L1
L3
L2
16
1
VCC1
VCC2
4 D0
5 D1
Q0 2
6 D2
7 D3
Q1 3
10 D4
11 D5
Q2 14
12 D6
13 D7
Q̄3 9
Q4 15
50Ω
50Ω
50Ω
50Ω
VEE
8
RT
CL
RT
VIHmax OR VILmin
SCOPE CHANNEL B
25μF
0.01μF
−3.2V ± 0.010V
TC04640S

**NOTES:**
1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$
2. Decoupling 0.1μF and 25μF from GND to $V_{CC}$, 0.01μF and 25μF from GND to $V_{EE}$. (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance $\leqslant$ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.

Figure 7. AC Test Circuit for 10103


NEGATIVE PULSE
POSITIVE PULSE
tTHL
tTLH
80%
50%
20%
20%
80%
50%
tw(L)
tw(H)
80%
80%
50%
20%
50%
20%
tTLH
tTHL
+1110 mV
+310 mV
+1110 mV
+310 mV
WF12390S

**INPUT PULSE REQUIREMENTS**

**$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$, $V_T$ = GND (0V)**

| Family | Amplitude | Rep Rate | Pulse Width | $t_{TLH}$ | $t_{THL}$ |
|---|---|---|---|---|---|
| 10K ECL | 800mVp-p | 1MHz | 500ns | 2.0 ± 0.2ns | 2.0 ± 0.2ns |

Figure 8. Input Pulse Definition

**Signetics**

# 10104
## Gate

**Quad 2-Input AND Gate**
***Product Specification***

**ECL Products**

## DESCRIPTION

The 10104 is a high-speed logic, low power, AND function.

All unused inputs can be left open due to integrated pull-down resistors which avoid the need for a supply voltage.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT $(-I_{EE})$ |
|---|---|---|
| 10104 | 2.7ns | 20mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} = GND$; $V_{EE} = -5.2V$<br>$T_A = -30°C$ to $+85°C$ |
|---|---|
| Plastic DIP | 10104N |
| Ceramic DIP | 10104F |

## PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_0$–$D_7$ | Data Inputs |
| $Q_0$, $Q_1$, $Q_2$, $Q_4$ | Data Outputs (AND) |
| $\overline{Q}_3$ | Data Output (NAND) |

## PIN CONFIGURATION

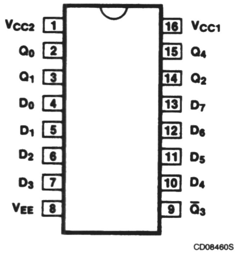

$V_{CC2}$ 1
$Q_0$ 2
$Q_1$ 3
$D_0$ 4
$D_1$ 5
$D_2$ 6
$D_3$ 7
$V_{EE}$ 8
16 $V_{CC1}$
15 $Q_4$
14 $Q_2$
13 $D_7$
12 $D_6$
11 $D_5$
10 $D_4$
9 $\overline{Q}_3$
CD08460S

Figure 1

## LOGIC SYMBOL

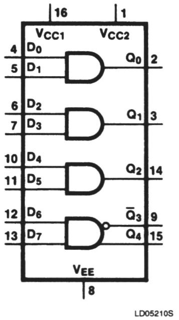

16
1
$V_{CC1}$
$V_{CC2}$
4 $D_0$
5 $D_1$
$Q_0$ 2
6 $D_2$
7 $D_3$
$Q_1$ 3
10 $D_4$
11 $D_5$
$Q_2$ 14
12 $D_6$
13 $D_7$
$\overline{Q}_3$ 9
$Q_4$ 15
$V_{EE}$
8
LD05210S

Figure 2

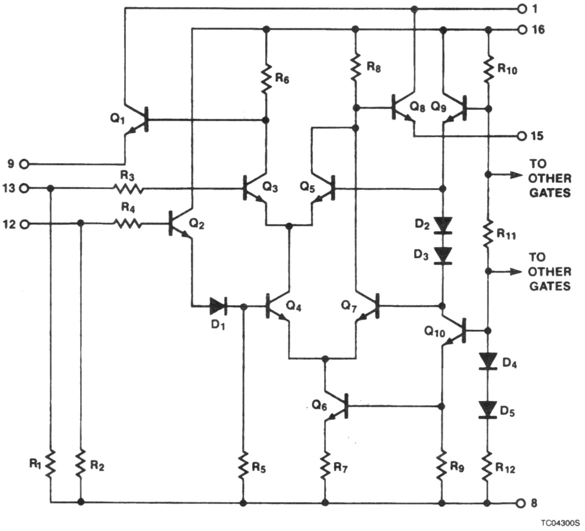
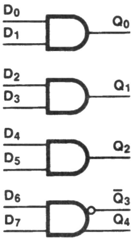

1
16
R$_6$
R$_8$
R$_{10}$
Q$_1$
Q$_8$ Q$_9$
15
9
13
12
R$_3$
R$_4$
Q$_3$
Q$_5$
Q$_2$
TO OTHER GATES
D$_2$
D$_3$
R$_{11}$
TO OTHER GATES
D$_1$
Q$_4$
Q$_7$
Q$_{10}$
D$_4$
D$_5$
Q$_6$
R$_1$
R$_2$
R$_5$
R$_7$
R$_9$
R$_{12}$
8
TC04300S

**Figure 3. Circuit Diagram (One Gate)**


D$_0$
D$_1$
Q$_0$
D$_2$
D$_3$
Q$_1$
D$_4$
D$_5$
Q$_2$
D$_6$
D$_7$
$\overline{Q}_3$
Q$_4$

$Q_0 = D_0 \cdot D_1$
$Q_1 = D_2 \cdot D_3$
$Q_2 = D_4 \cdot D_5$
$Q_3 = \overline{Q}_4$
$Q_4 = D_6 \cdot D_7$

**Positive logic**
**H = HIGH state**
**(the more positive voltage) = 1**
**L = LOW state**
**(the more negative voltage) = 1**

LD04651S

**Figure 4. Logic Diagram**

## Gate

## 10104

**ABSOLUTE MAXIMUM RATINGS** (Operation beyond the limits set forth in this table may impair useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | | 10K ECL | UNIT |
|---|---|---|---|---|
| $V_{EE}$ | Supply voltage | | −8.0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | | 0 to $V_{EE}$ | V |
| $I_O$ | Output current | | −50 | mA |
| $T_S$ | Storage temperature | | −55 to +150 | °C |
| $T_J$ | Maximum junction temperature | Ceramic package | +165 | °C |
| | | Plastic package | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | 10K ECL | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | −5.2 | | V |
| $V_{IH}$ | HIGH level input voltage | $T_A$ = −30°C | | | −890 | mV |
| | | $T_A$ = +25°C | | | −810 | mV |
| | | $T_A$ = +85°C | | | −700 | mV |
| $V_{IHT}$ | HIGH level input threshold voltage | $T_A$ = −30°C | −1205 | | | mV |
| | | $T_A$ = +25°C | −1105 | | | mV |
| | | $T_A$ = +85°C | −1035 | | | mV |
| $V_{ILT}$ | LOW level input threshold voltage | $T_A$ = −30°C | | | −1500 | mV |
| | | $T_A$ = +25°C | | | −1475 | mV |
| | | $T_A$ = +85°C | | | −1440 | mV |
| $V_{IL}$ | LOW level input voltage | $T_A$ = −30°C | −1890 | | | mV |
| | | $T_A$ = +25°C | −1850 | | | mV |
| | | $T_A$ = +85°C | −1825 | | | mV |
| $T_A$ | Operating ambient temperature | | −30 | +25 | +85 | °C |

**NOTE:**
When operating at $V_{EE}$ other than specified voltage (−5.2V), the DC and AC Characteristics will vary slightly from specified values.
(See table of DC Characteristics)

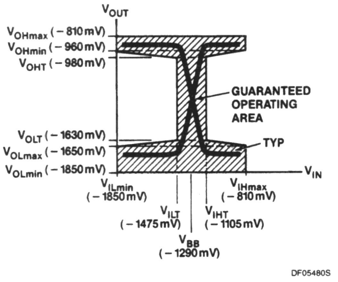
## DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = GND, $V_{EE} = -5.2V \pm 0.010V$, $T_A$ = −30°C to +85°C, output loading with 50Ω to −2.0V ±0.010V, unless otherwise specified[1,3]

| PARAMETER | | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | | $T_A$ = −30°C | −1060 | | −890 | mV | For $Q_n$ outputs, apply $V_{IHmax}$ to all inputs.<br>For $\overline{Q}_3$ output, apply $V_{ILmin}$ to all inputs. |
| | | | $T_A$ = +25°C | −960 | | −810 | mV | |
| | | | $T_A$ = +85°C | −890 | | −700 | mV | |
| $V_{OHT}$ | HIGH level output threshold voltage | | $T_A$ = −30°C | −1080 | | | mV | For $Q_n$ outputs, apply $V_{IHT}$ to one gate input with $V_{IHmax}$ applied to the other gate input.<br>For $\overline{Q}_3$ output, apply $V_{ILT}$ to one gate input with $V_{IHmax}$ applied to the other gate input. |
| | | | $T_A$ = +25°C | −980 | | | mV | |
| | | | $T_A$ = +85°C | −910 | | | mV | |
| $V_{OLT}$ | LOW level output threshold voltage | | $T_A$ = −30°C | | | −1655 | mV | For $Q_n$ outputs, apply $V_{ILT}$ to one gate input with $V_{IHmax}$ applied to the other gate input.<br>For $\overline{Q}_3$ output, apply $V_{IHT}$ to one gate input with $V_{IHmax}$ applied to the other gate input. |
| | | | $T_A$ = +25°C | | | −1630 | mV | |
| | | | $T_A$ = +85°C | | | −1595 | mV | |
| $V_{OL}$ | LOW level output voltage | | $T_A$ = −30°C | −1890 | | −1675 | mV | For $Q_n$ outputs, apply $V_{ILmin}$ to all inputs.<br>For $\overline{Q}_3$ output, apply $V_{IHmax}$ to all inputs. |
| | | | $T_A$ = +25°C | −1850 | | −1650 | mV | |
| | | | $T_A$ = +85°C | −1825 | | −1615 | mV | |
| $I_{IH}$ | HIGH level input current | $D_0$, $D_3$, $D_4$, $D_7$ inputs | $T_A$ = −30°C | | | 425 | μA | Apply $V_{IHmax}$ to each input under test, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A$ = +25°C | | | 265 | μA | |
| | | | $T_A$ = +85°C | | | 265 | μA | |
| | | $D_1$, $D_2$, $D_5$, $D_6$ inputs | $T_A$ = −30°C | | | 350 | μA | |
| | | | $T_A$ = +25°C | | | 220 | μA | |
| | | | $T_A$ = +85°C | | | 220 | μA | |
| $I_{IL}$ | LOW level input current | | $T_A$ = −30°C | 0.5 | | | μA | Apply $V_{ILmin}$ to each input under test, one at a time, with $V_{IHmax}$ applied to all other inputs. |
| | | | $T_A$ = +25°C | 0.5 | | | μA | |
| | | | $T_A$ = +85°C | 0.3 | | | μA | |
| $-I_{EE}$ | $V_{EE}$ supply current | | $T_A$ = −30°C | | | 39 | mA | |
| | | | $T_A$ = +25°C | | 20 | 35 | mA | |
| | | | $T_A$ = +85°C | | | 39 | mA | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | | $T_A$ = +25°C | | 0.016 | | V/V | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | | 0.250 | | V/V | |
| $\frac{\Delta V_{BB}}{\Delta V_{EE}}$ | Reference bias voltage compensation | | | | 0.148 | | V/V | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst-case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 5.



**NOTES:**

| | |
|---|---|
| $V_{IHmax}$ | – Maximum HIGH level input voltage (the most positive $V_{IH}$). |
| $V_{IHT}$ | – HIGH level input threshold voltage. |
| $V_{ILT}$ | – LOW level input threshold voltage. |
| $V_{ILmin}$ | – Minimum LOW level input voltage (the most negative $V_{IL}$). |
| $V_{OHmax}$ | – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition. |
| $V_{OHmin}$ | – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition. |
| $V_{OHT}$ | – HIGH level output threshold voltage with the inputs set to their respective threshold levels. |
| $V_{OLT}$ | – LOW level output threshold voltage with the inputs set to their respective threshold levels. |
| $V_{OLmax}$ | – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions. |
| $V_{OLmin}$ | – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions. |
| $V_{BB}$ | – Reference bias voltage (the internally generated reference voltage which is used to set the input and output threshold level). |

Figure 5. Transfer Characteristics

## AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$

| PARAMETER | $T_A = -30°C$ | | $T_A = +25°C$ | | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Typ | Max | Min | Max | | |
| $t_{PLH}$ Propagation delay | 1.0 | 4.3 | 1.0 | 2.7 | 4.0 | 1.0 | 4.2 | ns | Figs. 6, 7, 8 |
| $t_{PHL}$ $D_n$ to $Q_n$, $\overline{Q}_3$ | 1.0 | 4.3 | 1.0 | 2.7 | 4.0 | 1.0 | 4.2 | ns | |
| $t_{TLH}$ Transition time | 1.5 | 3.7 | 1.5 | 2.0 | 3.5 | 1.5 | 3.6 | ns | Figs. 6, 7, 8 |
| $t_{THL}$ 20% to 80%, 80% to 20% | 1.5 | 3.7 | 1.5 | 2.0 | 3.5 | 1.5 | 3.6 | ns | |

## AC WAVEFORMS

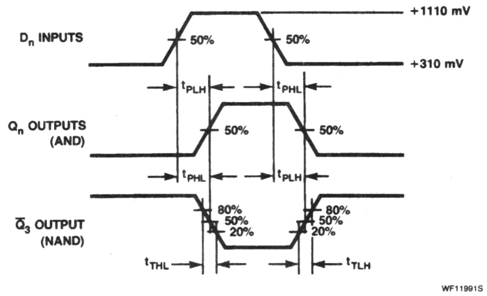
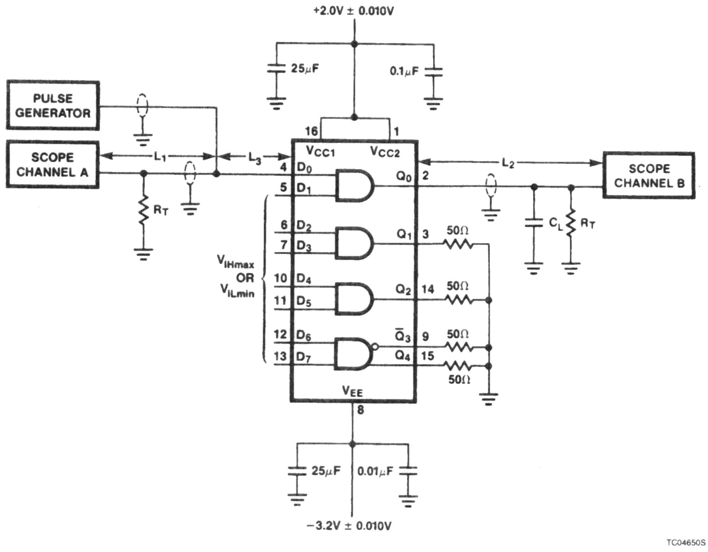


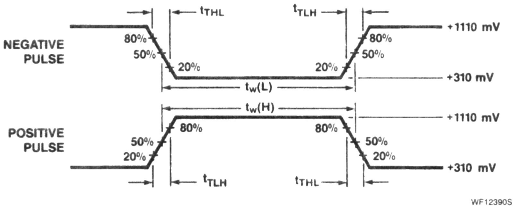
Figure 6. Propagation Delay and Transition Times

## TEST CIRCUITS AND WAVEFORMS


+2.0V ± 0.010V
25μF
0.1μF
PULSE GENERATOR
SCOPE CHANNEL A
L1
L3
L2
$R_T$
16
1
$V_{CC1}$
$V_{CC2}$
4 $D_0$
5 $D_1$
6 $D_2$
7 $D_3$
10 $D_4$
11 $D_5$
12 $D_6$
13 $D_7$
$Q_0$ 2
$Q_1$ 3
$Q_2$ 14
$\bar{Q}_3$ 9
$Q_4$ 15
50Ω
50Ω
50Ω
50Ω
$V_{IHmax}$ OR $V_{ILmin}$
$V_{EE}$
8
SCOPE CHANNEL B
$C_L$
$R_T$
25μF
0.01μF
−3.2V ± 0.010V
TC04650S

NOTES:
1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$
2. Decoupling 0.1μF and 25μF from GND to $V_{CC}$, 0.01μF and 25μF from GND to $V_{EE}$. (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance ≤ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.

Figure 7. AC Test Circuit for 10104


NEGATIVE PULSE
$t_{THL}$
$t_{TLH}$
80%
50%
20%
20%
80%
50%
+1110 mV
+310 mV
$t_w(L)$
$t_w(H)$
POSITIVE PULSE
80%
80%
50%
20%
50%
20%
+1110 mV
+310 mV
$t_{TLH}$
$t_{THL}$
WF12390S

**INPUT PULSE REQUIREMENTS**

**$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$, $V_T$ = GND (0V)**

| Family | Amplitude | Rep Rate | Pulse Width | $t_{TLH}$ | $t_{THL}$ |
|---|---|---|---|---|---|
| 10K ECL | 800mVp-p | 1MHz | 500ns | 2.0 ±0.2ns | 2.0 ±0.2ns |

Figure 8. Input Pulse Definition

**Signetics**

# 10105
## Gate

**Triple 2-3-2 Input OR/NOR Gate**
***Product Specification***

**ECL Products**

### DESCRIPTION

The 10105 is a Triple 2-3-2 Input OR/NOR Gate.

All unused inputs can be left open due to integrated pull-down resistors which avoid the need for a supply voltage.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 10105 | 2.0ns | 17mA |

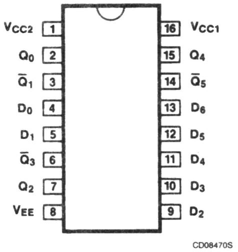
### ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} = GND$; $V_{EE} = -5.2V$<br>$T_A = -30°C$ to $+85°C$ |
|---|---|
| Plastic DIP | 10105N |
| Ceramic DIP | 10105F |

### PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_0$–$D_6$ | Data Inputs |
| $Q_0$, $Q_2$, $Q_4$ | Data Outputs (OR) |
| $\overline{Q}_1$, $\overline{Q}_3$, $\overline{Q}_5$ | Data Outputs (NOR) |

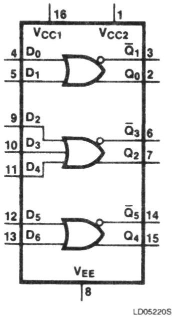
### PIN CONFIGURATION



$V_{CC2}$ 1
$Q_0$ 2
$\overline{Q}_1$ 3
$D_0$ 4
$D_1$ 5
$\overline{Q}_3$ 6
$Q_2$ 7
$V_{EE}$ 8
16 $V_{CC1}$
15 $Q_4$
14 $\overline{Q}_5$
13 $D_6$
12 $D_5$
11 $D_4$
10 $D_3$
9 $D_2$
CD08470S

Figure 1

### LOGIC SYMBOL

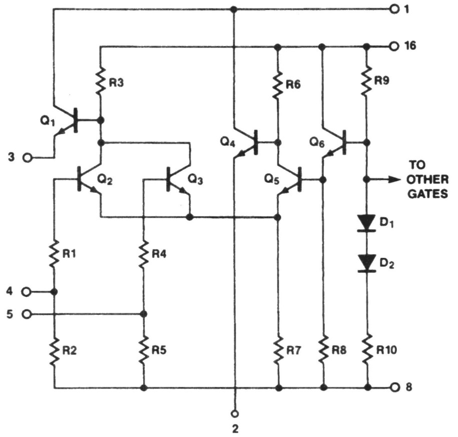


16
1
$V_{CC1}$
$V_{CC2}$
4 $D_0$
5 $D_1$
$\overline{Q}_1$ 3
$Q_0$ 2
9 $D_2$
10 $D_3$
11 $D_4$
$\overline{Q}_3$ 6
$Q_2$ 7
12 $D_5$
13 $D_6$
$\overline{Q}_5$ 14
$Q_4$ 15
$V_{EE}$
8
LD05220S

Figure 2

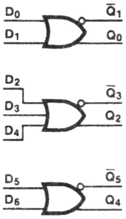
## Gate

## 10105


1
16
R3
R6
R9
Q1
Q4
Q6
3
Q2
Q3
Q5
TO OTHER GATES
D1
D2
R1
R4
4
5
R2
R5
R7
R8
R10
8
2

TC04270S

Figure 3. Circuit Diagram (One Gate)


D0
D1
$\overline{Q}_1$
Q0
D2
D3
D4
$\overline{Q}_3$
Q2
D5
D6
$\overline{Q}_5$
Q4

$Q_0 = D_0 + D_1$
$Q_2 = D_2 + D_3 + D_4$
$Q_4 = D_5 + D_6$
$Q_1 = \overline{D_0 + D_1}$
$Q_3 = \overline{D_2 + D_3 + D_4}$
$Q_5 = \overline{D_5 + D_6}$

**Positive logic:** HIGH state = 1
LOW state = 0

LD04661S

Figure 4. Logic Diagram

## Gate

## 10105

**ABSOLUTE MAXIMUM RATINGS** (Operation beyond the limits set forth in this table may impair useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | | 10K ECL | UNIT |
|---|---|---|---|---|
| $V_{EE}$ | Supply voltage | | −8.0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | | 0 to $V_{EE}$ | V |
| $I_O$ | Output current | | −50 | mA |
| $T_S$ | Storage temperature | | −55 to +150 | °C |
| $T_J$ | Maximum junction temperature | Ceramic package | +165 | °C |
| | | Plastic package | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | 10K ECL | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | −5.2 | | V |
| $V_{IH}$ | HIGH level input voltage | $T_A$ = −30°C | | | −890 | mV |
| | | $T_A$ = +25°C | | | −810 | mV |
| | | $T_A$ = +85°C | | | −700 | mV |
| $V_{IHT}$ | HIGH level input threshold voltage | $T_A$ = −30°C | −1205 | | | mV |
| | | $T_A$ = +25°C | −1105 | | | mV |
| | | $T_A$ = +85°C | −1035 | | | mV |
| $V_{ILT}$ | LOW level input threshold voltage | $T_A$ = −30°C | | | −1500 | mV |
| | | $T_A$ = +25°C | | | −1475 | mV |
| | | $T_A$ = +85°C | | | −1440 | mV |
| $V_{IL}$ | LOW level input voltage | $T_A$ = −30°C | −1890 | | | mV |
| | | $T_A$ = +25°C | −1850 | | | mV |
| | | $T_A$ = +85°C | −1825 | | | mV |
| $T_A$ | Operating ambient temperature | | −30 | +25 | +85 | °C |

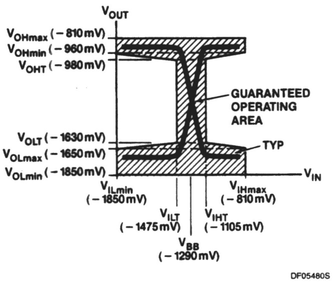
**NOTE:**
When operating at $V_{EE}$ other than specified voltage (−5.2V), the DC and AC Characteristics will vary slightly from specified values.
(See table of DC Characteristics)

**DC ELECTRICAL CHARACTERISTICS** $V_{CC1} = V_{CC2}$ = GND, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$, output loading with 50Ω to $-2.0V \pm 0.010V$ unless otherwise specified[1,3]

| PARAMETER | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | $T_A = -30°C$ | -1060 | | -890 | mV | For $Q_n$ outputs, apply $V_{IHmax}$ to all inputs.<br>For $\overline{Q}_n$ outputs, apply $V_{ILmin}$ to all inputs. |
| | | $T_A = +25°C$ | -960 | | -810 | mV | |
| | | $T_A = +85°C$ | -890 | | -700 | mV | |
| $V_{OHT}$ | HIGH level output threshold voltage | $T_A = -30°C$ | -1080 | | | mV | For $Q_n$ outputs, apply $V_{IHT}$ to each input, one at a time, with $V_{ILmin}$ applied to all other inputs.<br>For $\overline{Q}_n$ outputs, apply $V_{ILT}$ to each input, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | $T_A = +25°C$ | -980 | | | mV | |
| | | $T_A = +85°C$ | -910 | | | mV | |
| $V_{OLT}$ | LOW level output threshold voltage | $T_A = -30°C$ | | | -1655 | mV | For $Q_n$ outputs, apply $V_{ILT}$ to each input, one at a time, with $V_{ILmin}$ applied to all other inputs.<br>For $\overline{Q}_n$ outputs, apply $V_{IHT}$ to each input, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | $T_A = +25°C$ | | | -1630 | mV | |
| | | $T_A = +85°C$ | | | -1595 | mV | |
| $V_{OL}$ | LOW level output voltage | $T_A = -30°C$ | -1890 | | -1675 | mV | For $Q_n$ outputs, apply $V_{ILmin}$ to all inputs.<br>For $\overline{Q}_n$ outputs, apply $V_{IHmax}$ to all inputs. |
| | | $T_A = +25°C$ | -1850 | | -1650 | mV | |
| | | $T_A = +85°C$ | -1825 | | -1615 | mV | |
| $I_{IH}$ | HIGH level input current | $T_A = -30°C$ | | | 425 | µA | Apply $V_{IHmax}$ to each input under test, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | $T_A = +25°C$ | | | 265 | µA | |
| | | $T_A = +85°C$ | | | 265 | µA | |
| $I_{IL}$ | LOW level input current | $T_A = -30°C$ | 0.5 | | | µA | Apply $V_{ILmin}$ to each input under test, one at a time, with $V_{IHmax}$ applied to all other inputs. |
| | | $T_A = +25°C$ | 0.5 | | | µA | |
| | | $T_A = +85°C$ | 0.3 | | | µA | |
| $-I_{EE}$ | $V_{EE}$ supply current | $T_A = -30°C$ | | | 23 | mA | |
| | | $T_A = +25°C$ | | 17 | 21 | mA | |
| | | $T_A = +85°C$ | | | 23 | mA | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | $T_A = +25°C$ | | 0.016 | | V/V | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | 0.250 | | V/V | |
| $\frac{\Delta V_{BB}}{\Delta V_{EE}}$ | Reference bias voltage compensation | | | 0.148 | | V/V | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst-case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 5.



**NOTES:**

$V_{IHmax}$ – Maximum HIGH level input voltage (the most positive $V_{IH}$).
$V_{IHT}$ – HIGH level input threshold voltage.
$V_{ILT}$ – LOW level input threshold voltage.
$V_{ILmin}$ – Minimum LOW level input voltage (the most negative $V_{IL}$).
$V_{OHmax}$ – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition.
$V_{OHmin}$ – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition.
$V_{OHT}$ – HIGH level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLT}$ – LOW level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLmax}$ – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions.
$V_{OLmin}$ – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions.
$V_{BB}$ – Reference bias voltage (the internally generated reference voltage which is used to set the input and output threshold level).

**Figure 5. Transfer Characteristics**

## AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$

| PARAMETER | $T_A = -30°C$ |  | $T_A = +25°C$ |  |  | $T_A = +85°C$ |  | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
|  | Min | Max | Min | Typ | Max | Min | Max |  |  |
| $t_{PLH}$ Propagation delay | 1.0 | 3.1 | 1.0 | 2.0 | 2.9 | 1.0 | 3.3 | ns | Figs. 6, 7, 8 |
| $t_{PHL}$ $D_n$ to $Q_n$, $\overline{Q}_n$ | 1.0 | 3.1 | 1.0 | 2.0 | 2.9 | 1.0 | 3.3 | ns |  |
| $t_{TLH}$ Transition time | 1.1 | 3.6 | 1.1 | 2.0 | 3.3 | 1.1 | 3.7 | ns | Figs. 6, 7, 8 |
| $t_{THL}$ 20% to 80%, 80% to 20% | 1.1 | 3.6 | 1.1 | 2.0 | 3.3 | 1.1 | 3.7 | ns |  |

## AC WAVEFORMS

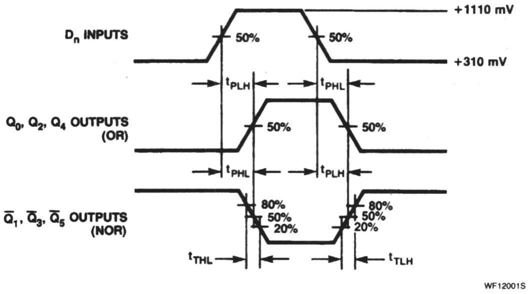
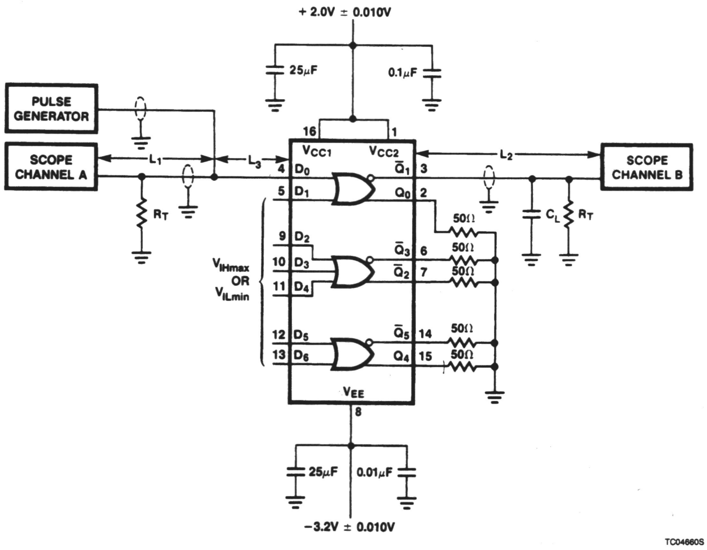


**Figure 6. Propagation Delay and Transition Times**

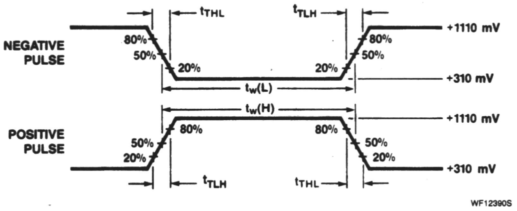
## TEST CIRCUITS AND WAVEFORMS


+2.0V ± 0.010V
25µF
0.1µF
PULSE GENERATOR
SCOPE CHANNEL A
L1
L3
RT
16
1
VCC1
VCC2
4 D0
5 D1
9 D2
10 D3
11 D4
12 D5
13 D6
Q̄1 3
Q0 2
Q̄3 6
Q̄2 7
Q̄5 14
Q4 15
VEE
8
VIHmax OR VILmin
50Ω
50Ω
50Ω
50Ω
50Ω
L2
CL
RT
SCOPE CHANNEL B
25µF
0.01µF
-3.2V ± 0.010V
TC04660S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$
2. Decoupling 0.1µF and 25µF from GND to $V_{CC}$, 0.01µF and 25µF from GND to $V_{EE}$. (0.01 and 0.1µF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T = 50\Omega$ terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance $\leqslant 3pF$.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ±1% or better.

**Figure 7. AC Test Circuit for 10105**


NEGATIVE PULSE
POSITIVE PULSE
tTHL
tTLH
80%
50%
20%
20%
80%
50%
+1110 mV
+310 mV
tw(L)
tw(H)
80%
80%
50%
20%
50%
20%
+1110 mV
+310 mV
tTLH
tTHL
WF12390S

| INPUT PULSE REQUIREMENTS<br>$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$, $V_T$ = GND (0V) | | | | | |
|---|---|---|---|---|---|
| Family | Amplitude | Rep Rate | Pulse Width | $t_{TLH}$ | $t_{THL}$ |
| 10K ECL | 800mVp-p | 1MHz | 500ns | 2.0 ±0.2ns | 2.0 ±0.2ns |

**Figure 8. Input Pulse Definition**

**Signetics**

**ECL Products**

# 10106
## Gate

**Triple 4-3-3 Input NOR Gate**
***Product Specification***

## DESCRIPTION

The 10106 is a Triple 4-3-3 Input NOR Gate. All unused inputs can be left open due to integrated pull-down resistors which avoid the need for a supply voltage.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 10106 | 2.0ns | 17mA |

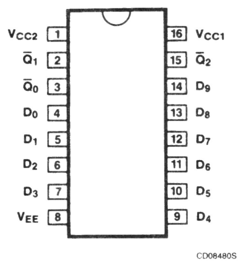
## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} = GND$; $V_{EE} = -5.2V$<br>$T_A = -30°C$ to $+85°C$ |
|---|---|
| Plastic DIP | 10106N |
| Ceramic DIP | 10106F |

## PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_0 - D_9$ | Data Inputs |
| $\overline{Q}_0 - \overline{Q}_2$ | Data Outputs |

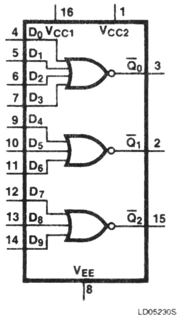
## PIN CONFIGURATION



$V_{CC2}$ 1
$\overline{Q}_1$ 2
$\overline{Q}_0$ 3
$D_0$ 4
$D_1$ 5
$D_2$ 6
$D_3$ 7
$V_{EE}$ 8
16 $V_{CC1}$
15 $\overline{Q}_2$
14 $D_9$
13 $D_8$
12 $D_7$
11 $D_6$
10 $D_5$
9 $D_4$
CD08480S

Figure 1

## LOGIC SYMBOL

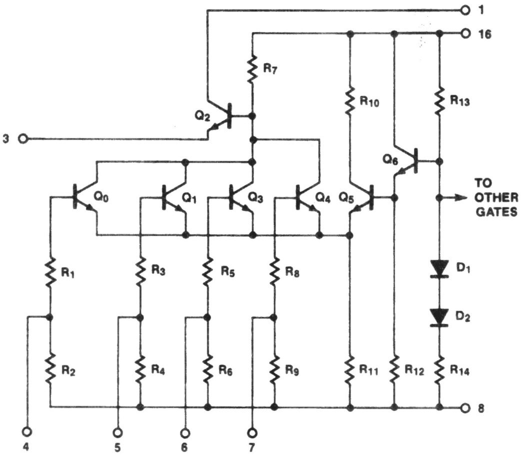


16
1
$V_{CC1}$
$V_{CC2}$
4 $D_0$
5 $D_1$
6 $D_2$
7 $D_3$
9 $D_4$
10 $D_5$
11 $D_6$
12 $D_7$
13 $D_8$
14 $D_9$
$\overline{Q}_0$ 3
$\overline{Q}_1$ 2
$\overline{Q}_2$ 15
$V_{EE}$
8
LD05230S

Figure 2

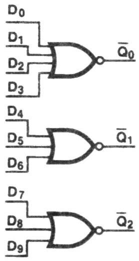
# Gate

# 10106


1
16
R7
R10
R13
Q2
3
Q6
TO OTHER GATES
Q0
Q1
Q3
Q4
Q5
R1
R3
R5
R8
D1
D2
R2
R4
R6
R9
R11
R12
R14
8
4
5
6
7

TC04310S

**Figure 3. Circuit Diagram (One Gate)**


D0
D1
D2
D3
$\overline{Q}_0$
D4
D5
D6
$\overline{Q}_1$
D7
D8
D9
$\overline{Q}_2$

$Q_0 = \overline{D_0 + D_1 + D_2 + D_3}$

$Q_1 = \overline{D_4 + D_5 + D_6}$

$Q_2 = \overline{D_7 + D_8 + D_9}$

**Positive Logic: HIGH state = 1**
**LOW state = 0**

LD04671S

**Figure 4. Logic Diagram**

# Gate

# 10106

**ABSOLUTE MAXIMUM RATINGS** (Operation beyond the limits set forth in this table may impair useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | | 10K ECL | UNIT |
|---|---|---|---|---|
| $V_{EE}$ | Supply voltage | | -8.0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | | 0 to $V_{EE}$ | V |
| $I_O$ | Output current | | -50 | mA |
| $T_S$ | Storage temperature | | -55 to +150 | °C |
| $T_J$ | Maximum junction temperature | Ceramic package | +165 | °C |
| | | Plastic package | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | 10K ECL | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | -5.2 | | V |
| $V_{IH}$ | HIGH level input voltage | $T_A$ = -30°C | | | -890 | mV |
| | | $T_A$ = +25°C | | | -810 | mV |
| | | $T_A$ = +85°C | | | -700 | mV |
| $V_{IHT}$ | HIGH level input threshold voltage | $T_A$ = -30°C | -1205 | | | mV |
| | | $T_A$ = +25°C | -1105 | | | mV |
| | | $T_A$ = +85°C | -1035 | | | mV |
| $V_{ILT}$ | LOW level input threshold voltage | $T_A$ = -30°C | | | -1500 | mV |
| | | $T_A$ = +25°C | | | -1475 | mV |
| | | $T_A$ = +85°C | | | -1440 | mV |
| $V_{IL}$ | LOW level input voltage | $T_A$ = -30°C | -1890 | | | mV |
| | | $T_A$ = +25°C | -1850 | | | mV |
| | | $T_A$ = +85°C | -1825 | | | mV |
| $T_A$ | Operating ambient temperature | | -30 | +25 | +85 | °C |

**NOTE:**
When operating at $V_{EE}$ other than specified voltage (-5.2V), the DC and AC Characteristics will vary slightly from specified values. (See table of DC Characteristics)

**DC ELECTRICAL CHARACTERISTICS** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$, output loading with 50Ω to −2.0V ±0.010V unless otherwise specified[1,3]

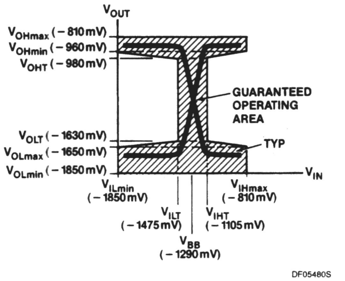
| PARAMETER | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | $T_A = -30°C$ | −1060 | | −890 | mV | Apply $V_{Imin}$ to all inputs. |
| | | $T_A = +25°C$ | −960 | | −810 | mV | |
| | | $T_A = +85°C$ | −890 | | −700 | mV | |
| $V_{OHT}$ | HIGH level output threshold voltage | $T_A = -30°C$ | −1080 | | | mV | Apply $V_{ILT}$ to each input, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | $T_A = +25°C$ | −980 | | | mV | |
| | | $T_A = +85°C$ | −910 | | | mV | |
| $V_{OLT}$ | LOW level output threshold voltage | $T_A = -30°C$ | | | −1655 | mV | Apply $V_{IHT}$ to each input, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | $T_A = +25°C$ | | | −1630 | mV | |
| | | $T_A = +85°C$ | | | −1595 | mV | |
| $V_{OL}$ | LOW level output voltage | $T_A = -30°C$ | −1890 | | −1675 | mV | Apply $V_{IHmax}$ to all inputs. |
| | | $T_A = +25°C$ | −1850 | | −1650 | mV | |
| | | $T_A = +85°C$ | −1825 | | −1615 | mV | |
| $I_{IH}$ | HIGH level input current | $T_A = -30°C$ | | | 425 | μA | Apply $V_{IHmax}$ to each input under test, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | $T_A = +25°C$ | | | 265 | μA | |
| | | $T_A = +85°C$ | | | 265 | μA | |
| $I_{IL}$ | LOW level input current | $T_A = -30°C$ | 0.5 | | | μA | Apply $V_{ILmin}$ to each input under test, one at a time, with $V_{IHmax}$ applied to all other inputs. |
| | | $T_A = +25°C$ | 0.5 | | | μA | |
| | | $T_A = +85°C$ | 0.3 | | | μA | |
| $-I_{EE}$ | $V_{EE}$ supply current | $T_A = -30°C$ | | | 23 | mA | |
| | | $T_A = +25°C$ | | 17 | 21 | mA | |
| | | $T_A = +85°C$ | | | 23 | mA | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | $T_A = +25°C$ | | 0.016 | | V/V | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | 0.250 | | V/V | |
| $\frac{\Delta V_{BB}}{\Delta V_{EE}}$ | Reference bias voltage compensation | | | 0.148 | | V/V | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst-case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 5.

## Gate

## 10106


$V_{OUT}$
$V_{OHmax}$ (−810mV)
$V_{OHmin}$ (−960mV)
$V_{OHT}$ (−980mV)
GUARANTEED OPERATING AREA
$V_{OLT}$ (−1630mV)
$V_{OLmax}$ (−1650mV)
$V_{OLmin}$ (−1850mV)
TYP
$V_{IN}$
$V_{ILmin}$ (−1850mV)
$V_{IHmax}$ (−810mV)
$V_{ILT}$ (−1475mV)
$V_{IHT}$ (−1105mV)
$V_{BB}$ (−1290mV)
DF05480S

**NOTES:**

$V_{IHmax}$ – Maximum HIGH level input voltage (the most positive $V_{IH}$).
$V_{IHT}$ – HIGH level input threshold voltage.
$V_{ILT}$ – LOW level input threshold voltage.
$V_{ILmin}$ – Minimum LOW level input voltage (the most negative $V_{IL}$).
$V_{OHmax}$ – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition.
$V_{OHmin}$ – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition.
$V_{OHT}$ – HIGH level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLT}$ – LOW level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLmax}$ – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions.
$V_{OLmin}$ – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions.
$V_{BB}$ – Reference bias voltage (the internally generated reference voltage which is used to set the input and output threshold level).

**Figure 5. Transfer Characteristics**

## AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2 \pm 0.010V$

| PARAMETER | $T_A = -30°C$ | | $T_A = +25°C$ | | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Typ | Max | Min | Max | | |
| $t_{PLH}$ Propagation delay<br>$t_{PHL}$ $D_n$ to $\overline{Q}_n$ | 1.0<br>1.0 | 3.1<br>3.1 | 1.0<br>1.0 | 2.0<br>2.0 | 2.9<br>2.9 | 1.0<br>1.0 | 3.3<br>3.3 | ns<br>ns | Figs. 6, 7, 8 |
| $t_{TLH}$ Transition time<br>$t_{THL}$ 20% to 80%, 80% to 20% | 1.1<br>1.1 | 3.6<br>3.6 | 1.1<br>1.1 | 2.0<br>2.0 | 3.3<br>3.3 | 1.1<br>1.1 | 3.7<br>3.7 | ns<br>ns | Figs. 6, 7, 8 |

## AC WAVEFORMS

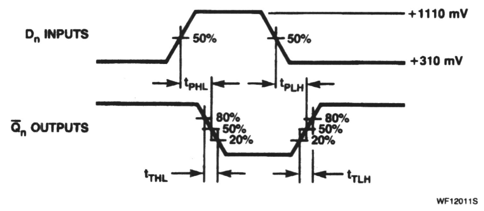
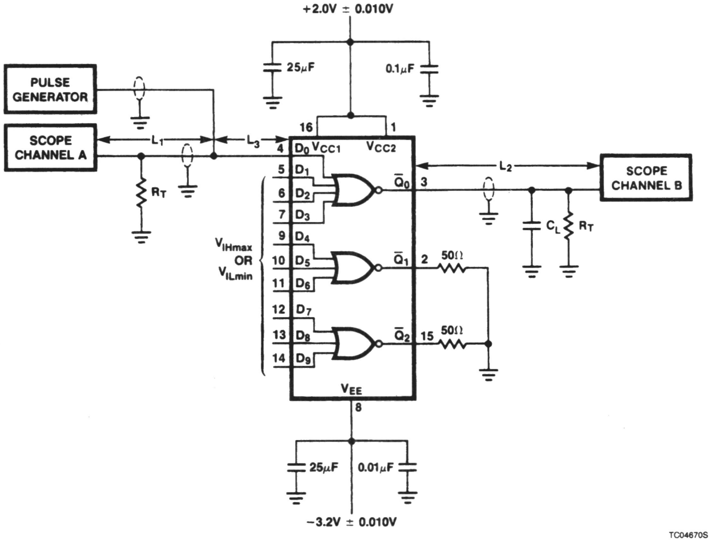

$D_n$ INPUTS
50%
50%
+1110 mV
+310 mV
$t_{PHL}$
$t_{PLH}$
$\overline{Q}_n$ OUTPUTS
80%
50%
20%
80%
50%
20%
$t_{THL}$
$t_{TLH}$
WF12011S

**Figure 6. Propagation Delay and Transition Times**

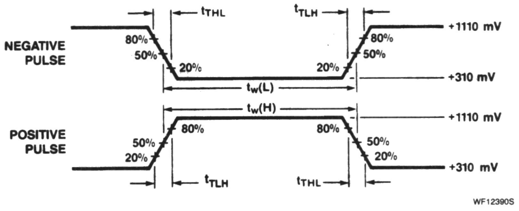
## TEST CIRCUITS AND WAVEFORMS


+2.0V ± 0.010V
25μF
0.1μF
PULSE GENERATOR
SCOPE CHANNEL A
L1
L3
RT
16
1
4 D0 VCC1
VCC2
5 D1
6 D2
7 D3
9 D4
10 D5
11 D6
12 D7
13 D8
14 D9
VIHmax OR VILmin
Q̄0 3
Q̄1 2
Q̄2 15
50Ω
50Ω
L2
SCOPE CHANNEL B
CL
RT
VEE
8
25μF
0.01μF
−3.2V ± 0.010V
TC04670S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$
2. Decoupling 0.1μF and 25μF from GND to $V_{CC}$, 0.01μF and 25μF from GND to $V_{EE}$. (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance $\leq$ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.

Figure 7. AC Test Circuit for 10106


NEGATIVE PULSE
POSITIVE PULSE
tTHL
tTLH
80%
50%
20%
tw(L)
tw(H)
+1110 mV
+310 mV
+1110 mV
+310 mV
WF12390S

**INPUT PULSE REQUIREMENTS**

**$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$, $V_T$ = GND (0V)**

| Family | Amplitude | Rep Rate | Pulse Width | $t_{TLH}$ | $t_{THL}$ |
|---|---|---|---|---|---|
| 10K ECL | 800mVp-p | 1MHz | 500ns | 2.0 ±0.2ns | 2.0 ±0.2ns |

Figure 8. Input Pulse Definition

**Signetics**

**ECL Products**

# 10107
## Gate

**Triple 2-Input Exclusive-OR/Exclusive-NOR Gate**
***Product Specification***

## DESCRIPTION

The 10107 is a three gate array designed to provide the positive Exclusive-OR and NOR functions. All unused inputs can be left open due to pull-down resistors which avoid the need for a supply voltage.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 10107 | 2.8 ns | 22mA |

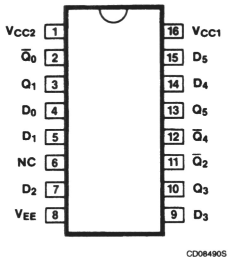
## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} = GND$; $V_{EE} = -5.2V$<br>$T_A = -30°C$ to $+85°C$ |
|---|---|
| Plastic DIP | 10107N |
| Ceramic DIP | 10107F |

## PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_0 - D_5$ | Data Inputs |
| $Q_1, Q_3, Q_5$ | Data Outputs (OR) |
| $\overline{Q}_0, \overline{Q}_2, \overline{Q}_4$ | Data Outputs (NOR) |

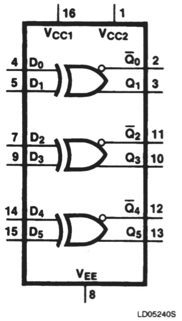
## PIN CONFIGURATION



$V_{CC2}$ 1
$\overline{Q}_0$ 2
$Q_1$ 3
$D_0$ 4
$D_1$ 5
NC 6
$D_2$ 7
$V_{EE}$ 8
16 $V_{CC1}$
15 $D_5$
14 $D_4$
13 $Q_5$
12 $\overline{Q}_4$
11 $\overline{Q}_2$
10 $Q_3$
9 $D_3$
CD08490S

Figure 1

## LOGIC SYMBOL



16
1
$V_{CC1}$
$V_{CC2}$
4 $D_0$
5 $D_1$
$\overline{Q}_0$ 2
$Q_1$ 3
7 $D_2$
9 $D_3$
$\overline{Q}_2$ 11
$Q_3$ 10
14 $D_4$
15 $D_5$
$\overline{Q}_4$ 12
$Q_5$ 13
$V_{EE}$
8
LD05240S

Figure 2

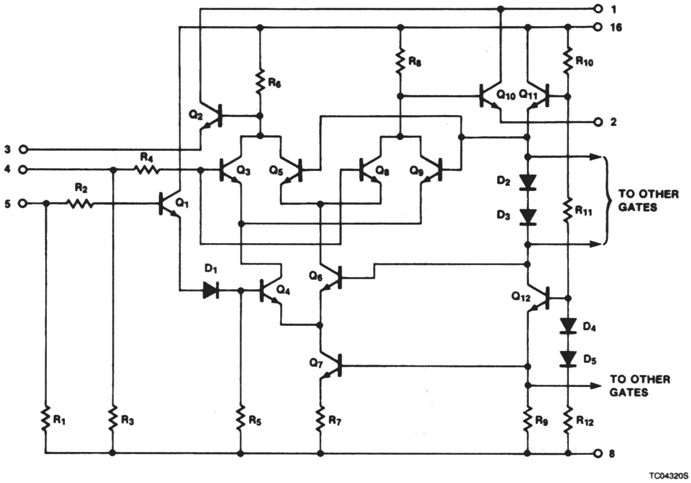
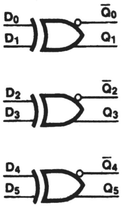

1
16
2
3
4
5
8
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
D1
D2
D3
D4
D5
TO OTHER GATES
TO OTHER GATES
TC04320S

Figure 3. Circuit Diagram (One Gate)


D0
D1
$\overline{Q}_0$
Q1
D2
D3
$\overline{Q}_2$
Q3
D4
D5
$\overline{Q}_4$
Q5

$Q_0 = \overline{D}_0 \bullet \overline{D}_1 + D_0 \bullet D_1$

$Q_1 = D_0 \bullet \overline{D}_1 + \overline{D}_0 \bullet D_1$

$Q_2 = \overline{D}_2 \bullet \overline{D}_3 + D_2 \bullet D_3$

$Q_3 = D_2 \bullet \overline{D}_3 + \overline{D}_2 \bullet D_3$

$Q_4 = \overline{D}_4 \bullet \overline{D}_5 + D_4 \bullet D_5$

$Q_5 = D_4 \bullet \overline{D}_5 + \overline{D}_4 \bullet D_5$

**Positive Logic:** HIGH state = 1
LOW state = 0

LD04681S

Figure 4. Logic Diagram

## ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | | 10K ECL | UNIT |
|---|---|---|---|---|
| $V_{EE}$ | Supply voltage | | -8.0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | | 0 to $V_{EE}$ | V |
| $I_O$ | Output current | | -50 | mA |
| $T_S$ | Storage temperature | | -55 to +150 | °C |
| $T_J$ | Maximum junction temperature | Ceramic package | +165 | °C |
| | | Plastic package | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | 10K ECL | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | -5.2 | | V |
| $V_{IH}$ | HIGH level input voltage | $T_A = -30°C$ | | | -890 | mV |
| | | $T_A = +25°C$ | | | -810 | mV |
| | | $T_A = +85°C$ | | | -700 | mV |
| $V_{IHT}$ | HIGH level input threshold voltage | $T_A = -30°C$ | -1205 | | | mV |
| | | $T_A = +25°C$ | -1105 | | | mV |
| | | $T_A = +85°C$ | -1035 | | | mV |
| $V_{ILT}$ | LOW level input threshold voltage | $T_A = -30°C$ | | | -1500 | mV |
| | | $T_A = +25°C$ | | | -1475 | mV |
| | | $T_A = +85°C$ | | | -1440 | mV |
| $V_{IL}$ | LOW level input voltage | $T_A = -30°C$ | -1890 | | | mV |
| | | $T_A = +25°C$ | -1850 | | | mV |
| | | $T_A = +85°C$ | -1825 | | | mV |
| $T_A$ | Operating ambient temperature | | -30 | +25 | +85 | °C |

**NOTE:**
When operating at $V_{EE}$ other than specified voltage (-5.2V), the DC and AC Characteristics will vary slightly from specified values.
(See table of DC Characteristics)

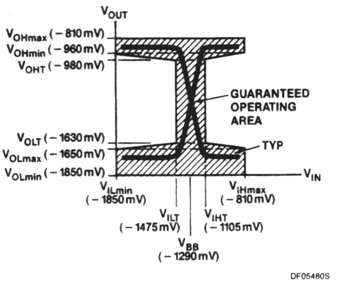
6

**DC ELECTRICAL CHARACTERISTICS** $V_{CC1} = V_{CC2} = \text{GND}$, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$, output loading with 50Ω to −2.0V ±0.010V unless otherwise specified[1,3]

| PARAMETER | | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | | $T_A = -30°C$ | −1060 | | −890 | mV | For $\overline{Q}_n$ outputs, apply $V_{ILmin}$ to all inputs.<br>For $Q_n$ outputs, apply $V_{IHmax}$ to each input ($D_1$, $D_2$, $D_5$), one at a time, with $V_{ILmin}$ applied to all other inputs.<br>For $Q_n$ outputs apply $V_{IHmax}$ to each input ($D_0$, $D_3$, $D_4$), one at a time, with $V_{ILmin}$ applied to all other inputs.<br>For $\overline{Q}_n$ outputs, apply $V_{IHmax}$ to all inputs. |
| | | | $T_A = +25°C$ | −960 | | −810 | mV | |
| | | | $T_A = +85°C$ | −890 | | −700 | mV | |
| $V_{OHT}$ | HIGH level output threshold voltage | | $T_A = -30°C$ | −1080 | | | mV | For $Q_n$ outputs, apply $V_{IHT}$ to one gate input with $V_{ILmin}$ applied to the other gate input.<br>For $\overline{Q}_n$ outputs, apply $V_{IHT}$ to one gate input with $V_{ILmax}$ applied to the other gate input. |
| | | | $T_A = +25°C$ | −980 | | | mV | |
| | | | $T_A = +85°C$ | −910 | | | mV | |
| $V_{OLT}$ | LOW level output threshold voltage | | $T_A = -30°C$ | | | −1655 | mV | For $Q_n$ outputs, apply $V_{ILT}$ to one gate input with $V_{ILmin}$ applied to the other gate input.<br>For $\overline{Q}_n$ outputs, apply $V_{IHT}$ to one gate input with $V_{ILmin}$ applied to the other gate input. |
| | | | $T_A = +25°C$ | | | −1630 | mV | |
| | | | $T_A = +85°C$ | | | −1595 | mV | |
| $V_{OL}$ | LOW level output voltage | | $T_A = -30°C$ | −1890 | | −1675 | mV | For $Q_n$ outputs, apply $V_{ILmin}$ to all inputs.<br>For $\overline{Q}_n$ outputs, apply $V_{IHmax}$ to each input ($D_1$, $D_2$, $D_5$), one at a time, with $V_{ILmin}$ applied to all other inputs.<br>For $\overline{Q}_n$ outputs apply $V_{IHmax}$ to each input ($D_0$, $D_3$, $D_4$), one at a time, with $V_{ILmin}$ applied to all other inputs.<br>For $Q_n$ outputs, apply $V_{IHmax}$ to all inputs. |
| | | | $T_A = +25°C$ | −1850 | | −1650 | mV | |
| | | | $T_A = +85°C$ | −1825 | | −1615 | mV | |
| $I_{IH}$ | HIGH level input current | $D_0$, $D_3$, $D_4$ Inputs | $T_A = -30°C$ | | | 425 | μA | Apply $V_{IHmax}$ to each input under test, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = -25°C$ | | | 265 | μA | |
| | | | $T_A = +25°C$ | | | 265 | μA | |
| | | $D_1$, $D_2$, $D_5$ Inputs | $T_A = +30°C$ | | | 350 | μA | Apply $V_{IHmax}$ to each input under test, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | | | 220 | μA | |
| | | | $T_A = +85°C$ | | | 220 | μA | |
| $I_{IL}$ | LOW level input current | | $T_A = -30°C$ | 0.5 | | | μA | Apply $V_{ILmin}$ to each input under test, one at a time, with $V_{IHmax}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | 0.5 | | | μA | |
| | | | $T_A = +85°C$ | 0.3 | | | μA | |
| $-I_{EE}$ | $V_{EE}$ supply current | | $T_A = -30°C$ | | | 31 | mA | Apply $V_{IHmax}$ to $D_1$, $D_2$, $D_5$. |
| | | | $T_A = +25°C$ | | | 28 | mA | |
| | | | $T_A = +85°C$ | | | 31 | mA | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | | $T_A = +25°C$ | | 0.016 | | V/V | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | | 0.250 | | V/V | |
| $\frac{\Delta V_{BB}}{\Delta V_{EE}}$ | Reference bias voltage compensation | | | | 0.148 | | V/V | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst-case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 5.



$V_{OUT}$
$V_{OHmax}$ (−810mV)
$V_{OHmin}$ (−960mV)
$V_{OHT}$ (−980mV)
GUARANTEED OPERATING AREA
$V_{OLT}$ (−1630mV)
$V_{OLmax}$ (−1650mV)
$V_{OLmin}$ (−1850mV)
TYP
$V_{IN}$
$V_{ILmin}$ (−1850mV)
$V_{IHmax}$ (−810mV)
$V_{ILT}$ (−1475mV)
$V_{IHT}$ (−1105mV)
$V_{BB}$ (−1290mV)
DF05480S

**NOTES:**

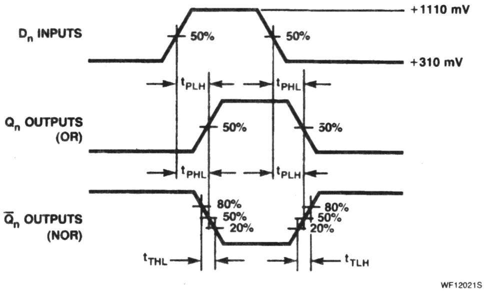
$V_{IHmax}$ – Maximum HIGH level input voltage (the most positive $V_{IH}$).
$V_{IHT}$ – HIGH level input threshold voltage.
$V_{ILT}$ – LOW level input threshold voltage.
$V_{ILmin}$ – Minimum LOW level input voltage (the most negative $V_{IL}$).
$V_{OHmax}$ – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition.
$V_{OHmin}$ – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition.
$V_{OHT}$ – HIGH level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLT}$ – LOW level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLmax}$ – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions.
$V_{OLmin}$ – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions.
$V_{BB}$ – Reference bias voltage (the internally generated reference voltage which is used to set the input and output threshold level).

**Figure 5. Transfer Characteristics**

## AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$

| PARAMETER | $T_A = -30°C$ | | $T_A = +25°C$ | | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Typ | Max | Min | Max | | |
| $t_{PLH}$ Propagation delay | 1.1 | 3.8 | 1.1 | 2.8 | 3.7 | 1.1 | 4.0 | ns | Figs. 6, 7, 8 |
| $t_{PHL}$ $D_n$ to $Q_n$, $\overline{Q}_n$ | 1.1 | 3.8 | 1.1 | 2.8 | 3.7 | 1.1 | 4.0 | ns | |
| $t_{TLH}$ Transition time | 1.1 | 3.5 | 1.1 | 2.5 | 3.5 | 1.1 | 3.8 | ns | Figs. 6, 7, 8 |
| $t_{THL}$ 20% to 80%, 80% to 20% | 1.1 | 3.5 | 1.1 | 2.5 | 3.5 | 1.1 | 3.8 | ns | |

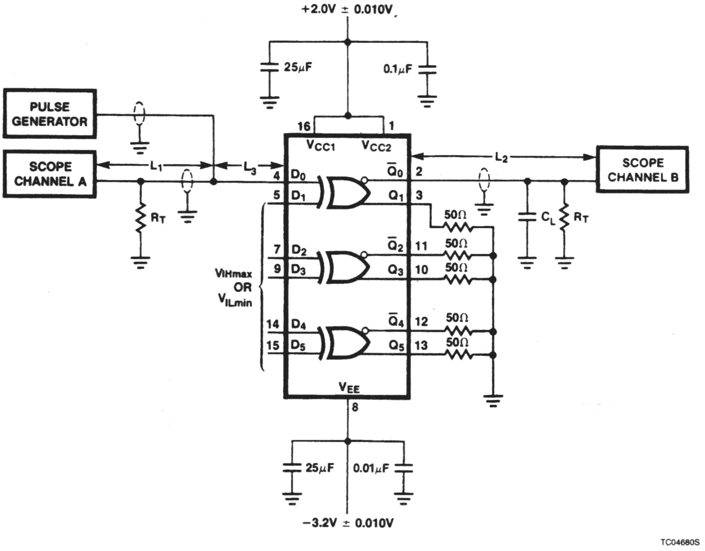
## AC WAVEFORMS



$D_n$ INPUTS
50%
50%
+1110 mV
+310 mV
$t_{PLH}$
$t_{PHL}$
$Q_n$ OUTPUTS (OR)
50%
50%
$t_{PHL}$
$t_{PLH}$
$\overline{Q}_n$ OUTPUTS (NOR)
80%
50%
20%
80%
50%
20%
$t_{THL}$
$t_{TLH}$
WF12021S

**Figure 6. Propagation Delay and Transition Times**

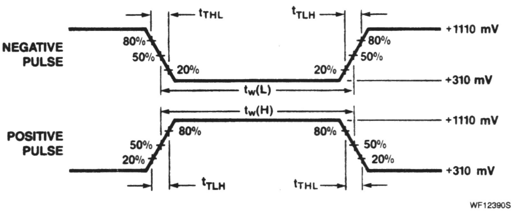
## TEST CIRCUITS AND WAVEFORMS


+2.0V ± 0.010V
25µF
0.1µF
PULSE GENERATOR
SCOPE CHANNEL A
L1
L3
RT
16
1
VCC1
VCC2
4 D0
5 D1
7 D2
9 D3
14 D4
15 D5
Q̄0 2
Q1 3
Q̄2 11
Q3 10
Q̄4 12
Q5 13
50Ω
VIHmax OR VILmin
VEE
8
L2
SCOPE CHANNEL B
CL
RT
25µF
0.01µF
−3.2V ± 0.010V
TC04680S

NOTES:

1. $V_{CC1} = V_{CC2} = +2V$ ± 0.010V, $V_{EE} = -3.2V$ ± 0.010V
2. Decoupling 0.1µF and 25µF from GND to $V_{CC}$, 0.01µF and 25µF from GND to $V_{EE}$. (0.01 and 0.1µF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance ⩽ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.

Figure 7. AC Test Circuit for 10107


NEGATIVE PULSE
POSITIVE PULSE
tTHL
tTLH
80%
50%
20%
tw(L)
tw(H)
+1110 mV
+310 mV
WF12390S

| INPUT PULSE REQUIREMENTS<br>$V_{CC1} = V_{CC2} = +2.0V$ ±0.010V, $V_{EE} = -3.2V$ ±0.010V, $V_T$ = GND (0V) | | | | | |
|---|---|---|---|---|---|
| **Family** | **Amplitude** | **Rep Rate** | **Pulse Width** | **$t_{TLH}$** | **$t_{THL}$** |
| 10K ECL | 800mVp-p | 1MHz | 500ns | 2.0 ±0.2ns | 2.0 ±0.2ns |

Figure 8. Input Pulse Definition

# 10108
## Gate

**Dual 4-Input AND/NAND Gate**
***Product Specification***

**ECL Products**

### DESCRIPTION

The 10108 is a Dual AND/NAND Gate. All unused inputs can be left open due to integrated pull-down resistors which avoid the need for a supply voltage.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 10108 | AND output 2.3ns | 28mA |
| | NAND output 2.8ns | |

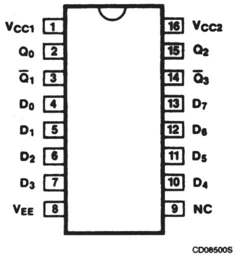
### ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} = \text{GND}$; $V_{EE} = -5.2\text{V}$<br>$T_A = -30°\text{C}$ to $+85°\text{C}$ |
|---|---|
| Plastic DIP | 10108N |
| Ceramic DIP | 10108F |

### PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_0 - D_7$ | Data Inputs |
| $Q_0$, $Q_2$ | Data Outputs (AND) |
| $\overline{Q}_1$, $\overline{Q}_3$ | Data Outputs (NAND) |

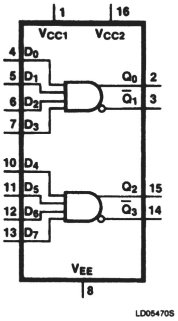
### PIN CONFIGURATION



$V_{CC1}$ 1
$Q_0$ 2
$\overline{Q}_1$ 3
$D_0$ 4
$D_1$ 5
$D_2$ 6
$D_3$ 7
$V_{EE}$ 8
16 $V_{CC2}$
15 $Q_2$
14 $\overline{Q}_3$
13 $D_7$
12 $D_6$
11 $D_5$
10 $D_4$
9 NC
CD08500S

Figure 1

### LOGIC SYMBOL



1
16
$V_{CC1}$
$V_{CC2}$
4 $D_0$
5 $D_1$
6 $D_2$
7 $D_3$
$Q_0$ 2
$\overline{Q}_1$ 3
10 $D_4$
11 $D_5$
12 $D_6$
13 $D_7$
$Q_2$ 15
$\overline{Q}_3$ 14
$V_{EE}$
8
LD05470S

Figure 2

# Gate

# 10108

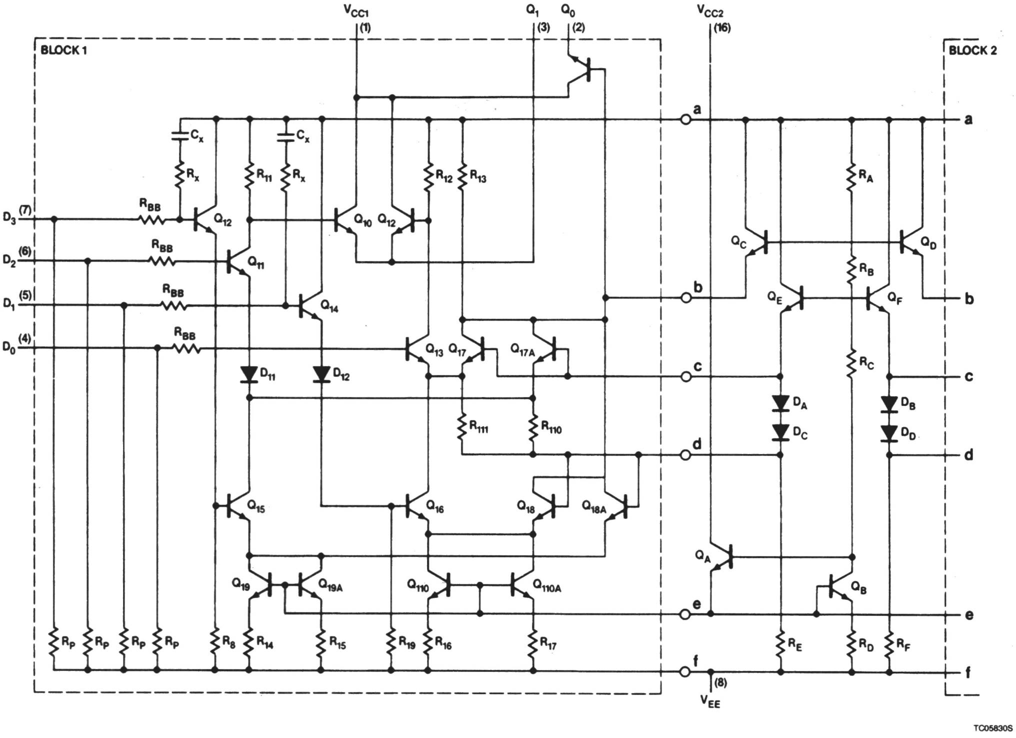
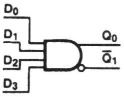

$V_{CC1}$
(1)
$Q_1$
(3)
$Q_0$
(2)
$V_{CC2}$
(16)
BLOCK 1
BLOCK 2
$D_3$ (7)
$D_2$ (6)
$D_1$ (5)
$D_0$ (4)
$R_{BB}$
$C_x$
$R_x$
$R_{11}$
$R_{12}$
$R_{13}$
$Q_{12}$
$Q_{11}$
$Q_{10}$
$Q_{14}$
$Q_{13}$
$Q_{17}$
$Q_{17A}$
$D_{11}$
$D_{12}$
$R_{111}$
$R_{110}$
$Q_{15}$
$Q_{16}$
$Q_{18}$
$Q_{18A}$
$Q_{19}$
$Q_{19A}$
$Q_{110}$
$Q_{110A}$
$R_P$
$R_8$
$R_{14}$
$R_{15}$
$R_{19}$
$R_{16}$
$R_{17}$
a
b
c
d
e
f
(8)
$V_{EE}$
$R_A$
$R_B$
$R_C$
$Q_C$
$Q_D$
$Q_E$
$Q_F$
$D_A$
$D_B$
$D_C$
$D_D$
$Q_A$
$Q_B$
$R_E$
$R_D$
$R_F$
TC05830S

Figure 3. Circuit Diagram


$D_0$
$D_1$
$D_2$
$D_3$
$Q_0$
$\overline{Q}_1$

$Q_0 = D_1 \cdot D_2 \cdot D_3 \cdot D_4$
$Q_1 = \overline{Q}_0$

POSITIVE LOGIC:
HIGH STATE = 1
LOW STATE = 1

LD05351S

Figure 4. Logic Diagram (One AND/NAND Gate)

## ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | | 10K ECL | UNIT |
|---|---|---|---|---|
| $V_{EE}$ | Supply voltage | | −8.0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | | 0 to $V_{EE}$ | V |
| $I_O$ | Output current | | −50 | mA |
| $T_S$ | Storage temperature | | −55 to +150 | °C |
| $T_J$ | Maximum junction temperature | Ceramic package | +165 | °C |
| | | Plastic package | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | 10K ECL | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | −5.2 | | V |
| $V_{IH}$ | HIGH level input voltage | $T_A$ = −30°C | | | −890 | mV |
| | | $T_A$ = +25°C | | | −810 | mV |
| | | $T_A$ = +85°C | | | −700 | mV |
| $V_{IHT}$ | HIGH level input threshold voltage | $T_A$ = −30°C | −1205 | | | mV |
| | | $T_A$ = +25°C | −1105 | | | mV |
| | | $T_A$ = +85°C | −1035 | | | mV |
| $V_{ILT}$ | LOW level input threshold voltage | $T_A$ = −30°C | | | −1500 | mV |
| | | $T_A$ = +25°C | | | −1475 | mV |
| | | $T_A$ = +85°C | | | −1440 | mV |
| $V_{IL}$ | LOW level input voltage | $T_A$ = −30°C | −1890 | | | mV |
| | | $T_A$ = +25°C | −1850 | | | mV |
| | | $T_A$ = +85°C | −1825 | | | mV |
| $T_A$ | Operating ambient temperature | | −30 | +25 | +85 | °C |

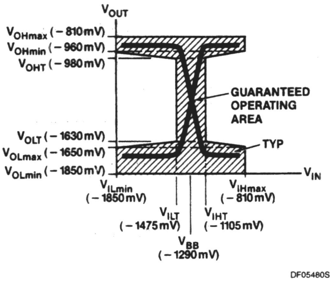
**NOTE:**
When operating at $V_{EE}$ other than specified voltage (−5.2V), the DC and AC Characteristics will vary slightly from specified values.
(See table of DC Characteristics)

**DC ELECTRICAL CHARACTERISTICS** $V_{CC1} = V_{CC2} =$ GND, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$, output loading with 50Ω to −2.0V ±0.010V unless otherwise specified[1]

| PARAMETER | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | $T_A = -30°C$ | −1060 | | −890 | mV | For $Q_n$ outputs apply $V_{IHmax}$ to all inputs.<br>For $\overline{Q}_n$ outputs, apply $V_{ILmin}$ to all inputs. |
| | | $T_A = +25°C$ | −960 | | −810 | mV | |
| | | $T_A = +85°C$ | −890 | | −700 | mV | |
| $V_{OHT}$ | HIGH level output threshold voltage | $T_A = -30°C$ | −1080 | | | mV | For $Q_n$ outputs, apply $V_{IHT}$ to each input, one at a time, with $V_{IHmax}$ applied to all other inputs.<br>For $\overline{Q}_n$ outputs, apply $V_{ILT}$ to each input, one at a time, with $V_{IHmax}$ applied to all other inputs. |
| | | $T_A = +25°C$ | −980 | | | mV | |
| | | $T_A = +85°C$ | −910 | | | mV | |
| $V_{OLT}$ | LOW level output threshold voltage | $T_A = -30°C$ | | | −1655 | mV | For $Q_n$ outputs, apply $V_{ILT}$ to each input, one at a time, with $V_{IHmax}$ applied to all other inputs.<br>For $\overline{Q}_n$ outputs, apply $V_{IHT}$ to each input, one at a time, with $V_{IHmax}$ applied to all other inputs. |
| | | $T_A = +25°C$ | | | −1630 | mV | |
| | | $T_A = +85°C$ | | | −1595 | mV | |
| $V_{OL}$ | LOW level output voltage | $T_A = -30°C$ | −1890 | | −1675 | mV | For $Q_n$ outputs, apply $V_{ILmin}$ to all inputs.<br>For $\overline{Q}_n$ outputs, apply $V_{IHmax}$ to all inputs. |
| | | $T_A = +25°C$ | −1850 | | −1650 | mV | |
| | | $T_A = +85°C$ | −1825 | | −1615 | mV | |
| $I_{IH}$ | HIGH level input current | $T_A = -30°C$ | | | 425 | μA | Apply $V_{IHmax}$ to input under test, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | $T_A = +25°C$ | | | 265 | μA | |
| | | $T_A = +85°C$ | | | 265 | μA | |
| $I_{IL}$ | LOW level input current | $T_A = -30°C$ | 0.5 | | | μA | Apply $V_{ILmin}$ to input under test, one at a time, with $V_{IHmax}$ applied to all other inputs. |
| | | $T_A = +25°C$ | 0.5 | | | μA | |
| | | $T_A = +85°C$ | 0.3 | | | μA | |
| $-I_{EE}$ | $V_{EE}$ supply current | $T_A = -30°C$ | | | 40 | mA | |
| | | $T_A = +25°C$ | | 28 | 36 | mA | |
| | | $T_A = +85°C$ | | | 40 | mA | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | $T_A = +25°C$ | | 0.016 | | V/V | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | 0.250 | | V/V | |
| $\frac{\Delta V_{BB}}{\Delta V_{EE}}$ | Reference bias voltage compensation | | | 0.148 | | V/V | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst-case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 5.



**NOTES:**

| | |
|---|---|
| $V_{IHmax}$ | – Maximum HIGH level input voltage (the most positive $V_{IH}$). |
| $V_{IHT}$ | – HIGH level input threshold voltage. |
| $V_{ILT}$ | – LOW level input threshold voltage. |
| $V_{ILmin}$ | – Minimum LOW level input voltage (the most negative $V_{IL}$). |
| $V_{OHmax}$ | – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition. |
| $V_{OHmin}$ | – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition. |
| $V_{OHT}$ | – HIGH level output threshold voltage with the inputs set to their respective threshold levels. |
| $V_{OLT}$ | – LOW level output threshold voltage with the inputs set to their respective threshold levels. |
| $V_{OLmax}$ | – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions. |
| $V_{OLmin}$ | – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions. |
| $V_{BB}$ | – Reference bias voltage (the internally generated reference voltage which is used to set the input and output threshold level). |

Figure 5. Transfer Characteristics

## AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$

| PARAMETER | $T_A = -30°C$ | | $T_A = +25°C$ | | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Typ | Max | Min | Max | | |
| $t_{PLH}$ Propagation delay | 1.4 | 4.1 | 1.4 | 2.3 | 3.7 | 1.4 | 4.1 | ns | Figs. 6, 7, 8 |
| $t_{PHL}$ $D_n$ to $Q_n$, $\overline{Q}_n$ | 1.4 | 4.1 | 1.4 | 2.3 | 3.7 | 1.4 | 4.1 | ns | |
| $t_{TLH}$ Transition time | 1.1 | 4.5 | 1.1 | 2.8 | 4.0 | 1.1 | 4.5 | ns | Figs. 6, 7, 8 |
| $t_{THL}$ 20% to 80%, 80% to 20% | 1.1 | 4.5 | 1.1 | 2.8 | 4.0 | 1.1 | 4.5 | ns | |

## AC WAVEFORMS

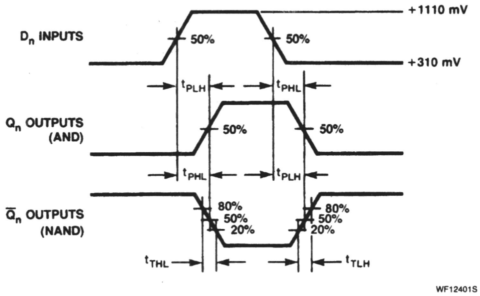
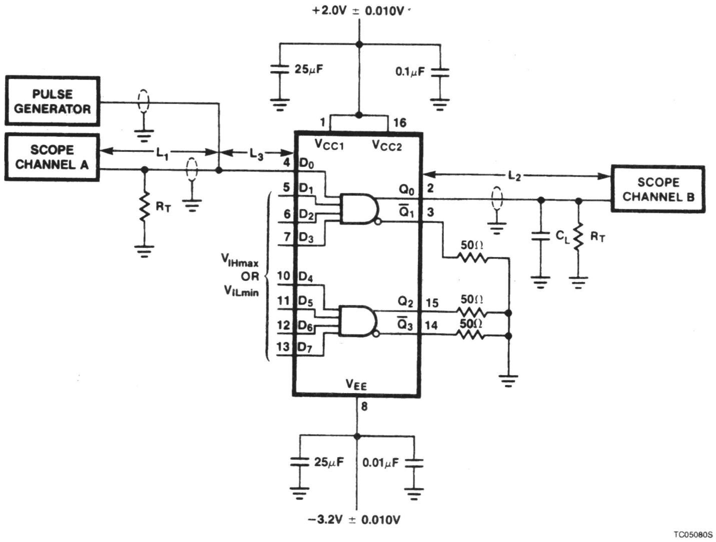


Figure 6. Propagation Delay and Transition Times

# Gate

# 10108

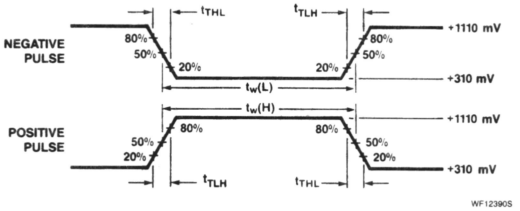
## TEST CIRCUITS AND WAVEFORMS


+2.0V ± 0.010V
25μF
0.1μF
PULSE GENERATOR
SCOPE CHANNEL A
L1
L3
RT
1
16
VCC1
VCC2
4 D0
5 D1
6 D2
7 D3
10 D4
11 D5
12 D6
13 D7
Q0 2
Q1 3
Q2 15
Q3 14
VIHmax OR VILmin
50Ω
50Ω
50Ω
L2
SCOPE CHANNEL B
CL
RT
VEE
8
25μF
0.01μF
−3.2V ± 0.010V
TC05080S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$
2. Decoupling 0.1μF and 25μF from GND to $V_{CC}$, 0.01μF and 25μF from GND to $V_{EE}$. (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T = 50\Omega$ terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance $\leq$ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ±1% or better.

Figure 7. AC Test Circuit for 10108


NEGATIVE PULSE
POSITIVE PULSE
$t_{THL}$
$t_{TLH}$
80%
50%
20%
$t_w(L)$
$t_w(H)$
+1110 mV
+310 mV
+1110 mV
+310 mV
$t_{TLH}$
$t_{THL}$
WF12390S

**INPUT PULSE REQUIREMENTS**
$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$, $V_T$ = GND (0V)

| Family | Amplitude | Rep Rate | Pulse Width | $t_{TLH}$ | $t_{THL}$ |
|---|---|---|---|---|---|
| 10K ECL | 800mVp-p | 1MHz | 500ns | 2.0 ±0.2ns | 2.0 ±0.2ns |

Figure 8. Input Pulse Definition

**Signetics**

# 10109
## Gate

**Dual 4-5 Input OR/NOR Gate**
***Product Specification***

**ECL Products**

### DESCRIPTION

The 10109 is a Dual 4-5 Input OR/NOR Gate. All unused inputs can be left open due to integrated pull-down resistors which avoid the need for a supply voltage.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT $(-I_{EE})$ |
|---|---|---|
| 10109 | 2.0ns | 11mA |

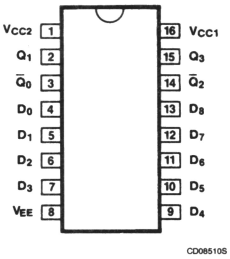
### ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} = GND$; $V_{EE} = -5.2V$<br>$T_A = -30°C$ to $+85°C$ |
|---|---|
| Plastic DIP | 10109N |
| Ceramic DIP | 10109F |

### PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_0 - D_8$ | Data Inputs |
| $Q_1$, $Q_3$ | Data Outputs (OR) |
| $\overline{Q}_0$, $\overline{Q}_2$ | Data Outputs (NOR) |

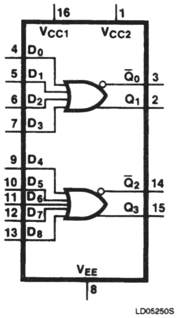
### PIN CONFIGURATION



VCC2 1
Q1 2
Q̄0 3
D0 4
D1 5
D2 6
D3 7
VEE 8
16 VCC1
15 Q3
14 Q̄2
13 D8
12 D7
11 D6
10 D5
9 D4
CD08510S

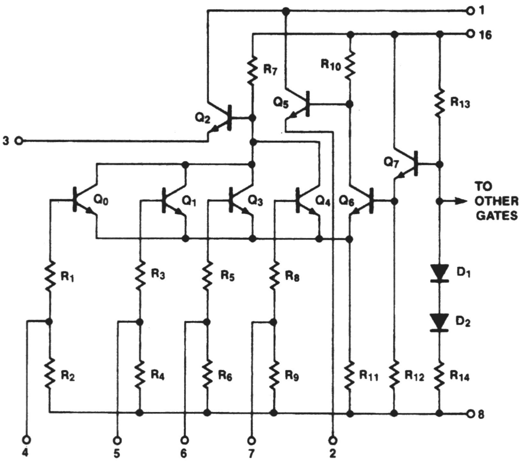
**Figure 1**

### LOGIC SYMBOL



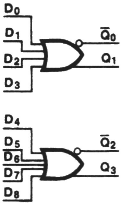
16
1
VCC1
VCC2
4 D0
5 D1
6 D2
7 D3
Q̄0 3
Q1 2
9 D4
10 D5
11 D6
12 D7
13 D8
Q̄2 14
Q3 15
VEE
8
LD05250S

**Figure 2**


1
16
R7
R10
R13
Q5
Q2
3
Q7
TO OTHER GATES
Q0
Q1
Q3
Q4
Q6
R1
R3
R5
R8
D1
D2
R2
R4
R6
R9
R11
R12
R14
8
4
5
6
7
2

TC04331S

Figure 3. Circuit Diagram (One Gate)


D0
D1
D2
D3
$\overline{Q}_0$
Q1
D4
D5
D6
D7
D8
$\overline{Q}_2$
Q3

$Q_0 = \overline{D_0 + D_1 + D_2 + D_3}$

$Q_2 = \overline{D_4 + D_5 + D_6 + D_7 + D_8}$

$Q_1 = D_0 + D_1 + D_2 + D_3$

$Q_3 = D_4 + D_5 + D_6 + D_7 + D_8$

Positive Logic: HIGH state = 1
LOW state = 0

LD04691S

Figure 4. Logic Diagram

# Gate 10109

**ABSOLUTE MAXIMUM RATINGS** (Operation beyond the limits set forth in this table may impair useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | | 10K ECL | UNIT |
|---|---|---|---|---|
| $V_{EE}$ | Supply voltage | | −8.0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | | 0 to $V_{EE}$ | V |
| $I_O$ | Output current | | −50 | mA |
| $T_S$ | Storage temperature | | −55 to +150 | °C |
| $T_J$ | Maximum junction temperature | Ceramic package | +165 | °C |
| | | Plastic package | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | 10K ECL | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | −5.2 | | V |
| $V_{IH}$ | HIGH level input voltage | $T_A = -30°C$ | | | −890 | mV |
| | | $T_A = +25°C$ | | | −810 | mV |
| | | $T_A = +85°C$ | | | −700 | mV |
| $V_{IHT}$ | HIGH level input threshold voltage | $T_A = -30°C$ | −1205 | | | mV |
| | | $T_A = +25°C$ | −1105 | | | mV |
| | | $T_A = +85°C$ | −1035 | | | mV |
| $V_{ILT}$ | LOW level input threshold voltage | $T_A = -30°C$ | | | −1500 | mV |
| | | $T_A = +25°C$ | | | −1475 | mV |
| | | $T_A = +85°C$ | | | −1440 | mV |
| $V_{IL}$ | LOW level input voltage | $T_A = -30°C$ | −1890 | | | mV |
| | | $T_A = +25°C$ | −1850 | | | mV |
| | | $T_A = +85°C$ | −1825 | | | mV |
| $T_A$ | Operating ambient temperature | | −30 | +25 | +85 | °C |

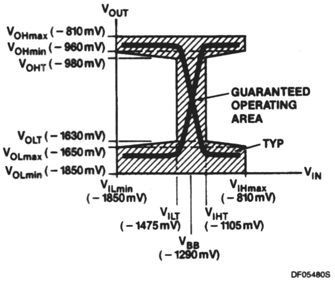
**NOTE:**
When operating at $V_{EE}$ other than specified voltage (−5.2V), the DC and AC Characteristics will vary slightly from specified values. (See table of DC Characteristics)

**DC ELECTRICAL CHARACTERISTICS** $V_{CC1} = V_{CC2}$ = GND, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$, output loading with 50Ω to −2.0V ±0.010V unless otherwise specified[1,3]

| PARAMETER | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | $T_A = -30°C$ | −1060 | | −890 | mV | For $Q_n$ outputs, apply $V_{IHmax}$ to all inputs.<br>For $\overline{Q}_n$ outputs, apply $V_{ILmin}$ to all inputs. |
| | | $T_A = +25°C$ | −960 | | −810 | mV | |
| | | $T_A = +85°C$ | −890 | | −700 | mV | |
| $V_{OHT}$ | HIGH level output threshold voltage | $T_A = -30°C$ | −1080 | | mV | | For $Q_n$ outputs, apply $V_{IHT}$ to each input, one at a time, with $V_{ILmin}$ applied to all other inputs.<br>For $\overline{Q}_n$ outputs, apply $V_{ILT}$ to each input, one at a time, with $V_{IHmin}$ applied to all other inputs. |
| | | $T_A = +25°C$ | −980 | | mV | | |
| | | $T_A = +85°C$ | −910 | | mV | | |
| $V_{OLT}$ | LOW level output threshold voltage | $T_A = -30°C$ | | | −1655 | mV | For $Q_n$ outputs, apply $V_{ILT}$ to each input, one at a time, with $V_{ILmin}$ applied to all other inputs.<br>For $\overline{Q}$ outputs, apply $V_{IHT}$ to each input, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | $T_A = +25°C$ | | | −1630 | mV | |
| | | $T_A = +85°C$ | | | −1595 | mV | |
| $V_{OL}$ | LOW level output voltage | $T_A = -30°C$ | −1890 | | −1675 | mV | For $\overline{Q}_n$ outputs, apply $V_{IHmax}$ to all inputs.<br>For $Q_n$ outputs, apply $V_{ILmin}$ to all inputs. |
| | | $T_A = +25°C$ | −1850 | | −1650 | mV | |
| | | $T_A = +85°C$ | −1825 | | −1615 | mV | |
| $I_{IH}$ | HIGH level input current | $T_A = -30°C$ | | | 425 | μA | Apply $V_{IHmax}$ to input under test, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | $T_A = +25°C$ | | | 265 | μA | |
| | | $T_A = +85°C$ | | | 265 | μA | |
| $I_{IL}$ | LOW level input current | $T_A = -30°C$ | 0.5 | | | μA | Apply $V_{ILmin}$ to input under test, one at a time, with $V_{IHmax}$ applied to all other inputs. |
| | | $T_A = +25°C$ | 0.5 | | | μA | |
| | | $T_A = +85°C$ | 0.3 | | | μA | |
| $-I_{EE}$ | $V_{EE}$ supply current | $T_A = -30°C$ | | | 15 | mA | |
| | | $T_A = +25°C$ | | 11 | 14 | mA | |
| | | $T_A = +85°C$ | | | 15 | mA | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | $T_A = +25°C$ | | 0.016 | | V/V | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | 0.250 | | V/V | |
| $\frac{\Delta V_{BB}}{\Delta V_{EE}}$ | Reference bias voltage compensation | | | 0.148 | | V/V | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst-case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 5.



**NOTES:**

$V_{IHmax}$ – Maximum HIGH level input voltage (the most positive $V_{IH}$).
$V_{IHT}$ – HIGH level input threshold voltage.
$V_{ILT}$ – LOW level input threshold voltage.
$V_{ILmin}$ – Minimum LOW level input voltage (the most negative $V_{IL}$).
$V_{OHmax}$ – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition.
$V_{OHmin}$ – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition.
$V_{OHT}$ – HIGH level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLT}$ – LOW level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLmax}$ – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions.
$V_{OLmin}$ – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions.
$V_{BB}$ – Reference bias voltage (the internally generated reference voltage which is used to set the input and output threshold level).

Figure 5. Transfer Characteristics

## AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$

| PARAMETER | | $T_A = -30°C$ | | $T_A = +25°C$ | | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Typ | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 1.0 | 3.1 | 1.0 | 2.0 | 2.9 | 1.0 | 3.3 | ns | Figs. 6, 7, 8 |
| $t_{PHL}$ | $D_n$ to $Q_1$, $Q_3$ | 1.0 | 3.1 | 1.0 | 2.0 | 2.9 | 1.0 | 3.3 | ns | |
| $t_{PLH}$ | Propagation delay | 1.0 | 3.1 | 1.0 | 2.0 | 2.9 | 1.0 | 3.3 | ns | Figs. 6, 7, 8 |
| $t_{PHL}$ | $D_n$ to $\overline{Q}_0$, $\overline{Q}_2$ | 1.0 | 3.1 | 1.0 | 2.0 | 2.9 | 1.0 | 3.3 | ns | |
| $t_{TLH}$ | Transition time | 1.1 | 3.6 | 1.1 | 2.0 | 3.3 | 1.1 | 3.7 | ns | Figs. 6, 7, 8 |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 1.1 | 3.6 | 1.1 | 2.0 | 3.3 | 1.1 | 3.7 | ns | |

## AC WAVEFORMS

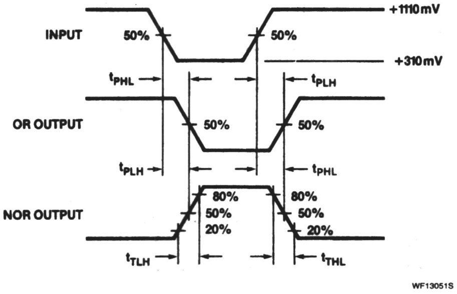
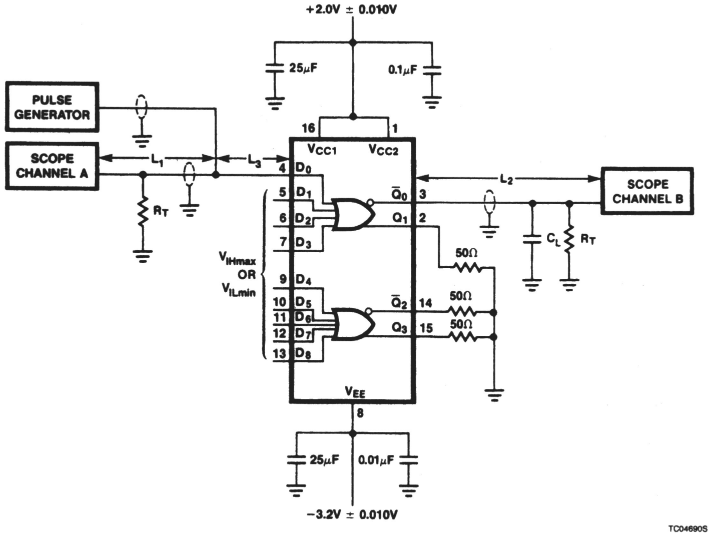


Figure 6. Propagation Delay and Transition Times

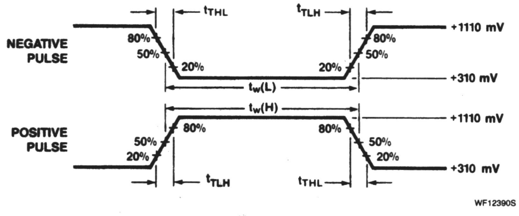
## TEST CIRCUITS AND WAVEFORMS


+2.0V ± 0.010V
25µF
0.1µF
PULSE GENERATOR
SCOPE CHANNEL A
$L_1$
$L_3$
$R_T$
16
1
$V_{CC1}$
$V_{CC2}$
4 $D_0$
5 $D_1$
6 $D_2$
7 $D_3$
9 $D_4$
10 $D_5$
11 $D_6$
12 $D_7$
13 $D_8$
$\overline{Q}_0$ 3
$Q_1$ 2
$\overline{Q}_2$ 14
$Q_3$ 15
$V_{IHmax}$ OR $V_{ILmin}$
$V_{EE}$
8
50Ω
50Ω
50Ω
$L_2$
SCOPE CHANNEL B
$C_L$
$R_T$
25µF
0.01µF
−3.2V ± 0.010V
TC04690S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$
2. Decoupling 0.1µF and 25µF from GND to $V_{CC}$, 0.01µF and 25µF from GND to $V_{EE}$. (0.01 and 0.1µF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance ⩽ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.

Figure 7. AC Test Circuit for 10109


NEGATIVE PULSE
POSITIVE PULSE
$t_{THL}$
$t_{TLH}$
80%
50%
20%
$t_w(L)$
$t_w(H)$
+1110 mV
+310 mV
+1110 mV
+310 mV
WF12390S

**INPUT PULSE REQUIREMENTS**
**$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$, $V_T$ = GND (0V)**

| Family | Amplitude | Rep Rate | Pulse Width | $t_{TLH}$ | $t_{THL}$ |
|---|---|---|---|---|---|
| 10K ECL | 800mVp-p | 1MHz | 500ns | 2.0 ± 0.2ns | 2.0 ± 0.2ns |

Figure 8. Input Pulse Definition

**Signetics**

# 10110
## Gate

**Dual 3-Input/3-Output OR Gate (Line Driver)**
***Product Specification***

**ECL Products**

### DESCRIPTION

The 10110 is a Dual 3-Input/3-Output OR Gate intended to drive up to three transmission lines simultaneously. This feature makes the device particularly useful in clock distribution applications. All unused inputs can be left open due to integrated pull-down resistors which avoid the need for a supply voltage.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 10110 | 2.4ns | 30mA |

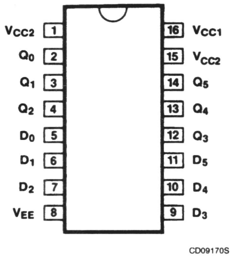
### ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} = GND$; $V_{EE} = -5.2V$,<br>$T_A = -30°C$ to $+85°C$ |
|---|---|
| Plastic DIP | 10110N |
| Ceramic DIP | 10110F |

### PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_0 - D_5$ | Data Inputs |
| $Q_0 - Q_5$ | Data Outputs (OR) |

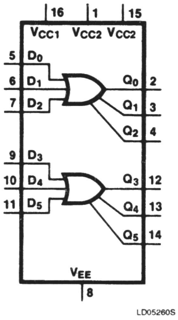
### PIN CONFIGURATION



VCC2 1
Q0 2
Q1 3
Q2 4
D0 5
D1 6
D2 7
VEE 8
16 VCC1
15 VCC2
14 Q5
13 Q4
12 Q3
11 D5
10 D4
9 D3
CD09170S

Figure 1

### LOGIC SYMBOL



16
1
15
VCC1 VCC2 VCC2
5 D0
6 D1
7 D2
Q0 2
Q1 3
Q2 4
9 D3
10 D4
11 D5
Q3 12
Q4 13
Q5 14
VEE
8
LD05260S

Figure 2

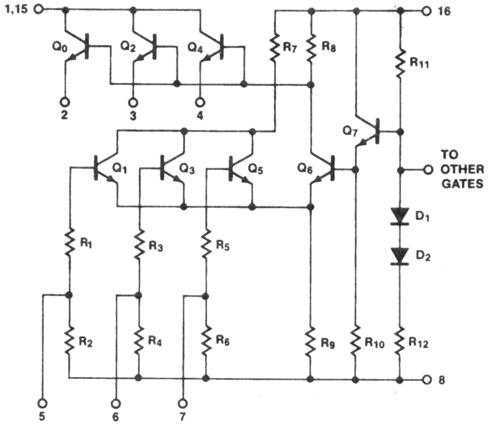
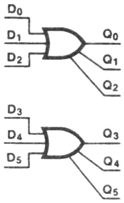

1,15
16
Q0
Q2
Q4
R7
R8
R11
2
3
4
Q7
Q1
Q3
Q5
Q6
TO OTHER GATES
D1
D2
R1
R3
R5
R2
R4
R6
R9
R10
R12
8
5
6
7
TC04340S

Figure 3. Circuit Diagram (One Gate)


D0
D1
D2
Q0
Q1
Q2
D3
D4
D5
Q3
Q4
Q5

$Q_0 = Q_1 = Q_2 = D_0 + D_1 + D_2$

$Q_3 = Q_4 = Q_5 = D_3 + D_4 + D_5$

**Positive logic:** **HIGH state = 1**
**LOW state = 0**

LD04700S

Figure 4. Logic Diagram

## Gate

## 10110

**ABSOLUTE MAXIMUM RATINGS** (Operation beyond the limits set forth in this table may impair useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | | 10K ECL | UNIT |
|---|---|---|---|---|
| $V_{EE}$ | Supply voltage | | −8.0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | | 0 to $V_{EE}$ | V |
| $I_O$ | Output current | | −50 | mA |
| $T_S$ | Storage temperature | | −55 to +150 | °C |
| $T_J$ | Maximum junction temperature | Ceramic package | +165 | °C |
| | | Plastic package | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | 10K ECL | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$, $V_{CC3}$ | Circuit ground | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | −5.2 | | V |
| $V_{IH}$ | HIGH level input voltage | $T_A$ = −30°C | | | −890 | mV |
| | | $T_A$ = +25°C | | | −810 | mV |
| | | $T_A$ = +85°C | | | −700 | mV |
| $V_{IHT}$ | HIGH level input threshold voltage | $T_A$ = −30°C | −1205 | | | mV |
| | | $T_A$ = +25°C | −1105 | | | mV |
| | | $T_A$ = +85°C | −1035 | | | mV |
| $V_{ILT}$ | LOW level input threshold voltage | $T_A$ = −30°C | | | −1500 | mV |
| | | $T_A$ = +25°C | | | −1475 | mV |
| | | $T_A$ = +85°C | | | −1440 | mV |
| $V_{IL}$ | LOW level input voltage | $T_A$ = −30°C | −1890 | | | mV |
| | | $T_A$ = +25°C | −1850 | | | mV |
| | | $T_A$ = +85°C | −1825 | | | mV |
| $T_A$ | Operating ambient temperature | | −30 | +25 | +85 | °C |

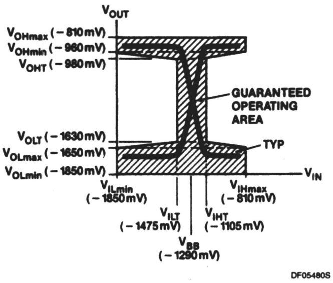
**NOTE:**
When operating at $V_{EE}$ other than specified voltage (−5.2V), the DC and AC Characteristics will vary slightly from specified values.
(See table of DC Characteristics)

**DC ELECTRICAL CHARACTERISTICS** $V_{CC1} = V_{CC2} =$ GND, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$, output loading with 50Ω to $-2.0V \pm 0.010V$ unless otherwise specified[1, 3]

| PARAMETER | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | $T_A = -30°C$ | -1060 | | -890 | mV | Apply $V_{IHmax}$ to all inputs. |
| | | $T_A = +25°C$ | -960 | | -810 | mV | |
| | | $T_A = +85°C$ | -890 | | -700 | mV | |
| $V_{OHT}$ | HIGH level output threshold voltage | $T_A = -30°C$ | -1080 | | | mV | Apply $V_{IHT}$ to each input, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | $T_A = +25°C$ | -980 | | | mV | |
| | | $T_A = +85°C$ | -910 | | | mV | |
| $V_{OLT}$ | LOW level output threshold voltage | $T_A = -30°C$ | | | -1655 | mV | Apply $V_{ILT}$ to each input, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | $T_A = +25°C$ | | | -1630 | mV | |
| | | $T_A = +85°C$ | | | -1595 | mV | |
| $V_{OL}$ | LOW level output voltage | $T_A = -30°C$ | -1890 | | -1675 | mV | Apply $V_{ILmin}$ to all inputs. |
| | | $T_A = +25°C$ | -1850 | | -1650 | mV | |
| | | $T_A = +85°C$ | -1825 | | -1615 | mV | |
| $I_{IH}$ | HIGH level input current | $T_A = -30°C$ | | | 680 | μA | Apply $V_{IHmax}$ to each input under test, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | $T_A = +25°C$ | | | 425 | μA | |
| | | $T_A = +85°C$ | | | 425 | μA | |
| $I_{IL}$ | LOW level input current | $T_A = -30°C$ | 0.5 | | | μA | Apply $V_{ILmin}$ to each input under test, one at a time, with $V_{IHmax}$ applied to all other inputs. |
| | | $T_A = +25°C$ | 0.5 | | | μA | |
| | | $T_A = +85°C$ | 0.3 | | | μA | |
| $-I_{EE}$ | $V_{EE}$ supply current | $T_A = -30°C$ | | | 42 | mA | |
| | | $T_A = +25°C$ | | 30 | 38 | mA | |
| | | $T_A = +85°C$ | | | 42 | mA | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | $T_A = +25°C$ | | 0.016 | | V/V | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | 0.250 | | V/V | |
| $\frac{\Delta V_{BB}}{\Delta V_{EE}}$ | Reference bias voltage compensation | | | 0.148 | | V/V | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst-case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 5.


$V_{OUT}$
$V_{OHmax}$ (−810mV)
$V_{OHmin}$ (−960mV)
$V_{OHT}$ (−980mV)
GUARANTEED OPERATING AREA
$V_{OLT}$ (−1630mV)
$V_{OLmax}$ (−1650mV)
$V_{OLmin}$ (−1850mV)
TYP
$V_{IN}$
$V_{ILmin}$ (−1850mV)
$V_{IHmax}$ (−810mV)
$V_{ILT}$ (−1475mV)
$V_{IHT}$ (−1105mV)
$V_{BB}$ (−1290mV)
DF05480S

**NOTES:**

$V_{IHmax}$ – Maximum HIGH level input voltage (the most positive $V_{IH}$).
$V_{IHT}$ – HIGH level input threshold voltage.
$V_{ILT}$ – LOW level input threshold voltage.
$V_{ILmin}$ – Minimum LOW level input voltage (the most negative $V_{IL}$).
$V_{OHmax}$ – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition.
$V_{OHmin}$ – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition.
$V_{OHT}$ – HIGH level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLT}$ – LOW level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLmax}$ – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions.
$V_{OLmin}$ – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions.
$V_{BB}$ – Reference bias voltage (the internally generated reference voltage which is used to set the input and output threshold level).

**Figure 5. Transfer Characteristics**

## AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$

| PARAMETER | $T_A = -30°C$ | | $T_A = +25°C$ | | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Typ | Max | Min | Max | | |
| $t_{PLH}$ Propagation delay | 1.4 | 3.5 | 1.4 | 2.4 | 3.5 | 1.5 | 3.8 | ns | Figs. 6, 7, 8 |
| $t_{PHL}$ $D_n$ to $Q_n$ | 1.4 | 3.5 | 1.4 | 2.4 | 3.5 | 1.5 | 3.8 | ns | |
| $t_{TLH}$ Transition time | 1.0 | 3.5 | 1.1 | 2.2 | 3.5 | 1.2 | 3.8 | ns | Figs. 6, 7, 8 |
| $t_{THL}$ 20% to 80%, 80% to 20% | 1.0 | 3.5 | 1.1 | 2.2 | 3.5 | 1.2 | 3.8 | ns | |

## AC WAVEFORMS

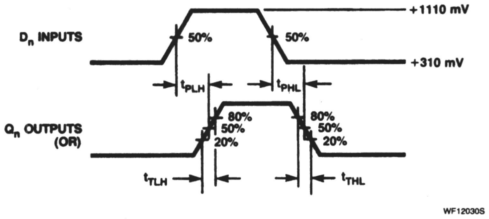
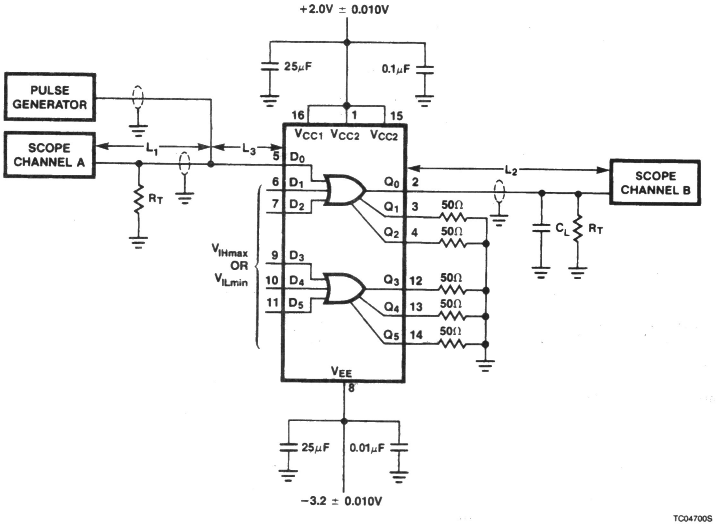

$D_n$ INPUTS
50%
50%
+1110 mV
+310 mV
$t_{PLH}$
$t_{PHL}$
$Q_n$ OUTPUTS (OR)
80%
50%
20%
80%
50%
20%
$t_{TLH}$
$t_{THL}$
WF12030S

**Figure 6. Propagation Delay and Transition Times**

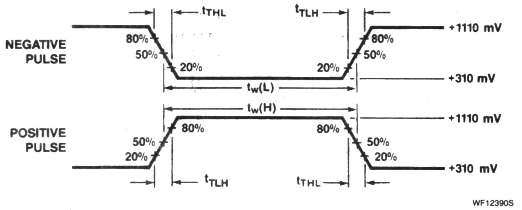
## TEST CIRCUITS AND WAVEFORMS


+2.0V ± 0.010V
25μF
0.1μF
16
1
15
PULSE GENERATOR
SCOPE CHANNEL A
L1
L3
L2
Vcc1 Vcc2 Vcc2
5 D0
6 D1
7 D2
9 D3
10 D4
11 D5
Q0 2
Q1 3
Q2 4
Q3 12
Q4 13
Q5 14
50Ω
RT
CL
VIHmax OR VILmin
SCOPE CHANNEL B
VEE
8
25μF
0.01μF
−3.2 ± 0.010V
TC04700S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$
2. Decoupling 0.1μF and 25μF from GND to $V_{CC}$, 0.01μF and 25μF from GND to $V_{EE}$. (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance ≤ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ±1% or better.

Figure 7. AC Test Circuit for 10110


NEGATIVE PULSE
POSITIVE PULSE
tTHL
tTLH
80%
50%
20%
tw(L)
tw(H)
+1110 mV
+310 mV
WF12390S

| INPUT PULSE REQUIREMENTS<br>$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$, $V_T$ = GND (0V) | | | | | |
|---|---|---|---|---|---|
| Family | Amplitude | Rep Rate | Pulse Width | $t_{TLH}$ | $t_{THL}$ |
| 10K ECL | 800mVp-p | 1MHz | 500ns | 2.0 ±0.2ns | 2.0 ±0.2ns |

Figure 8. Input Pulse Definition

**Signetics**

# 10111
# Gate

**Dual 3-Input/3-Output NOR Gate (Line Driver)**
***Product Specification***

**ECL Products**

## DESCRIPTION

The 10111 is a Dual 3-Input/3-Output NOR Gate intended to drive up to three transmission lines simultaneously. The ability to control three parallel lines makes this device particularly useful in clock distribution applications. All unused inputs can be left open due to integrated pull-down resistors which avoid the need for a supply voltage.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 10111 | 2.4ns | 29mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} = \text{GND}$; $V_{EE} = -5.2V$<br>$T_A = -30°C$ to $+85°C$ |
|---|---|
| Plastic DIP | 10111N |
| Ceramic DIP | 10111F |

## PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_0 - D_5$ | Data Inputs |
| $\overline{Q}_0 - \overline{Q}_5$ | Data Outputs (NOR) |

## PIN CONFIGURATION

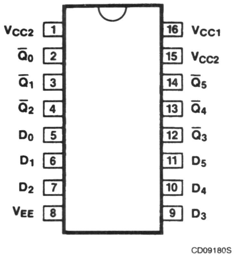

VCC2 1
Q̄0 2
Q̄1 3
Q̄2 4
D0 5
D1 6
D2 7
VEE 8
16 VCC1
15 VCC2
14 Q̄5
13 Q̄4
12 Q̄3
11 D5
10 D4
9 D3
CD09180S

Figure 1

## LOGIC SYMBOL

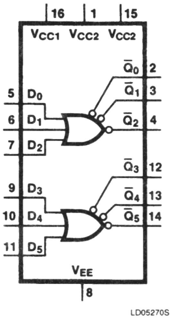
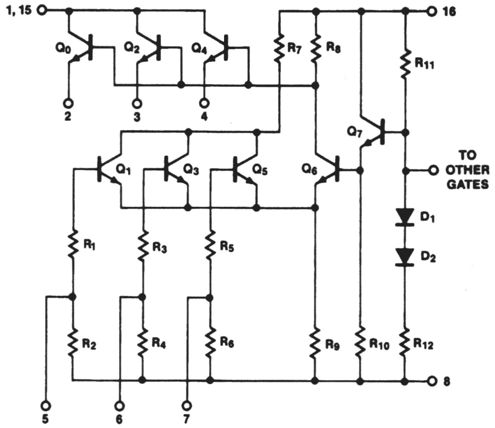
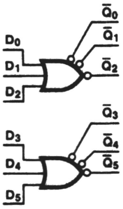

16
1
15
VCC1
VCC2
VCC2
Q̄0 2
Q̄1 3
Q̄2 4
5 D0
6 D1
7 D2
Q̄3 12
Q̄4 13
Q̄5 14
9 D3
10 D4
11 D5
VEE
8
LD05270S

Figure 2


1, 15
16
Q0
Q2
Q4
R7
R8
R11
2
3
4
Q7
Q1
Q3
Q5
Q6
TO OTHER GATES
D1
D2
R1
R3
R5
R2
R4
R6
R9
R10
R12
8
5
6
7

TC04351S

Figure 3. Circuit Diagram (One Gate)


D0
D1
D2
$\bar{Q}_0$
$\bar{Q}_1$
$\bar{Q}_2$
D3
D4
D5
$\bar{Q}_3$
$\bar{Q}_4$
$\bar{Q}_5$

$Q_0 = Q_1 = Q_2 = \overline{D_0 + D_1 + D_2}$
$Q_3 = Q_4 = Q_5 = \overline{D_3 + D_4 + D_5}$

**Positive logic:** **HIGH state = 1**
**LOW state = 0**

LD04711S

Figure 4. Logic Diagram

**ABSOLUTE MAXIMUM RATINGS** (Operation beyond the limits set forth in this table may impair useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | | 10K ECL | UNIT |
|---|---|---|---|---|
| $V_{EE}$ | Supply voltage | | -8.0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | | 0 to $V_{EE}$ | V |
| $I_O$ | Output current | | -50 | mA |
| $T_S$ | Storage temperature | | -55 to +150 | °C |
| $T_J$ | Maximum junction temperature | Ceramic package | +165 | °C |
| | | Plastic package | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | 10K ECL | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | -5.2 | | V |
| $V_{IH}$ | HIGH level input voltage | $T_A$ = -30°C | | | -890 | mV |
| | | $T_A$ = +25°C | | | -810 | mV |
| | | $T_A$ = +85°C | | | -700 | mV |
| $V_{IHT}$ | HIGH level input threshold voltage | $T_A$ = -30°C | -1205 | | | mV |
| | | $T_A$ = +25°C | -1105 | | | mV |
| | | $T_A$ = +85°C | -1035 | | | mV |
| $V_{ILT}$ | LOW level input threshold voltage | $T_A$ = -30°C | | | -1500 | mV |
| | | $T_A$ = +25°C | | | -1475 | mV |
| | | $T_A$ = +85°C | | | -1440 | mV |
| $V_{IL}$ | LOW level input voltage | $T_A$ = -30°C | -1890 | | | mV |
| | | $T_A$ = +25°C | -1850 | | | mV |
| | | $T_A$ = +85°C | -1825 | | | mV |
| $T_A$ | Operating ambient temperature | | -30 | +25 | +85 | °C |

**NOTE:**
When operating at $V_{EE}$ other than specified voltage (-5.2V), the DC and AC Characteristics will vary slightly from specified values. (See table of DC Characteristics)

**DC ELECTRICAL CHARACTERISTICS** $V_{CC1} = V_{CC2}$ = GND, $V_{EE}$ = −5.2V ± 0.010V, $T_A$ = −30°C to +85°C, output loading with 50Ω to −2.0V ± 0.010V unless otherwise specified[1, 3]

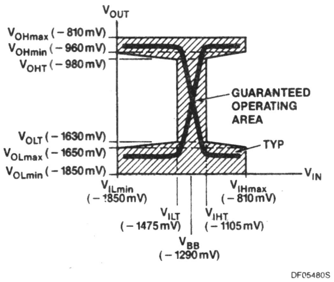
| PARAMETER | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | $T_A$ = −30°C | −1060 | | −890 | mV | Apply $V_{ILmin}$ to all inputs. |
| | | $T_A$ = +25°C | −960 | | −810 | mV | |
| | | $T_A$ = +85°C | −890 | | −700 | mV | |
| $V_{OHT}$ | HIGH level output threshold voltage | $T_A$ = −30°C | −1080 | | | mV | Apply $V_{ILT}$ to each input, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | $T_A$ = +25°C | −980 | | | mV | |
| | | $T_A$ = +85°C | −910 | | | mV | |
| $V_{OLT}$ | LOW level output threshold voltage | $T_A$ = −30°C | | | −1655 | mV | Apply $V_{IHT}$ to each input, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | $T_A$ = +25°C | | | −1630 | mV | |
| | | $T_A$ = +85°C | | | −1595 | mV | |
| $V_{OL}$ | LOW level output voltage | $T_A$ = −30°C | −1890 | | −1675 | mV | Apply $V_{IHmax}$ to all inputs. |
| | | $T_A$ = +25°C | −1850 | | −1650 | mV | |
| | | $T_A$ = +85°C | −1825 | | −1615 | mV | |
| $I_{IH}$ | HIGH level input current | $T_A$ = −30°C | | | 680 | μA | Apply $V_{IHmax}$ to each input under test, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | $T_A$ = +25°C | | | 425 | μA | |
| | | $T_A$ = +85°C | | | 425 | μA | |
| $I_{IL}$ | LOW level input current | $T_A$ = −30°C | 0.5 | | | μA | Apply $V_{ILmin}$ to each input under test, one at a time, with $V_{IHmax}$ applied to all other inputs. |
| | | $T_A$ = +25°C | 0.5 | | | μA | |
| | | $T_A$ = +85°C | 0.3 | | | μA | |
| $-I_{EE}$ | $V_{EE}$ supply current | $T_A$ = −30°C | | | 42 | mA | |
| | | $T_A$ = +25°C | | 29 | 38 | mA | |
| | | $T_A$ = +85°C | | | 42 | mA | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | $T_A$ = +25°C | | 0.016 | | V/V | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | 0.250 | | V/V | |
| $\frac{\Delta V_{BB}}{\Delta V_{EE}}$ | Reference bias voltage compensation | | | 0.148 | | V/V | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst-case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 5.

# Gate

# 10111


$V_{OUT}$
$V_{OHmax}$ (−810mV)
$V_{OHmin}$ (−960mV)
$V_{OHT}$ (−980mV)
GUARANTEED OPERATING AREA
$V_{OLT}$ (−1630mV)
$V_{OLmax}$ (−1650mV)
$V_{OLmin}$ (−1850mV)
TYP
$V_{IN}$
$V_{ILmin}$ (−1850mV)
$V_{IHmax}$ (−810mV)
$V_{ILT}$ (−1475mV)
$V_{IHT}$ (−1105mV)
$V_{BB}$ (−1290mV)
DF05480S

**NOTES:**

$V_{IHmax}$ – Maximum HIGH level input voltage (the most positive $V_{IH}$).
$V_{IHT}$ – HIGH level input threshold voltage.
$V_{ILT}$ – LOW level input threshold voltage.
$V_{ILmin}$ – Minimum LOW level input voltage (the most negative $V_{IL}$).
$V_{OHmax}$ – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition.
$V_{OHmin}$ – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition.
$V_{OHT}$ – HIGH level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLT}$ – LOW level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLmax}$ – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions.
$V_{OLmin}$ – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions.
$V_{BB}$ – Reference bias voltage (the internally generated reference voltage which is used to set the input and output threshold level).

Figure 5. Transfer Characteristics.

## AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$

| PARAMETER | $T_A = -30°C$ | | $T_A = +25°C$ | | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Typ | Max | Min | Max | | |
| $t_{PLH}$ Propagation delay | 1.4 | 3.5 | 1.4 | 2.4 | 3.5 | 1.5 | 3.8 | ns | Figs. 6, 7, 8 |
| $t_{PHL}$ $D_n$ to $\overline{Q}_n$ | 1.4 | 3.5 | 1.4 | 2.4 | 3.5 | 1.5 | 3.8 | ns | |
| $t_{TLH}$ Transition time | 1.0 | 3.5 | 1.1 | 2.2 | 3.5 | 1.2 | 3.8 | ns | Figs. 6, 7, 8 |
| $t_{THL}$ 20% to 80%, 80% to 20% | 1.0 | 3.5 | 1.1 | 2.2 | 3.5 | 1.2 | 3.8 | ns | |

## AC WAVEFORMS

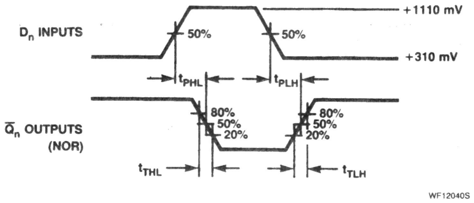
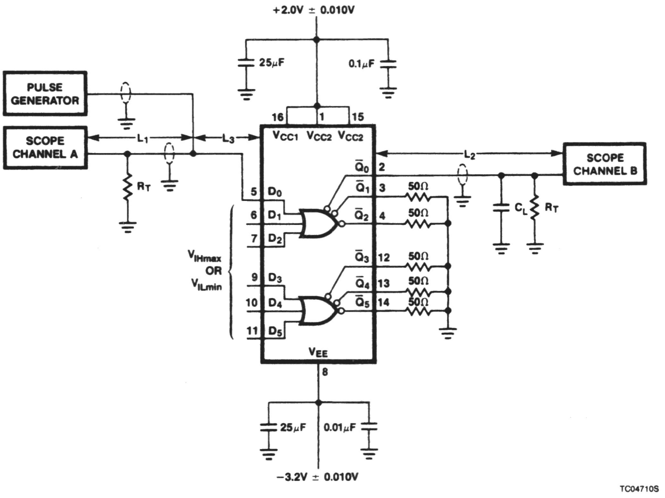

$D_n$ INPUTS
50%
50%
+1110 mV
+310 mV
$t_{PHL}$
$t_{PLH}$
$\overline{Q}_n$ OUTPUTS (NOR)
80%
50%
20%
80%
50%
20%
$t_{THL}$
$t_{TLH}$
WF12040S

Figure 6. Propagation Delay and Transition Times

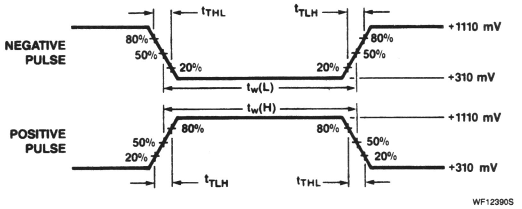
## TEST CIRCUITS AND WAVEFORMS


+2.0V ± 0.010V
25μF
0.1μF
PULSE GENERATOR
SCOPE CHANNEL A
L1
L3
L2
16
1
15
VCC1 VCC2 VCC2
SCOPE CHANNEL B
RT
Q̄0 2
Q̄1 3
Q̄2 4
Q̄3 12
Q̄4 13
Q̄5 14
50Ω
CL
RT
5 D0
6 D1
7 D2
9 D3
10 D4
11 D5
VIHmax OR VILmin
VEE
8
25μF
0.01μF
−3.2V ± 0.010V
TC04710S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$
2. Decoupling 0.1μF and 25μF from GND to $V_{CC}$, 0.01μF and 25μF from GND to $V_{EE}$. (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance ≤ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ±1% or better.

Figure 7. AC Test Circuit for 10111


NEGATIVE PULSE
POSITIVE PULSE
tTHL
tTLH
80%
50%
20%
tw(L)
tw(H)
+1110 mV
+310 mV
WF12390S

| INPUT PULSE REQUIREMENTS<br>$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$, $V_T$ = GND (0V) | | | | | |
|---|---|---|---|---|---|
| Family | Amplitude | Rep Rate | Pulse Width | $t_{TLH}$ | $t_{THL}$ |
| 10K ECL | 800mVp-p | 1MHz | 500ns | 2.0 ±0.2ns | 2.0 ±0.2ns |

Figure 8. Input Pulse Definition

**Signetics**

# 10113
## Gate

**Quad Exclusive-OR Gate With Enable Input**
***Product Specification***

**ECL Products**

## DESCRIPTION

The 10113 is a Quadruple Exclusive-OR Gate with enable input common to all gates. The enable is active in LOW state. A 4-bit comparision function (A = B) can be obtained by wire-ORing the four outputs together. Direct connection to buses is possible thanks to open-emitter outputs. All unused inputs can be left open due to integrated pull-down resistors which avoid the need for a supply voltage.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 10113 | 2.6ns | 34mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} =$ GND; $V_{EE} = -5.2V$<br>$T_A = -30°C$ to $+85°C$ |
|---|---|
| Plastic DIP | 10113N |
| Ceramic DIP | 10113F |

## PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_0 - D_7$ | Data Inputs |
| $\overline{E}$ | Enable Input |
| $Q_0 - Q_3$ | Data Outputs |

## PIN CONFIGURATION

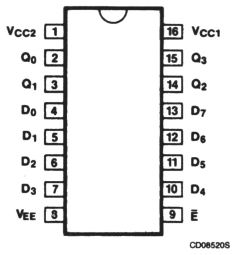

VCC2 1
Q0 2
Q1 3
D0 4
D1 5
D2 6
D3 7
VEE 8
16 VCC1
15 Q3
14 Q2
13 D7
12 D6
11 D5
10 D4
9 Ē
CD08520S

Figure 1

## LOGIC SYMBOL

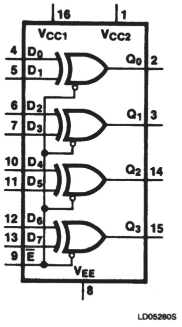

16
1
VCC1
VCC2
4 D0
5 D1
6 D2
7 D3
10 D4
11 D5
12 D6
13 D7
9 Ē
Q0 2
Q1 3
Q2 14
Q3 15
VEE
8
LD05280S

Figure 2

## Gate

## 10113

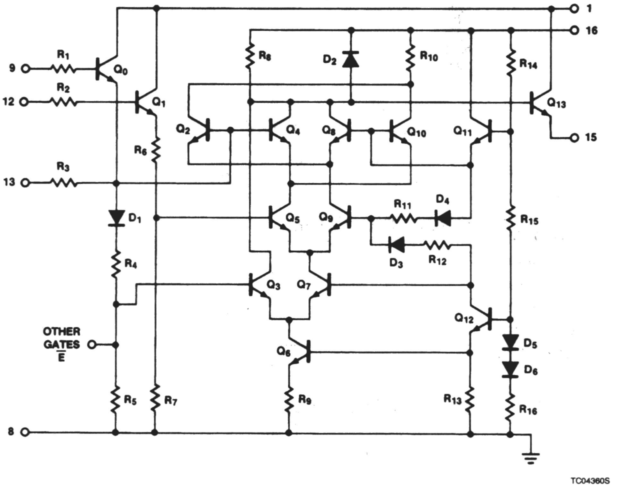
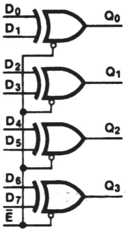

1
16
9
R1
Q0
12
R2
Q1
R8
D2
R10
R14
Q13
15
Q2
Q4
Q8
Q10
Q11
R6
13
R3
D1
R11
D4
Q5
Q9
R15
D3
R12
R4
Q3
Q7
Q12
OTHER
GATES
Ē
D5
D6
Q6
R5
R7
R9
R13
R16
8
TC04360S

Figure 3. Circuit Diagram (One Gate)


D0
D1
Q0
D2
D3
Q1
D4
D5
Q2
D6
D7
Q3
Ē

$Q_0 = (D_0 \oplus D_1) \cdot \overline{E}$

$Q_1 = (D_2 \oplus D_3) \cdot \overline{E}$

$Q_2 = (D_4 \oplus D_5) \cdot \overline{E}$

$Q_3 = (D_6 \oplus D_7) \cdot \overline{E}$

**Positive logic:** HIGH state = 1
LOW state = 0

LD04721S

Figure 4. Logic Diagram

### FUNCTION TABLE

| $D_0$ | $D_1$ | $\overline{E}$ | $Q_0$ |
|---|---|---|---|
| L | L | L | L |
| L | H | L | H |
| H | L | L | H |
| H | H | L | L |
| X | X | H | L |

Positive Logic:
H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = Don't care

**ABSOLUTE MAXIMUM RATINGS** (Operation beyond the limits set forth in this table may impair useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | | 10K ECL | UNIT |
|---|---|---|---|---|
| $V_{EE}$ | Supply voltage | | −8.0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | | 0 to $V_{EE}$ | V |
| $I_O$ | Output current | | −50 | mA |
| $T_S$ | Storage temperature | | −55 to +150 | °C |
| $T_J$ | Maximum junction temperature | Ceramic package | +165 | °C |
| | | Plastic package | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | 10K ECL | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | −5.2 | | V |
| $V_{IH}$ | HIGH level input voltage | $T_A = -30°C$ | | | −890 | mV |
| | | $T_A = +25°C$ | | | −810 | mV |
| | | $T_A = +85°C$ | | | −700 | mV |
| $V_{IHT}$ | HIGH level input threshold voltage | $T_A = -30°C$ | −1205 | | | mV |
| | | $T_A = +25°C$ | −1105 | | | mV |
| | | $T_A = +85°C$ | −1035 | | | mV |
| $V_{ILT}$ | LOW level input threshold voltage | $T_A = -30°C$ | | | −1500 | mV |
| | | $T_A = +25°C$ | | | −1475 | mV |
| | | $T_A = +85°C$ | | | −1440 | mV |
| $V_{IL}$ | LOW level input voltage | $T_A = -30°C$ | −1890 | | | mV |
| | | $T_A = +25°C$ | −1850 | | | mV |
| | | $T_A = +85°C$ | −1825 | | | mV |
| $T_A$ | Operating ambient temperature | | −30 | +25 | +85 | °C |

**NOTE:**
When operating at $V_{EE}$ other than specified voltage (−5.2V), the DC and AC Characteristics will vary slightly from specified values.
(See table of DC Characteristics)

# Gate

# 10113

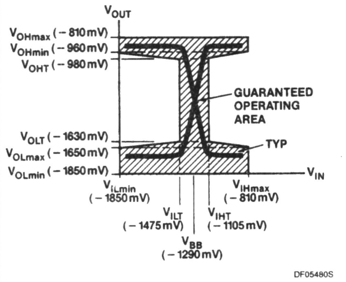
## DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = GND, $V_{EE}$ = −5.2V ±0.010V, $T_A$ = −30°C to +85°C, output loading with 50Ω to −2.0V ±0.010V unless otherwise specified[1, 3]

| PARAMETER | | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | | $T_A$ = −30°C | −1060 | | −890 | mV | Apply $V_{ILmin}$ to enable input and one gate input with $V_{IHmax}$ applied to the other gate input. |
| | | | $T_A$ = +25°C | −960 | | −810 | mV | |
| | | | $T_A$ = +85°C | −890 | | −700 | mV | |
| $V_{OHT}$ | HIGH level output threshold voltage | | $T_A$ = −30°C | −1080 | | | mV | Apply $V_{IHT}$ to one gate input with $V_{ILmin}$ applied to the other gate input and enable input. |
| | | | $T_A$ = +25°C | −980 | | | mV | |
| | | | $T_A$ = +85°C | −910 | | | mV | |
| $V_{OLT}$ | LOW level output threshold voltage | | $T_A$ = −30°C | | | −1655 | mV | Apply $V_{ILT}$ to one gate input with $V_{ILmin}$ applied to the other gate input. |
| | | | $T_A$ = +25°C | | | −1630 | mV | |
| | | | $T_A$ = +85°C | | | −1595 | mV | |
| $V_{OL}$ | LOW level output voltage | | $T_A$ = −30°C | −1890 | | −1675 | mV | Apply $V_{ILmin}$ to all inputs for each output. |
| | | | $T_A$ = +25°C | −1850 | | −1650 | mV | |
| | | | $T_A$ = +85°C | −1825 | | −1615 | mV | |
| $I_{IH}$ | HIGH level input current | $D_0$, $D_3$ $D_4$, $D_7$ inputs | $T_A$ = −30°C | | | 425 | μA | Apply $V_{IHmax}$ to each input under test, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A$ = +25°C | | | 265 | μA | |
| | | | $T_A$ = +85°C | | | 265 | μA | |
| | | $D_1$, $D_2$ $D_5$, $D_6$ inputs | $T_A$ = −30°C | | | 350 | μA | |
| | | | $T_A$ = +25°C | | | 220 | μA | |
| | | | $T_A$ = +85°C | | | 220 | μA | |
| | | $\overline{E}$ input | $T_A$ = −30°C | | | 870 | μA | Apply $V_{IHmax}$ to $\overline{E}$ input with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A$ = +25°C | | | 545 | μA | |
| | | | $T_A$ = +85°C | | | 545 | μA | |
| $I_{IL}$ | LOW level input current | | $T_A$ = −30°C | 0.5 | | | μA | Apply $V_{ILmin}$ to each input under test, one at time, with $V_{IHmax}$ applied to all other inputs. |
| | | | $T_A$ = +25°C | 0.5 | | | μA | |
| | | | $T_A$ = +85°C | 0.3 | | | μA | |
| $-I_{EE}$ | $V_{EE}$ supply current | | $T_A$ = −30°C | | | 46 | mA | |
| | | | $T_A$ = +25°C | | 34 | 42 | mA | |
| | | | $T_A$ = +85°C | | | 46 | mA | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | | $T_A$ = +25°C | | 0.016 | | V/V | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | | 0.250 | | V/V | |
| $\frac{\Delta V_{BB}}{\Delta V_{EE}}$ | Reference bias voltage compensation | | | | 0.148 | | V/V | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst-case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 5.



**NOTES:**

| | |
|---|---|
| $V_{IHmax}$ | – Maximum HIGH level input voltage (the most positive $V_{IH}$). |
| $V_{IHT}$ | – HIGH level input threshold voltage. |
| $V_{ILT}$ | – LOW level input threshold voltage. |
| $V_{ILmin}$ | – Minimum LOW level input voltage (the most negative $V_{IL}$). |
| $V_{OHmax}$ | – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition. |
| $V_{OHmin}$ | – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition. |
| $V_{OHT}$ | – HIGH level output threshold voltage with the inputs set to their respective threshold levels. |
| $V_{OLT}$ | – LOW level output threshold voltage with the inputs set to their respective threshold levels. |
| $V_{OLmax}$ | – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions. |
| $V_{OLmin}$ | – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions. |
| $V_{BB}$ | – Reference bias voltage (the internally generated reference voltage which is used to set the input and output threshold level). |

**Figure 5. Transfer Characteristics**

## AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$

| PARAMETER | $T_A = -30°C$ | | $T_A = +25°C$ | | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Typ | Max | Min | Max | | |
| $t_{PLH}$ Propagation delay<br>$t_{PHL}$ $D_n$ to $Q_n$ | 1.2<br>1.2 | 3.8<br>3.8 | 1.3<br>1.3 | 2.6<br>2.6 | 3.7<br>3.7 | 1.3<br>1.3 | 4.2<br>4.2 | ns<br>ns | Figs. 6, 7, 8 |
| $t_{PLH}$ Propagation delay<br>$t_{PHL}$ $\overline{E}$ to $Q_n$ | 1.3<br>1.3 | 4.1<br>4.1 | 1.5<br>1.5 | 3.4<br>3.4 | 4.0<br>4.0 | 1.5<br>1.5 | 4.6<br>4.6 | ns<br>ns | Figs. 6, 7, 8 |
| $t_{TLH}$ Transition time<br>$t_{THL}$ 20% to 80%, 80% to 20% | 1.3<br>1.3 | 3.5<br>3.5 | 1.3<br>1.3 | 2.5<br>2.5 | 3.5<br>3.5 | 1.3<br>1.3 | 3.5<br>3.5 | ns<br>ns | Figs. 6, 7, 8 |

## AC WAVEFORMS

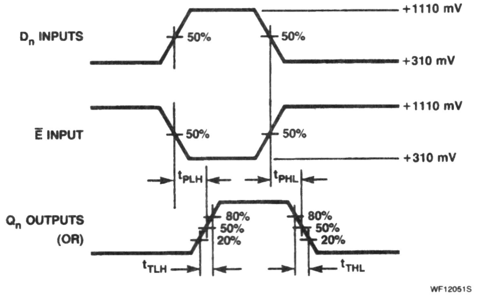
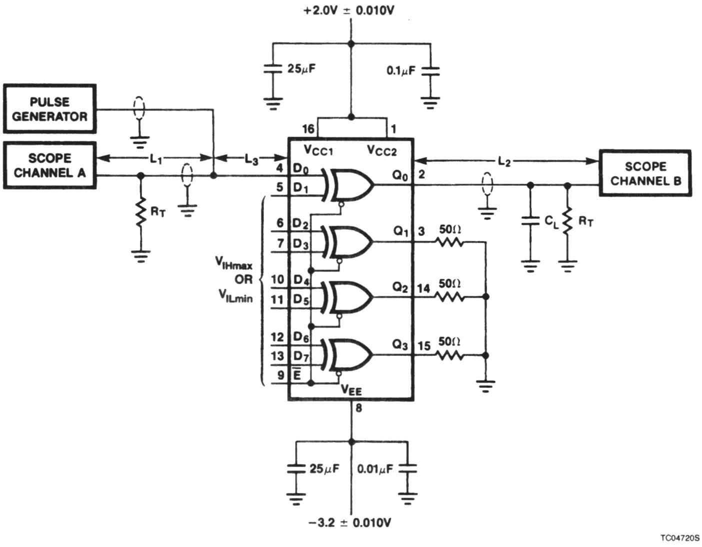


**Figure 6. Propagation Delay and Transition Times**

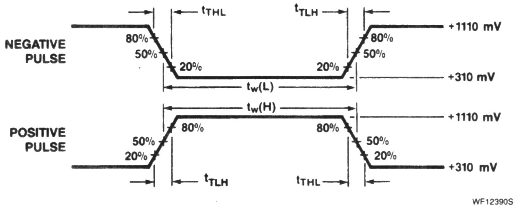
## TEST CIRCUITS AND WAVEFORMS


+2.0V ± 0.010V
25μF
0.1μF
PULSE GENERATOR
SCOPE CHANNEL A
L1
L3
L2
RT
16
1
VCC1
VCC2
4 D0
5 D1
6 D2
7 D3
10 D4
11 D5
12 D6
13 D7
9 Ē
Q0 2
Q1 3
Q2 14
Q3 15
50Ω
VIHmax OR VILmin
VEE
8
SCOPE CHANNEL B
CL
RT
25μF
0.01μF
−3.2 ± 0.010V
TC04720S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1μF and 25μF from GND to $V_{CC}$, 0.01μF and 25μF from GND to $V_{EE}$. (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T = 50\Omega$ terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance $\leqslant 3pF$.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ±1% or better.

Figure 7. AC Test Circuit for 10113


NEGATIVE PULSE
POSITIVE PULSE
tTHL
tTLH
80%
50%
20%
tw(L)
tw(H)
+1110 mV
+310 mV
WF12390S

| INPUT PULSE REQUIREMENTS<br>$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$, $V_T$ = GND (0V) | | | | | |
|---|---|---|---|---|---|
| **Family** | **Amplitude** | **Rep Rate** | **Pulse Width** | **$t_{TLH}$** | **$t_{THL}$** |
| 10K ECL | 800mVp-p | 1MHz | 500ns | 2.0 ±0.2ns | 2.0 ±0.2ns |

Figure 8. Input Pulse Definition

**Signetics**

# 10114
## Line Receiver

**Triple Differential Line Receiver**
***Product Specification***

**ECL Products**

## DESCRIPTION

The 10114 is a Triple Differential Line Receiver with low-impedance emitter-follower complementary outputs. With translated emitter-follower inputs and an active current source, it features a peak common-mode rejection voltage of ± 1V.

Furthermore, the OR outputs keep a LOW logic level whenever the inputs are left floating. Intended primarily to receive data from balanced twisted-pair lines, this device is also suitable for minicomputers, testing and instrumentation.

It can also be used as a sense amplifier for MOS RAMs as a MOS-to-ECL interface circuit, as a high-speed comparator and, having an internal reference bias voltage ($V_{BB}$) output, it can operate as a Schmitt trigger.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 10114 | 2.4ns | 28mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} = GND$; $V_{EE} = -5.2V$<br>$T_A = -30°C$ to $+85°C$ |
|---|---|
| Plastic DIP | 10114N |
| Ceramic DIP | 10114F |

## PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $\overline{D}_0$, $\overline{D}_2$, $\overline{D}_4$; $D_1$, $D_3$, $D_5$ | Data Inputs |
| $Q_1$, $Q_3$, $Q_5$ | Data Outputs (OR) |
| $\overline{Q}_0$, $\overline{Q}_2$, $\overline{Q}_4$ | Data Outputs (NOR) |
| $V_{BB}$ | Reference Bias Voltage Output |

## PIN CONFIGURATION

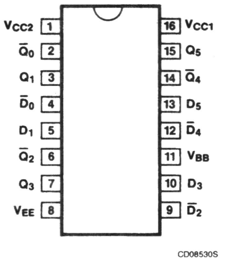

$V_{CC2}$ 1
$\overline{Q}_0$ 2
$Q_1$ 3
$\overline{D}_0$ 4
$D_1$ 5
$\overline{Q}_2$ 6
$Q_3$ 7
$V_{EE}$ 8
16 $V_{CC1}$
15 $Q_5$
14 $\overline{Q}_4$
13 $D_5$
12 $\overline{D}_4$
11 $V_{BB}$
10 $D_3$
9 $\overline{D}_2$
CD08530S

Figure 1

## LOGIC SYMBOL

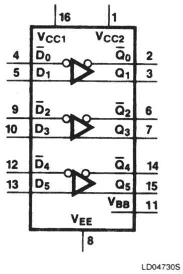

16
1
$V_{CC1}$
$V_{CC2}$
4 $\overline{D}_0$
5 $D_1$
$\overline{Q}_0$ 2
$Q_1$ 3
9 $\overline{D}_2$
10 $D_3$
$\overline{Q}_2$ 6
$Q_3$ 7
12 $\overline{D}_4$
13 $D_5$
$\overline{Q}_4$ 14
$Q_5$ 15
$V_{BB}$ 11
$V_{EE}$
8
LD04730S

Figure 2

## Line Receiver

## 10114

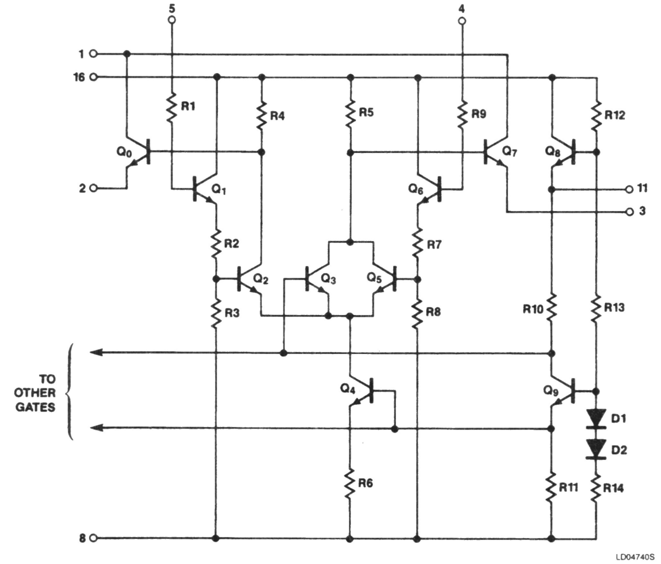
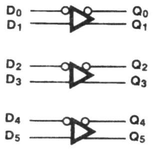

5
4
1
16
2
8
11
3
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
D1
D2
TO OTHER GATES
LD04740S

Figure 3. Circuit Diagram (One Gate)


D0
D1
Q0
Q1
D2
D3
Q2
Q3
D4
D5
Q4
Q5

WITH INPUTS $D_1$,$D_3$ AND $D_5$ CONNECTED TO $V_{BB}$ (PIN 11)

$Q_0 = D_0$
$Q_1 = \overline{D}_1$
$Q_2 = D_2$
$Q_3 = \overline{D}_2$
$Q_4 = D_4$
$Q_5 = \overline{D}_4$

LD04751S

Figure 4. Logic Diagram

**ABSOLUTE MAXIMUM RATINGS** (Operation beyond the limits set forth in this table may impair useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | | 10K ECL | UNIT |
|---|---|---|---|---|
| $V_{EE}$ | Supply voltage | | −8.0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | | 0 to $V_{EE}$ | V |
| $I_O$ | Output current | | −50 | mA |
| $T_S$ | Storage temperature | | −55 to +150 | °C |
| $T_J$ | Maximum junction temperature | Ceramic package | +165 | °C |
| | | Plastic package | +150 | °C |

# Line Receiver

# 10114

## DC OPERATING CONDITIONS

| PARAMETER | | | 10K ECL | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit Ground | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply Voltage (Negative) | | | -5.2 | | V |
| $V_{IH}$ | HIGH level input voltage | $T_A = -30°C$ | | | -890 | mV |
| | | $T_A = +25°C$ | | | -810 | mV |
| | | $T_A = +85°C$ | | | -700 | mV |
| $V_{IHT}$ | HIGH level input threshold voltage | $T_A = -30°C$ | -1205 | | | mV |
| | | $T_A = +25°C$ | -1105 | | | mV |
| | | $T_A = +85°C$ | -1035 | | | mV |
| $V_{ILT}$ | LOW level input threshold voltage | $T_A = -30°C$ | | | -1500 | mV |
| | | $T_A = +25°C$ | | | -1475 | mV |
| | | $T_A = +85°C$ | | | -1440 | mV |
| $V_{IL}$ | LOW level input voltage | $T_A = -30°C$ | -1890 | | | mV |
| | | $T_A = +25°C$ | -1850 | | | mV |
| | | $T_A = +85°C$ | -1825 | | | mV |
| $T_A$ | Operating ambient temperature | | -30 | +25 | +85 | °C |

**NOTE:**
When operating at $V_{EE}$ other than specified voltage (-5.2V), the DC and AC Characteristics will vary slightly from specified values. (See table of DC Characteristics)

## DC OPERATING CONDITIONS FOR COMMON-MODE REJECTION TEST $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V \pm 0.010V$

| PARAMETER | | | 10K ECL | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | |
| $V_{IHH}$ | $V_{IHmax} + 1.0V$ | $T_A = -30°C$ | | | +110 | mV |
| | | $T_A = +25°C$ | | | +190 | mV |
| | | $T_A = +85°C$ | | | +300 | mV |
| $V_{IHL}$ | $V_{IHmax} - 1.0V$ | $T_A = -30°C$ | | | -1890 | mV |
| | | $T_A = +25°C$ | | | -1810 | mV |
| | | $T_A = +85°C$ | | | -1700 | mV |
| $V_{ILH}$ | $V_{ILmin} + 1.0V$ | $T_A = -30°C$ | -890 | | | mV |
| | | $T_A = +25°C$ | -850 | | | mV |
| | | $T_A = +85°C$ | -825 | | | mV |
| $V_{ILL}$ | $V_{ILmin} - 1.0V$ | $T_A = -30°C$ | -2890 | | | mV |
| | | $T_A = +25°C$ | -2850 | | | mV |
| | | $T_A = +85°C$ | -2825 | | | mV |

**NOTE:**
When operating at $V_{EE}$ other than specified voltage (-5.2V), the DC and AC Characteristics will vary slightly from specified values. (See table of DC Characteristics)

**DC ELECTRICAL CHARACTERISTICS** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V$, $\pm 0.010V$, $T_A = -30°C$ to $+85°C$, output loading with $50\Omega$ to $-2.0V \pm 0.010V$, unless otherwise specified[1,3]

| PARAMETER | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | $T_A = -30°C$ | -1060 | | -890 | mV | For $\overline{Q}_n$ outputs, apply $V_{IHmax}$ to each inverting input, one at a time, with $V_{ILmin}$ applied to all other inverting inputs and $V_{BB}$ applied to all non-inverting inputs.<br>For $Q_n$ outputs, apply $V_{ILmin}$ to each inverting input, one at a time, with $V_{BB}$ applied to all non-inverting inputs and with $V_{IHmax}$ applied to all other inverting inputs.<br>(Refer to Fig. 8.) |
| | | $T_A = +25°C$ | -960 | | -810 | mV | |
| | | $T_A = +85°C$ | -890 | | -700 | mV | |
| $V_{OHT}$ | HIGH level output threshold voltage | $T_A = -30°C$ | -1080 | | | mV | For $\overline{Q}_n$ outputs, apply $V_{IHT}$ to each inverting input, one at a time, with $V_{ILmin}$ applied to allother inverting inputs and $V_{BB}$ applied to all non-inverting inputs.<br>For $Q_n$ outputs, apply $V_{ILT}$ to each inverting input, one at a time, with $V_{BB}$ applied to all non-inverting inputs and with $V_{IHmax}$ applied to all other inverting inputs.<br>(Refer to Fig. 8.) |
| | | $T_A = +25°C$ | -980 | | | mV | |
| | | $T_A = +85°C$ | -910 | | | mV | |
| $V_{OLT}$ | LOW level output threshold voltage | $T_A = -30°C$ | | | -1655 | mV | For $\overline{Q}_n$ outputs, apply $V_{ILT}$ to each inverting input, one at a time, with $V_{BB}$ applied to all non-inverting inputs and $V_{IHmax}$ applied to all other-inverting inputs.<br>For $Q_n$ outputs, apply $V_{IHT}$ to each inverting input, one at a time, with $V_{BB}$ applied to all non-inverting inputs and $V_{ILmin}$ applied to all other inverting inputs.<br>(Refer to Fig. 8.) |
| | | $T_A = +25°C$ | | | -1630 | mV | |
| | | $T_A = +85°C$ | | | -1595 | mV | |
| $V_{OL}$ | LOW level output voltage | $T_A = -30°C$ | -1890 | | -1675 | mV | For $\overline{Q}_n$ outputs, apply $V_{ILmin}$ to each inverting input, one at a time, with $V_{BB}$ applied to all non-inverting inputs and $V_{IHmax}$ applied to all other inverting inputs.<br>For $Q_n$ outputs, apply $V_{IHmax}$ to each inverting input, one at a time, with $V_{BB}$ applied to all non-inverting inputs and $V_{ILmin}$ applied to all other inverting inputs.<br>(Refer to Fig. 8.) |
| | | $T_A = +25°C$ | -1850 | | -1650 | mV | |
| | | $T_A = +85°C$ | -1825 | | -1615 | mV | |
| $I_{IH}$ | HIGH level input current | $T_A = -30°C$ | | | 70 | µA | Apply $V_{IHmax}$ to each inverting input under test one at a time, with $V_{ILmin}$ applied to all other inverting inputs and $V_{BB}$ applied to all non-inverting inputs. Apply $V_{IHmax}$ to each non-inverting input under test, one at a time, with $V_{ILmin}$ applied to all other non-inverting inputs and $V_{BB}$ applied to all inverting inputs.<br>(Refer to Fig. 8.) |
| | | $T_A = +25°C$ | | | 45 | µA | |
| | | $T_A = +85°C$ | | | 45 | µA | |
| $-I_{EE}$ | $V_{EE}$ supply current | $T_A = -30°C$ | | | 39 | mA | Apply $V_{ILmin}$ to all inverting inputs.<br>Apply $V_{BB}$ to all non-inverting inputs. |
| | | $T_A = +25°C$ | | 28 | 35 | mA | |
| | | $T_A = +85°C$ | | | 39 | mA | |

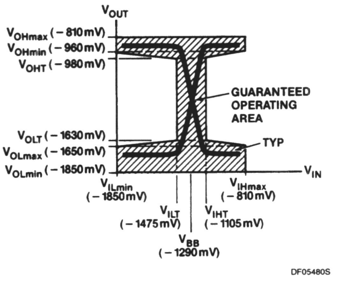
# Line Receiver　10114

## DC ELECTRICAL CHARACTERISTICS (Continued)

| PARAMETER | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] |
|---|---|---|---|---|---|---|---|
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | $T_A = +25°C$ | | 0.016 | | V/V | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | 0.250 | | V/V | |
| $\frac{\Delta V_{BB}}{\Delta V_{EE}}$ | Reference Bias voltage compensation | | | 0.148 | | V/V | |
| $V_{BB}$ | Reference voltage | $T_A = -30°C$ | −1420 | | −1280 | mV | All inverting or all non-inverting input pins are tied to the $V_{BB}$ pin during measurement. |
| | | $T_A = +25°C$ | −1350 | −1290 | −1230 | mV | |
| | | $T_A = +85°C$ | −1295 | | −1150 | mV | |
| $V_{OH}$ | HIGH level output voltage for Common-Mode Rejection Test | $T_A = -30°C$ | −1060 | | −1280 | mV | For $\overline{Q}_n$ outputs, apply $V_{IHH}$ to inverting inputs and $V_{ILH}$ to non-inverting inputs.<br>For $Q_n$ outputs, apply $V_{ILL}$ to inverting inputs and $V_{IHL}$ to non-inverting inputs. |
| | | $T_A = +25°C$ | −960 | | −810 | mV | |
| | | $T_A = +85°C$ | −890 | | −700 | mV | |
| $V_{OL}$ | LOW level output voltage for Common-Mode Rejection Test | $T_A = -30°C$ | −1890 | | −1675 | mV | For $\overline{Q}_n$ outputs, apply $V_{ILH}$ to inverting inputs and $V_{IHH}$ to non-inverting inputs.<br>For $Q_n$ outputs, apply $V_{IHL}$ to inverting inputs and $V_{ILL}$ to non-inverting inputs. |
| | | $T_A = +25°C$ | −1850 | | −1650 | mV | |
| | | $T_A = +85°C$ | −1825 | | −1615 | mV | |
| $-I_{CBO}$ | Input leakage current | $T_A = -30°C$ | | | 1.5 | µA | Apply $V_{EE}$ to each inverting input under test, one at a time, with $V_{ILmin}$ applied to all other inverting inputs and $V_{BB}$ applied to all non-inverting inputs (Refer to Fig. 8.) |
| | | $T_A = +25°C$ | | | 1.0 | µA | |
| | | $T_A = +85°C$ | | | 1.0 | µA | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst-case testing guidelines, refer to Section 3, Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 5.



**NOTES:**

$V_{IHmax}$ – Maximum HIGH level input voltage (the most positive $V_{IH}$).
$V_{IHT}$ – HIGH level input threshold voltage.
$V_{ILT}$ – LOW level input threshold voltage.
$V_{ILmin}$ – Minimum LOW level input voltage (the most negative $V_{IL}$).
$V_{OHmax}$ – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition.
$V_{OHmin}$ – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition.
$V_{OHT}$ – HIGH level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLT}$ – LOW level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLmax}$ – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions.
$V_{OLmin}$ – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions.
$V_{BB}$ – Reference bias voltage (the internally generated reference voltage which is used to set the input and output threshold level).

Figure 5. Transfer Characteristics

## AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$

| PARAMETER | $T_A = -30°C$ | | $T_A = +25°C$ | | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Typ | Max | Min | Max | | |
| $t_{PLH}$ Propagation delay | 1.0 | 4.4 | 1.0 | 2.4 | 4.0 | 0.9 | 4.3 | ns | Figs. 6, 7, 9 |
| $t_{PHL}$ $D_n$ to $Q_n$ | 1.0 | 4.4 | 1.0 | 2.4 | 4.0 | 0.9 | 4.3 | ns | |
| $t_{PLH}$ Propagation delay | 1.0 | 4.4 | 1.0 | 2.4 | 4.0 | 0.9 | 4.3 | ns | Figs. 6, 7, 9 |
| $t_{PHL}$ $\overline{D}_n$ to $\overline{Q}_n$ | 1.0 | 4.4 | 1.0 | 2.4 | 4.0 | 0.9 | 4.3 | ns | |
| $t_{TLH}$ Transition time | 1.5 | 3.8 | 1.5 | 2.1 | 3.5 | 1.5 | 3.7 | ns | Figs. 6, 7, 9 |
| $t_{THL}$ 20% to 80%, 80% to 20% | 1.5 | 3.8 | 1.5 | 2.1 | 3.5 | 1.5 | 3.7 | ns | |

## AC WAVEFORMS

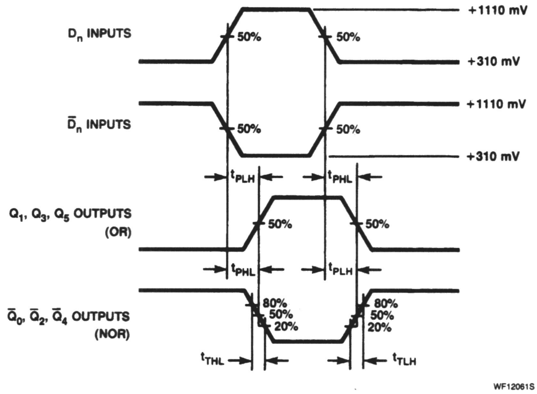
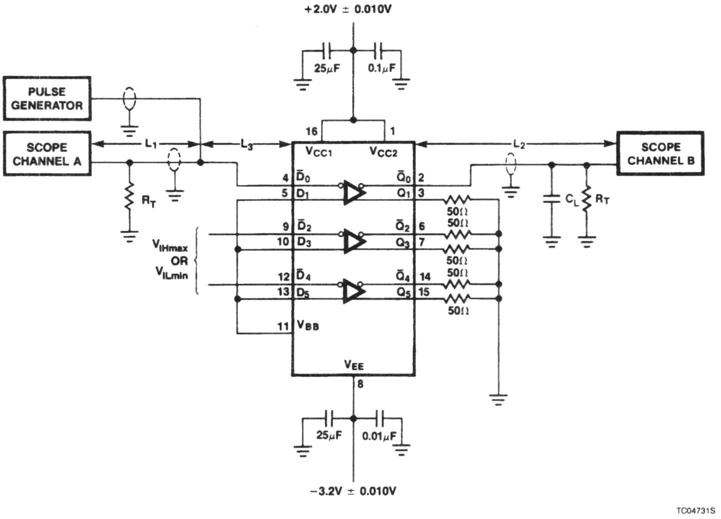

$D_n$ INPUTS
+1110 mV
50%
50%
+310 mV
$\overline{D}_n$ INPUTS
+1110 mV
50%
50%
+310 mV
$t_{PLH}$
$t_{PHL}$
$Q_1$, $Q_3$, $Q_5$ OUTPUTS (OR)
50%
50%
$t_{PHL}$
$t_{PLH}$
$\overline{Q}_0$, $\overline{Q}_2$, $\overline{Q}_4$ OUTPUTS (NOR)
80%
50%
20%
80%
50%
20%
$t_{THL}$
$t_{TLH}$
WF12061S

Figure 6. Propagation Delay and Transition Times

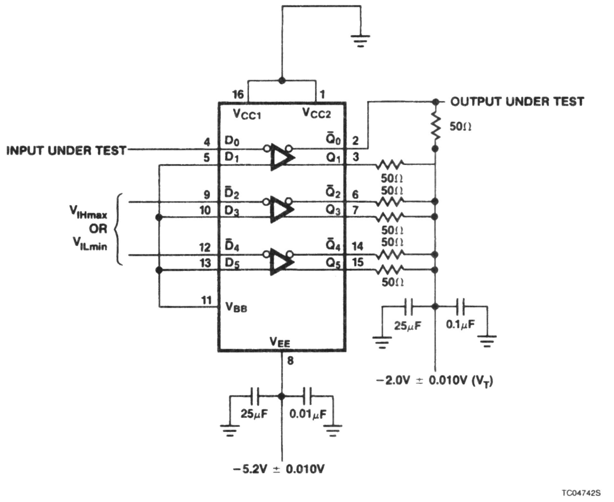
## TEST CIRCUITS AND WAVEFORMS


+2.0V ± 0.010V
25μF
0.1μF
PULSE GENERATOR
SCOPE CHANNEL A
L1
L3
L2
SCOPE CHANNEL B
$R_T$
$C_L$
$R_T$
16
1
$V_{CC1}$
$V_{CC2}$
4 $\bar{D}_0$
5 $D_1$
9 $\bar{D}_2$
10 $D_3$
12 $\bar{D}_4$
13 $D_5$
11 $V_{BB}$
$\bar{Q}_0$ 2
$Q_1$ 3
$\bar{Q}_2$ 6
$Q_3$ 7
$\bar{Q}_4$ 14
$Q_5$ 15
50Ω
50Ω
50Ω
50Ω
50Ω
$V_{IHmax}$ OR $V_{ILmin}$
$V_{EE}$
8
25μF
0.01μF
−3.2V ± 0.010V
TC04731S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1μF and 25μF from GND to $V_{CC}$, 0.01μF and 25μF from GND to $V_{EE}$ (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than ¼ inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the logic function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin and the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed ¼ inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than ¼ inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance ≤ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed ¼ inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ±1% or better.

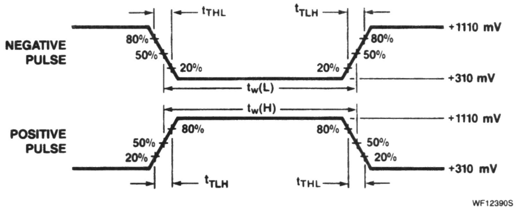
Figure 7. AC Test Circuit for 10114


16
1
$V_{CC1}$
$V_{CC2}$
OUTPUT UNDER TEST
50Ω
INPUT UNDER TEST
4 $D_0$
5 $D_1$
9 $\bar{D}_2$
10 $D_3$
12 $\bar{D}_4$
13 $D_5$
11 $V_{BB}$
$\bar{Q}_0$ 2
$Q_1$ 3
$\bar{Q}_2$ 6
$Q_3$ 7
$\bar{Q}_4$ 14
$Q_5$ 15
50Ω
50Ω
50Ω
50Ω
50Ω
$V_{IHmax}$ OR $V_{ILmin}$
25μF
0.1μF
−2.0V ± 0.010V ($V_T$)
$V_{EE}$
8
25μF
0.01μF
−5.2V ± 0.010V
TC04742S

**NOTES:**

1. $V_{CC1} = V_{CC2}$ = 0V (GND), $V_{EE} = -5.2V \pm 0.010V$.
2. Decoupling 0.01μF and 25μF from GND to $V_{EE}$, 0.1μF and 25μF from GND to $V_T$ (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT, and lead length should be kept to less than ¼ inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the logic function required.
4. All unused outputs are loaded with 50Ω to $V_T$.
5. All 50Ω resistors should have tolerance of ±1% or better.

Figure 8. DC Test Circuit for 10K ECL


$t_{THL}$
$t_{TLH}$
NEGATIVE PULSE
80%
50%
20%
20%
80%
50%
+1110 mV
+310 mV
$t_w(L)$
$t_w(H)$
+1110 mV
POSITIVE PULSE
80%
80%
50%
20%
50%
20%
+310 mV
$t_{TLH}$
$t_{THL}$
WF12390S

| INPUT PULSE REQUIREMENTS<br>$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$, $V_T$ = GND (0V) | | | | | |
|---|---|---|---|---|---|
| **Family** | **Amplitude** | **Rep Rate** | **Pulse Width** | $t_{TLH}$ | $t_{THL}$ |
| 10K ECL | 800mVp-p | 1MHz | 500ns | 2.0 ±0.2ns | 2.0 ±0.2ns |

**Figure 9. Input Pulse Definition**

Signetics

# 10115
## Line Receiver

**Quad Differential Line Receiver**
***Product Specification***

**ECL Products**

## DESCRIPTION

The 10115 is a Quad Differential Line Receiver intended for use in sensing signals over long lines. The base Reference Bias Voltage ($V_{BB}$) makes the device useful in other applications where a stable reference voltage is necessary. It features a peak common-mode rejection voltage of ± 1V.

One input from any unused amplifier in a package must be tied to $V_{BB}$.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 10115 | 2.0ns | 18mA |

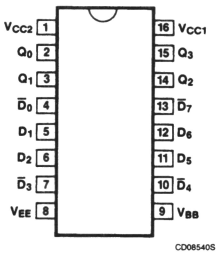
## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V$<br>$T_A = -30°C$ to $+85°C$ |
|---|---|
| Plastic DIP | 10115N |
| Ceramic DIP | 10115F |

## PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_1$, $D_2$, $D_5$, $D_6$;<br>$\overline{D}_0$, $\overline{D}_3$, $\overline{D}_4$, $\overline{D}_7$ | Data Inputs |
| $V_{BB}$ | Reference Bias Voltage Output |
| $Q_0 - Q_3$ | Data Outputs |

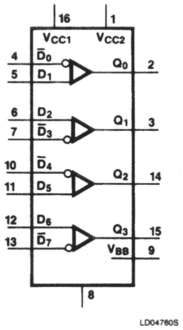
## PIN CONFIGURATION



VCC2 1
Q0 2
Q1 3
D̄0 4
D1 5
D2 6
D̄3 7
VEE 8
16 VCC1
15 Q3
14 Q2
13 D̄7
12 D6
11 D5
10 D̄4
9 VBB
CD08540S

Figure 1

## LOGIC SYMBOL



16
1
VCC1
VCC2
4 D̄0
5 D1
Q0 2
6 D2
7 D̄3
Q1 3
10 D̄4
11 D5
Q2 14
12 D6
13 D̄7
Q3 15
VBB 9
8
LD04760S

Figure 2

# Line Receiver 10115

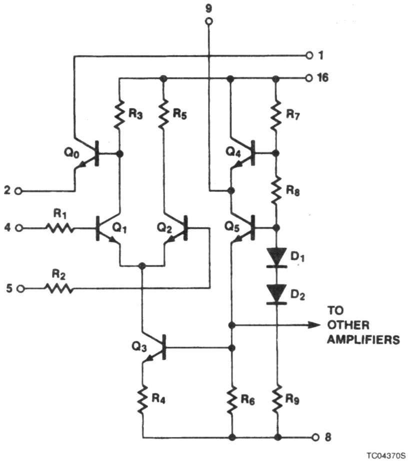
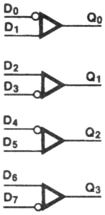

9
1
16
R3
R5
R7
Q0
Q4
2
R8
R1
4
Q1
Q2
Q5
D1
R2
5
D2
TO OTHER AMPLIFIERS
Q3
R4
R6
R9
8
TC04370S

Figure 3. Circuit Diagram (One Amplifier)


D0
D1
Q0
D2
D3
Q1
D4
D5
Q2
D6
D7
Q3
LD05292S

WITH INPUTS $D_1$, $D_2$, $D_5$, $D_6$
CONNECTED TO $V_{BB}$:
$Q_0 = \overline{D}_0$ $Q_2 = \overline{D}_4$
$Q_1 = \overline{D}_3$ $Q_3 = \overline{D}_7$
POSITIVE LOGIC: HIGH STATE = 1
LOW STATE = 0

Figure 4. Logic Diagram

**ABSOLUTE MAXIMUM RATINGS** (Operation beyond the limits set forth in this table may impair useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | | 10K ECL | UNIT |
|---|---|---|---|---|
| $V_{EE}$ | Supply voltage | | -8.0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | | 0 to $V_{EE}$ | V |
| $I_O$ | Output current | | -50 | mA |
| $T_S$ | Storage temperature | | -55 to +150 | °C |
| $T_J$ | Maximum junction temperature | Ceramic package | +165 | °C |
| | | Plastic package | +150 | °C |

# Line Receiver 10115

## DC OPERATING CONDITIONS

| PARAMETER | | | 10K ECL | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | −5.2 | | V |
| $V_{IH}$ | HIGH level input voltage | $T_A = -30°C$ | | | −890 | mV |
| | | $T_A = +25°C$ | | | −810 | mV |
| | | $T_A = +85°C$ | | | −700 | mV |
| $V_{IHT}$ | HIGH level input threshold voltage | $T_A = -30°C$ | −1205 | | | mV |
| | | $T_A = +25°C$ | −1105 | | | mV |
| | | $T_A = +85°C$ | −1035 | | | mV |
| $V_{ILT}$ | LOW level input threshold voltage | $T_A = -30°C$ | | | −1500 | mV |
| | | $T_A = +25°C$ | | | −1475 | mV |
| | | $T_A = +85°C$ | | | −1440 | mV |
| $V_{IL}$ | LOW level input voltage | $T_A = -30°C$ | −1890 | | | mV |
| | | $T_A = +25°C$ | −1850 | | | mV |
| | | $T_A = +85°C$ | −1825 | | | mV |
| $T_A$ | Operating ambient temperature | | −30 | +25 | +85 | °C |

**NOTE:**
When operating at $V_{EE}$ other than specified voltage (−5.2V), the DC and AC Characteristics will vary slightly from specified values.
(See table of DC Characteristics)

## DC OPERATING CONDITIONS FOR COMMON-MODE REJECTION TEST $V_{CC1} = V_{CC2} = GND, V_{EE} = -5.2V \pm 0.010V$

| PARAMETER | | | 10K ECL | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | |
| $V_{IHH}$ | $V_{IHmax} + 1.0V$ | $T_A = -30°C$ | | | +110 | mV |
| | | $T_A = +25°C$ | | | +190 | mV |
| | | $T_A = +85°C$ | | | +300 | mV |
| $V_{IHL}$ | $V_{IHmax} - 1.0V$ | $T_A = -30°C$ | | | −1890 | mV |
| | | $T_A = +25°C$ | | | −1810 | mV |
| | | $T_A = +85°C$ | | | −1700 | mV |
| $V_{ILH}$ | $V_{ILmin} + 1.0V$ | $T_A = -30°C$ | −890 | | | mV |
| | | $T_A = +25°C$ | −850 | | | mV |
| | | $T_A = +85°C$ | −825 | | | mV |
| $V_{ILL}$ | $V_{ILmin} - 1.0V$ | $T_A = -30°C$ | −2890 | | | mV |
| | | $T_A = +25°C$ | −2850 | | | mV |
| | | $T_A = +85°C$ | −2825 | | | mV |

**NOTE:**
When operating at $V_{EE}$ other than specified voltage (−5.2V), the DC and AC Characteristics will vary slightly from specified values.
(See table of DC Characteristics)

**DC ELECTRICAL CHARACTERISTICS** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$, output loading with 50Ω to −2.0V ±0.010V unless otherwise specified[1,3]

| PARAMETER | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | $T_A = -30°C$ | −1060 | | −890 | mV | Apply $V_{ILmin}$ to each inverting input, one at a time, with $V_{IHmax}$ applied to all other inverting inputs and $V_{BB}$ applied to all non-inverting inputs. Apply $V_{IHmax}$ to each non-inverting input, one at a time, with $V_{ILmin}$ applied to all other non-inverting inputs and with $V_{BB}$ applied to all inverting inputs. (Refer to Fig. 8) |
| | | $T_A = +25°C$ | −960 | | −810 | mV | |
| | | $T_A = +85°C$ | −890 | | −700 | mV | |
| $V_{OHT}$ | HIGH level output threshold voltage | $T_A = -30°C$ | −1080 | | | mV | Apply $V_{ILT}$ to each inverting input, one at a time, with $V_{ILmin}$ applied to all other inverting inputs and $V_{BB}$ applied to all non-inverting inputs. Apply $V_{IHT}$ to each non-inverting input, one at a time, with $V_{ILmin}$ applied to all other non-inverting inputs and with $V_{BB}$ applied to all inverting inputs. (Refer to Fig. 8) |
| | | $T_A = +25°C$ | −980 | | | mV | |
| | | $T_A = +85°C$ | −910 | | | mV | |
| $V_{OLT}$ | LOW level output threshold voltage | $T_A = -30°C$ | | | −1655 | mV | Apply $V_{IHT}$ to each inverting input, one at a time, with $V_{ILmin}$ applied to all other inverting inputs and $V_{BB}$ applied to all non-inverting inputs. Apply $V_{ILT}$ to each non-inverting input, one at a time, with $V_{ILmin}$ applied to all other non-inverting inputs and $V_{BB}$ applied to all inverting inputs. (Refer to Fig. 8) |
| | | $T_A = +25°C$ | | | −1630 | mV | |
| | | $T_A = +85°C$ | | | −1595 | mV | |
| $V_{OL}$ | LOW level output voltage | $T_A = -30°C$ | −1890 | | −1675 | mV | Apply $V_{IHmax}$ to each inverting input, one at a time, with $V_{ILmin}$ applied to all other inverting inputs and $V_{BB}$ applied to all non-inverting inputs. Apply $V_{ILmin}$ to each non-inverting input, one at a time, with $V_{IHmax}$ applied to all other non-inverting inputs and $V_{BB}$ applied to all inverting inputs. (Refer to Fig. 8) |
| | | $T_A = +25°C$ | −1850 | | −1650 | mV | |
| | | $T_A = +85°C$ | −1825 | | −1615 | mV | |
| $I_{IH}$ | HIGH level input current | $T_A = -30°C$ | | | 150 | μA | Apply $V_{IHmax}$ to each inverting input under test one at a time, with $V_{ILmin}$ applied to all other inverting inputs and $V_{BB}$ applied to all non-inverting inputs. (Refer to Fig. 8) |
| | | $T_A = +25°C$ | | | 95 | μA | |
| | | $T_A = +85°C$ | | | 95 | μA | |
| $-I_{EE}$ | $V_{EE}$ supply current | $T_A = -30°C$ | | | 29 | mA | Apply $V_{ILmin}$ to all inverting inputs and $V_{BB}$ to all non-inverting inputs. |
| | | $T_A = +25°C$ | | 18 | 26 | mA | |
| | | $T_A = +85°C$ | | | 29 | mA | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | $T_A = +25°C$ | | 0.016 | | V/V | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | 0.250 | | V/V | |
| $\frac{\Delta V_{BB}}{\Delta V_{EE}}$ | Reference bias voltage compensation | | | 0.140 | | V/V | |
| $V_{BB}$ | Reference voltage | $T_A = -30°C$ | −1420 | | −1280 | mV | All inverting or all non-inverting input pins are tied to the $V_{BB}$ pin during measurement. |
| | | $T_A = +25°C$ | −1350 | −1290 | −1230 | mV | |
| | | $T_A = +85°C$ | −1295 | | −1150 | mV | |
| $V_{OH}$ | HIGH level output voltage for Common-Mode Rejection Test | $T_A = -30°C$ | −1060 | | −890 | mV | Apply $V_{IHH}$ to non-inverting inputs and $V_{ILH}$ to inverting inputs. |
| | | $T_A = +25°C$ | −960 | | −810 | mV | |
| | | $T_A = +85°C$ | −890 | | −700 | mV | |
| $V_{OL}$ | LOW level output voltage for Common-Mode Rejection Test | $T_A = -30°C$ | −1890 | | −1675 | mV | Apply $V_{IHH}$ to inverting inputs and $V_{ILH}$ to non-inverting inputs. |
| | | $T_A = +25°C$ | −1850 | | −1650 | mV | |
| | | $T_A = +85°C$ | −1825 | | −1615 | mV | |

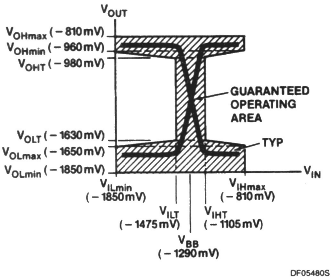
## Line Receiver 10115

### DC ELECTRICAL CHARACTERISTICS (Continued)

| PARAMETER | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] |
|---|---|---|---|---|---|---|
| $-I_{CBO}$ Input leakage current | $T_A = -30°C$ | | | 1.5 | μA | Apply $V_{EE}$ to each inverting input under test, one at a time, with $V_{ILmin}$ applied to all other inverting inputs and $V_{BB}$ applied to all non-inverting inputs. (Refer to Fig. 8) |
| | $T_A = +25°C$ | | | 1.0 | μA | |
| | $T_A = +85°C$ | | | 1.0 | μA | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst-case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 5.



**NOTES:**

$V_{IHmax}$ – Maximum HIGH level input voltage (the most positive $V_{IH}$).
$V_{IHT}$ – HIGH level input threshold voltage.
$V_{ILT}$ – LOW level input threshold voltage.
$V_{ILmin}$ – Minimum LOW level input voltage (the most negative $V_{IL}$).
$V_{OHmax}$ – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition.
$V_{OHmin}$ – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition.
$V_{OHT}$ – HIGH level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLT}$ – LOW level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLmax}$ – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions.
$V_{OLmin}$ – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions.
$V_{BB}$ – Reference bias voltage (the internally generated reference voltage which is used to set the input and output threshold level).

**Figure 5. Transfer Characteristics**

### AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$

| PARAMETER | $T_A = -30°C$ | | $T_A = +25°C$ | | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Typ | Max | Min | Max | | |
| $t_{PLH}$ Propagation delay<br>$t_{PHL}$ $D_n$, $\overline{D}_n$ to $Q_n$ | 1.0<br>1.0 | 3.1<br>3.1 | 1.0<br>1.0 | 2.0<br>2.0 | 2.9<br>2.9 | 1.0<br>1.0 | 3.3<br>3.3 | ns | Figs. 6, 7, 9 |
| $t_{TLH}$ Transition time<br>$t_{THL}$ 20% to 80%, 80% to 20% | 1.1<br>1.1 | 3.6<br>3.6 | 1.1<br>1.1 | 2.0<br>2.0 | 3.3<br>3.3 | 1.1<br>1.1 | 3.7<br>3.7 | ns | Figs. 6, 7, 9 |

## AC WAVEFORMS

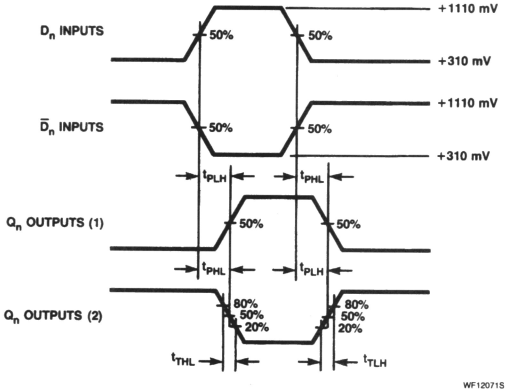
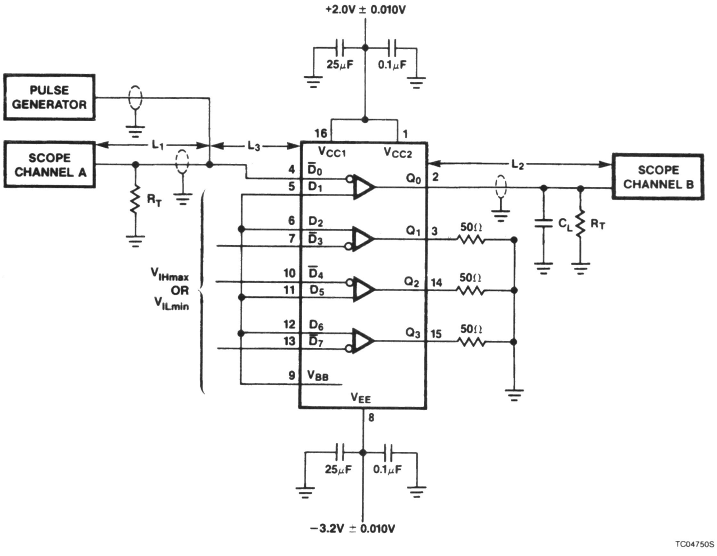

$D_n$ INPUTS
$\overline{D}_n$ INPUTS
$Q_n$ OUTPUTS (1)
$Q_n$ OUTPUTS (2)
50%
+1110 mV
+310 mV
$t_{PLH}$
$t_{PHL}$
80%
20%
$t_{THL}$
$t_{TLH}$
WF12071S

Figure 6. Propagation Delay and Transition Times

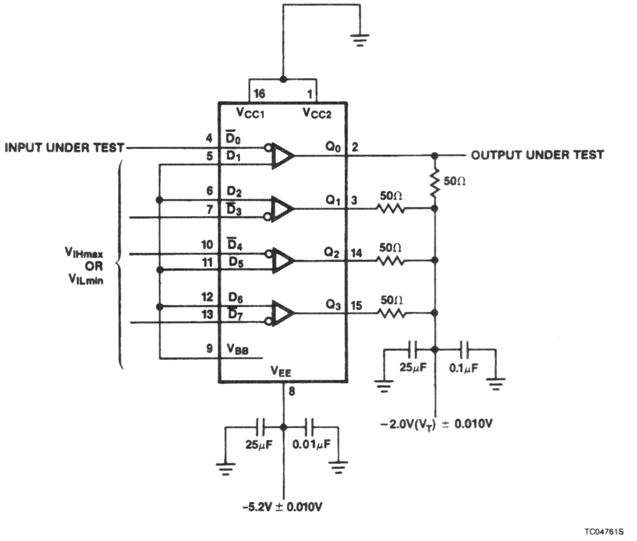
## TEST CIRCUITS AND WAVEFORMS


+2.0V ± 0.010V
25μF
0.1μF
PULSE GENERATOR
SCOPE CHANNEL A
SCOPE CHANNEL B
$L_1$
$L_2$
$L_3$
$R_T$
$C_L$
$V_{CC1}$
$V_{CC2}$
$\overline{D}_0$
$D_1$
$D_2$
$\overline{D}_3$
$\overline{D}_4$
$D_5$
$D_6$
$\overline{D}_7$
$V_{BB}$
$V_{EE}$
$Q_0$
$Q_1$
$Q_2$
$Q_3$
50Ω
$V_{IHmax}$ OR $V_{ILmin}$
−3.2V ± 0.010V
TC04750S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$
2. Decoupling 0.1μF and 25μF from GND to $V_{CC}$, 0.01μF and 25μF from GND to $V_{EE}$. (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance $\leqslant$ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.

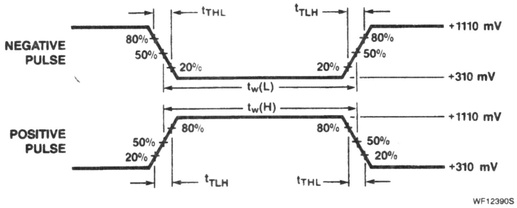
Figure 7. AC Test Circuit for 10K ECL


16
1
$V_{CC1}$
$V_{CC2}$
INPUT UNDER TEST
4 $\overline{D}_0$
5 $D_1$
6 $D_2$
7 $\overline{D}_3$
10 $\overline{D}_4$
11 $D_5$
12 $D_6$
13 $\overline{D}_7$
9 $V_{BB}$
$V_{IHmax}$ OR $V_{ILmin}$
$Q_0$ 2
$Q_1$ 3
$Q_2$ 14
$Q_3$ 15
OUTPUT UNDER TEST
50Ω
50Ω
50Ω
50Ω
25μF
0.1μF
$-2.0V(V_T) \pm 0.010V$
$V_{EE}$
8
25μF
0.01μF
$-5.2V \pm 0.010V$
TC04761S

**NOTES:**

1. $V_{CC1} = V_{CC2} =$ GND (0V), $V_{EE} = -5.2V \pm 0.010V$.
2. Decoupling 0.01μF and 25μF from GND to $V_{EE}$, 0.1μF and 25μF from GND to $V_T$ (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT, and lead length should be kept to less than ¼ inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to $V_T$.
5. All 50Ω resistors should have tolerance of ±1% or better.

**Figure 8. DC Test Circuit for 10115**


NEGATIVE PULSE
POSITIVE PULSE
$t_{THL}$
$t_{TLH}$
80%
50%
20%
$t_w(L)$
$t_w(H)$
+1110 mV
+310 mV
WF12390S

| INPUT PULSE REQUIREMENTS<br>$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$, $V_T =$ GND (0V) | | | | | |
|---|---|---|---|---|---|
| **Family** | **Amplitude** | **Rep Rate** | **Pulse Width** | **$t_{TLH}$** | **$t_{THL}$** |
| 10K ECL | 800mVp-p | 1MHz | 500ns | 2.0 ±0.2ns | 2.0 ±0.2ns |

**Figure 9. Input Pulse Definition**

**Signetics**

# 10116
## Line Receiver

**Triple Differential Line Receiver**
***Product Specification***

**ECL Products**

## DESCRIPTION

The 10116 is a Triple Differential Line Receiver with low-impedance emitter-follower complementary outputs.

It features a common-mode rejection of ± 1V.

Intended primarily to receive data from twisted-pair lines, this device is also suitable for minicomputers, testing and instrumentation. It can also be used as a sense amplifier for MOS RAMs as a MOS-to-ECL interface circuit; as a high-speed comparator and having an internal reference supply voltage ($V_{BB}$) output, it can operate as a Schmitt Trigger.

One input from any unused amplifer in a package must be tied to $V_{BB}$.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 10116 | 2.4ns | 17mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V$ $T_A = -30°C$ to $+85°C$ |
|---|---|
| Plastic DIP | 10116N |
| Ceramic DIP | 10116F |

## PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $\overline{D}_0, \overline{D}_2, \overline{D}_4$; $D_1, D_3, D_5$ | Data Inputs |
| $V_{BB}$ | Reference Bias Voltage Output |
| $Q_1, Q_3, Q_5$ | Data Outputs (OR) |
| $\overline{Q}_0, \overline{Q}_2, \overline{Q}_4$ | Data Outputs (NOR) |

## PIN CONFIGURATION

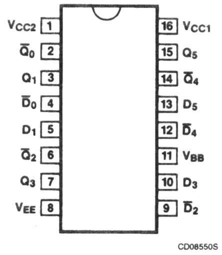

VCC2 1
Q̄0 2
Q1 3
D̄0 4
D1 5
Q̄2 6
Q3 7
VEE 8
16 VCC1
15 Q5
14 Q̄4
13 D5
12 D̄4
11 VBB
10 D3
9 D̄2
CD08550S

Figure 1

## LOGIC SYMBOL

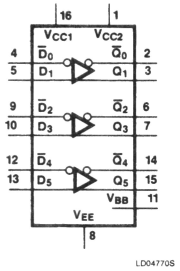

16
1
VCC1
VCC2
4
D̄0
Q̄0
2
5
D1
Q1
3
9
D̄2
Q̄2
6
10
D3
Q3
7
12
D̄4
Q̄4
14
13
D5
Q5
15
VBB
11
VEE
8
LD04770S

Figure 2

## Line Receiver

## 10116

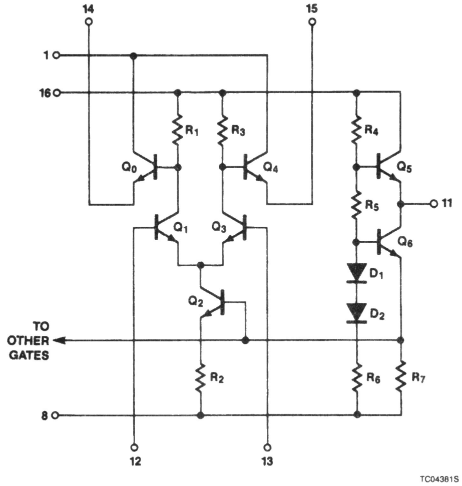
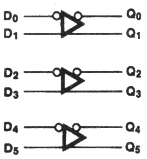

14
15
1
16
R1
R3
R4
Q0
Q4
Q5
R5
11
Q1
Q3
Q6
D1
Q2
D2
TO OTHER GATES
R2
R6
R7
8
12
13
TC04381S

Figure 3. Circuit Diagram (One Amplifier)


D0
D1
Q0
Q1
D2
D3
Q2
Q3
D4
D5
Q4
Q5

WITH INPUTS $D_1$,$D_3$ AND $D_5$ CONNECTED TO $V_{BB}$ (PIN 11)

$Q_0 = D_0$
$Q_1 = \overline{D}_0$
$Q_2 = D_2$
$Q_3 = \overline{D}_2$
$Q_4 = D_4$
$Q_5 = \overline{D}_4$

Positive logic:
HIGH state = 1
LOW state = 0

LD05301S

Figure 4. Logic Diagram

**ABSOLUTE MAXIMUM RATINGS** (Operation beyond the limits set forth in this table may impair useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | | 10K ECL | UNIT |
|---|---|---|---|---|
| $V_{EE}$ | Supply voltage | | −8.0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | | 0 to $V_{EE}$ | V |
| $I_O$ | Output current | | −50 | mA |
| $T_S$ | Storage temperature | | −55 to +150 | °C |
| $T_J$ | Maximum junction temperature | Ceramic package | +165 | °C |
| | | Plastic package | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | 10K ECL | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | -5.2 | | V |
| $V_{IH}$ | HIGH level input voltage | $T_A = -30°C$ | | | -890 | mV |
| | | $T_A = +25°C$ | | | -810 | mV |
| | | $T_A = +85°C$ | | | -700 | mV |
| $V_{IHT}$ | HIGH level input threshold voltage | $T_A = -30°C$ | -1205 | | | mV |
| | | $T_A = +25°C$ | -1105 | | | mV |
| | | $T_A = +85°C$ | -1035 | | | mV |
| $V_{ILT}$ | LOW level input threshold voltage | $T_A = -30°C$ | | | -1500 | mV |
| | | $T_A = +25°C$ | | | -1475 | mV |
| | | $T_A = +85°C$ | | | -1440 | mV |
| $V_{IL}$ | LOW level input voltage | $T_A = -30°C$ | -1890 | | | mV |
| | | $T_A = +25°C$ | -1850 | | | mV |
| | | $T_A = +85°C$ | -1825 | | | mV |
| $T_A$ | Operating ambient temperature | | -30 | +25 | +85 | °C |

**NOTE:**
When operating at $V_{EE}$ other than specified voltage (-5.2V), the DC and AC Characteristics will vary slightly from specified values.
(See table of DC Characteristics)

## DC OPERATING CONDITIONS FOR COMMON-MODE REJECTION TEST $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V \pm 0.010V$

| PARAMETER | | | 10K ECL | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | |
| $V_{IHH}$ | $V_{IHmax} + 1.0V$ | $T_A = -30°C$ | | | +110 | mV |
| | | $T_A = +25°C$ | | | +190 | mV |
| | | $T_A = +85°C$ | | | +300 | mV |
| $V_{IHL}$ | $V_{IHmax} - 1.0V$ | $T_A = -30°C$ | | | -1890 | mV |
| | | $T_A = +25°C$ | | | -1810 | mV |
| | | $T_A = +85°C$ | | | -1700 | mV |
| $V_{ILH}$ | $V_{ILmin} + 1.0V$ | $T_A = -30°C$ | -890 | | | mV |
| | | $T_A = +25°C$ | -850 | | | mV |
| | | $T_A = +85°C$ | -825 | | | mV |
| $V_{ILL}$ | $V_{ILmin} - 1.0V$ | $T_A = -30°C$ | -2890 | | | mV |
| | | $T_A = +25°C$ | -2850 | | | mV |
| | | $T_A = +85°C$ | -2825 | | | mV |

**NOTE:**
When operating at $V_{EE}$ other than specified voltage (-5.2V), the DC and AC Characteristics will vary slightly from specified values.
(See table of DC Characteristics)

**DC ELECTRICAL CHARACTERISTICS** $V_{CC1} = V_{CC2}$ = GND, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$, output loading with 50Ω to −2.0V ±0.010V, unless otherwise specified[1,3]

| PARAMETER | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | $T_A = -30°C$ | −1060 | | −890 | mV | For $Q_n$ outputs, apply $V_{ILmin}$ to each inverting input, one at a time, with $V_{IHmax}$ applied to all other inverting inputs and $V_{BB}$ applied to all non-inverting inputs. For $\overline{Q}_n$ outputs, apply $V_{IHmax}$ to each inverting input, one at a time, with $V_{ILmin}$ applied to all other inverting inputs and $V_{BB}$ applied to all non-inverting inputs. (Refer to Fig. 8.) |
| | | $T_A = +25°C$ | −960 | | −810 | mV | |
| | | $T_A = +85°C$ | −890 | | −700 | mV | |
| $V_{OHT}$ | HIGH level output threshold voltage | $T_A = -30°C$ | −1080 | | | mV | For $Q_n$ outputs, apply $V_{ILT}$ to each inverting input, one at a time, with $V_{IHmax}$ applied to all other inverting inputs and $V_{BB}$ applied to all non-inverting inputs. For $\overline{Q}_n$ outputs, apply $V_{IHT}$ to each inverting input, one at a time, with $V_{ILmin}$ applied to all other inverting inputs and $V_{BB}$ applied to all non-inverting inputs. (Refer to Fig. 8.) |
| | | $T_A = +25°C$ | −980 | | | mV | |
| | | $T_A = +85°C$ | −910 | | | mV | |
| $V_{OLT}$ | LOW level output threshold voltage | $T_A = -30°C$ | | | −1655 | mV | For $Q_n$ outputs, apply $V_{IHT}$ to each inverting input, one at a time, with $V_{ILmin}$ applied to all other inverting inputs and $V_{BB}$ applied to all non-inverting inputs. For $\overline{Q}_n$ outputs, apply $V_{ILT}$ to each inverting input, one at a time, with $V_{IHmax}$ applied to all other inverting inputs and $V_{BB}$ applied to all non-inverting inputs. (Refer to Fig. 8.) |
| | | $T_A = +25°C$ | | | −1630 | mV | |
| | | $T_A = +85°C$ | | | −1595 | mV | |
| $V_{OL}$ | LOW level output voltage | $T_A = -30°C$ | −1890 | | −1675 | mV | For $Q_n$ outputs apply $V_{IHmax}$ to each inverting input, one at a time, with $V_{ILmin}$ applied to all other inverting inputs and $V_{BB}$ applied to all non-inverting inputs. For $\overline{Q}_n$ outputs, apply $V_{ILmin}$ to each inverting input, one at a time, with $V_{IHmax}$ applied to all other inverting inputs and $V_{BB}$ applied to all non-inverting inputs. (Refer to Fig. 8.) |
| | | $T_A = +25°C$ | −1850 | | −1650 | mV | |
| | | $T_A = +85°C$ | −1825 | | −1615 | mV | |
| $I_{IH}$ | HIGH level input current | $T_A = -30°C$ | | | 150 | µA | Apply $V_{IHmax}$ to each inverting input under test one at a time, with $V_{ILmin}$ applied to all other inverting inputs and $V_{BB}$ applied to all non-inverting inputs. Apply $V_{IHmax}$ to each non-inverting input under test, one at a time, with $V_{ILmin}$ applied to all other non-inverting inputs and $V_{BB}$ applied to all inverting inputs. (Refer to Fig. 8.) |
| | | $T_A = +25°C$ | | | 95 | µA | |
| | | $T_A = +85°C$ | | | 95 | µA | |
| $-I_{EE}$ | $V_{EE}$ supply current | $T_A = -30°C$ | | | 23 | mA | Apply $V_{ILmin}$ to all inverting inputs.<br>Apply $V_{BB}$ to all non-inverting inputs. |
| | | $T_A = +25°C$ | | 17 | 21 | mA | |
| | | $T_A = +85°C$ | | | 23 | mA | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | $T_A = +25°C$ | | 0.016 | | V/V | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | 0.250 | | V/V | |
| $\frac{\Delta V_{BB}}{\Delta V_{EE}}$ | Reference Bias voltage compensation | | | 0.148 | | V/V | |

# Line Receiver

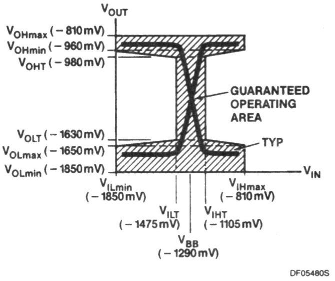
# 10116

## DC ELECTRICAL CHARACTERISTICS (Continued)

| PARAMETER | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] |
|---|---|---|---|---|---|---|---|
| $V_{BB}$ | Reference Bias voltage | $T_A = -30°C$ | −1420 | | −1280 | mV | All inverting or all non-inverting input pins are tied to the $V_{BB}$ pin during measurement. |
| | | $T_A = +25°C$ | −1350 | −1290 | −1230 | mV | |
| | | $T_A = +85°C$ | −1295 | | −1150 | mV | |
| $V_{OH}$ | HIGH level output voltage for Common-Mode Rejection Test | $T_A = -30°C$ | −1060 | | −890 | mV | For $Q_n$ outputs, apply $V_{ILL}$ to inverting inputs and $V_{IHL}$ to non-inverting inputs.<br>For $\overline{Q}_n$ outputs, apply $V_{IHH}$ to inverting inputs and $V_{ILH}$ to non-inverting inputs. |
| | | $T_A = +25°C$ | −960 | | −810 | mV | |
| | | $T_A = +85°C$ | −890 | | −700 | mV | |
| $V_{OL}$ | LOW level output voltage for Common-Mode Rejection Test | $T_A = -30°C$ | −1890 | | −890 | mV | For $Q_n$ outputs, apply $V_{IHL}$ to inverting inputs and $V_{ILL}$ to non-inverting inputs.<br>For $\overline{Q}_n$ outputs, apply $V_{ILH}$ to inverting inputs and $V_{IHH}$ to non-inverting inputs. |
| | | $T_A = +25°C$ | −1850 | | −810 | mV | |
| | | $T_A = +85°C$ | −1825 | | −700 | mV | |
| $-I_{CBO}$ | Input leakage current | $T_A = -30°C$ | | | 1.5 | μA | Apply $V_{EE}$ to each inverting input under test, one at a time, with $V_{ILmin}$ applied to all other inverting inputs and $V_{BB}$ applied to all non-inverting inputs. (Refer to Fig. 8.) |
| | | $T_A = +25°C$ | | | 1.0 | μA | |
| | | $T_A = +85°C$ | | | 1.0 | μA | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst-case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 5.



**NOTES:**

$V_{IHmax}$ – Maximum HIGH level input voltage (the most positive $V_{IH}$).
$V_{IHT}$ – HIGH level input threshold voltage.
$V_{ILT}$ – LOW level input threshold voltage.
$V_{ILmin}$ – Minimum LOW level input voltage (the most negative $V_{IL}$).
$V_{OHmax}$ – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition.
$V_{OHmin}$ – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition.
$V_{OHT}$ – HIGH level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLT}$ – LOW level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLmax}$ – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions.
$V_{OLmin}$ – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions.
$V_{BB}$ – Reference bias voltage (the internally generated reference voltage which is used to set the input and output threshold level).

**Figure 5. Transfer Characteristics**

## AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$

| PARAMETER | | $T_A = -30°C$ | | $T_A = +25°C$ | | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Typ | Max | Min | Max | | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$D_n$ to $Q_n$, $\overline{Q}_n$ | 1.0<br>1.0 | 3.1<br>3.1 | 1.0<br>1.0 | 2.0<br>2.0 | 2.9<br>2.9 | 1.0<br>1.0 | 3.3<br>3.3 | ns<br>ns | Figs. 6, 7, 9 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$\overline{D}_n$ to $Q_n$, $\overline{Q}_n$ | 1.0<br>1.0 | 3.1<br>3.1 | 1.0<br>1.0 | 2.0<br>2.0 | 2.9<br>2.9 | 1.0<br>1.0 | 3.3<br>3.3 | ns<br>ns | Figs. 6, 7, 9 |
| $t_{TLH}$<br>$t_{THL}$ | Transition time<br>20% to 80%, 80% to 20% | 1.1<br>1.1 | 3.6<br>3.6 | 1.1<br>1.1 | 2.0<br>2.0 | 3.3<br>3.3 | 1.1<br>1.1 | 3.7<br>3.7 | ns<br>ns | Figs. 6, 7, 9 |

## AC WAVEFORMS

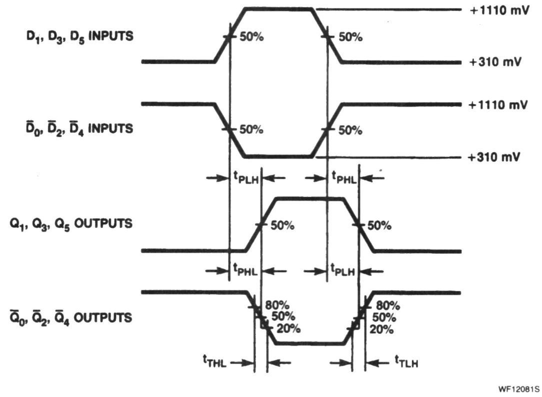
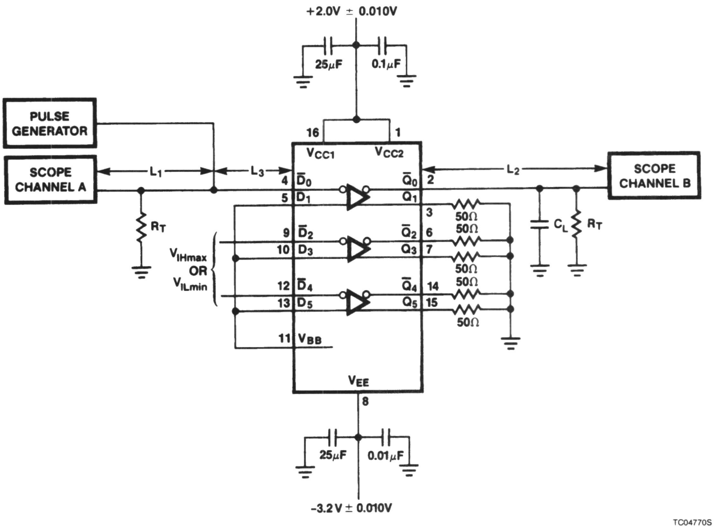

$D_1, D_3, D_5$ INPUTS
$\overline{D}_0, \overline{D}_2, \overline{D}_4$ INPUTS
$Q_1, Q_3, Q_5$ OUTPUTS
$\overline{Q}_0, \overline{Q}_2, \overline{Q}_4$ OUTPUTS
+1110 mV
+310 mV
+1110 mV
+310 mV
50%
$t_{PLH}$
$t_{PHL}$
80%
50%
20%
$t_{THL}$
$t_{TLH}$
WF12081S

Figure 6. Propagation Delay and Transition Times

## TEST CIRCUITS AND WAVEFORMS

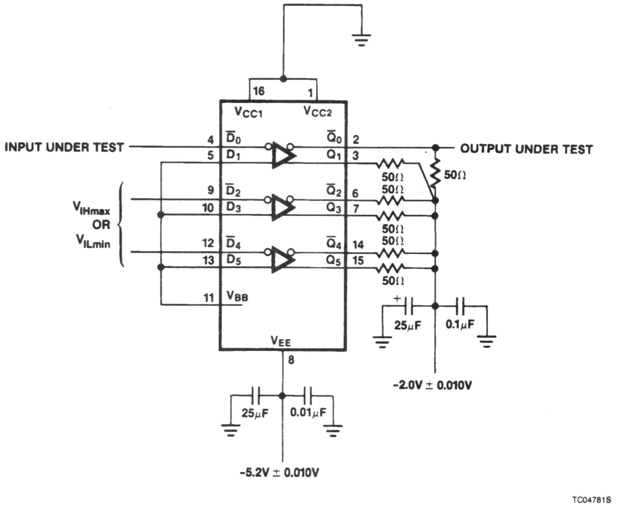

+2.0V ± 0.010V
25μF
0.1μF
PULSE GENERATOR
SCOPE CHANNEL A
SCOPE CHANNEL B
$L_1$
$L_2$
$L_3$
$R_T$
$C_L$
$V_{CC1}$
$V_{CC2}$
$V_{IHmax}$ OR $V_{ILmin}$
$V_{BB}$
$V_{EE}$
50Ω
25μF
0.01μF
-3.2 V ± 0.010V
TC04770S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1μF and 25μF from GND to $V_{CC}$, 0.01μF and 25μF from GND to $V_{EE}$ (0.01 and 0.1uF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lesd length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines.$L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should should not exceed 1/4 inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance $\leqslant$ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.

Figure 7. AC Test Circuit for 10116

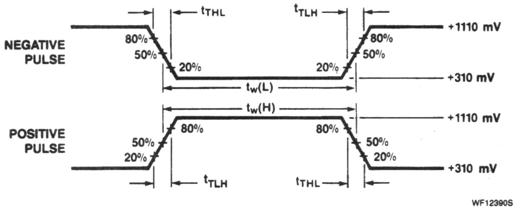
## TEST CIRCUITS AND WAVEFORMS


16
1
$V_{CC1}$
$V_{CC2}$
INPUT UNDER TEST
4 $\overline{D}_0$
5 $D_1$
$\overline{Q}_0$ 2
$Q_1$ 3
OUTPUT UNDER TEST
50Ω
50Ω
$V_{IHmax}$ OR $V_{ILmin}$
9 $\overline{D}_2$
10 $D_3$
$\overline{Q}_2$ 6
$Q_3$ 7
50Ω
50Ω
12 $\overline{D}_4$
13 $D_5$
$\overline{Q}_4$ 14
$Q_5$ 15
50Ω
50Ω
50Ω
11 $V_{BB}$
$V_{EE}$
8
+
25μF
0.1μF
-2.0V ± 0.010V
25μF
0.01μF
-5.2V ± 0.010V
TC04781S

**NOTES:**

1. $V_{CC1} = V_{CC2} = 0V$ (GND), $V_{EE} = -5.2V \pm 0.010V$.
2. Decoupling 0.01μF and 25μF from GND to $V_{EE}$, 0.1μF and 25μF from GND to $V_T$ (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than ¼ inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to $V_T$.
5. All 50Ω resistors should have tolerance of ± 1% or better.

Figure 8. DC Test Circuit for 10116


NEGATIVE PULSE
$t_{THL}$
$t_{TLH}$
80%
50%
20%
20%
80%
50%
+1110 mV
+310 mV
$t_w(L)$
$t_w(H)$
POSITIVE PULSE
80%
80%
50%
20%
50%
20%
+1110 mV
+310 mV
$t_{TLH}$
$t_{THL}$
WF12390S

| INPUT PULSE REQUIREMENTS<br>$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$, $V_T = GND\ (0V)$ | | | | | |
|---|---|---|---|---|---|
| Family | Amplitude | Rep Rate | Pulse Width | $t_{TLH}$ | $t_{THL}$ |
| 10K ECL | 800mVp-p | 1MHz | 500ns | 2.0 ± 0.2ns | 2.0 ± 0.2ns |

Figure 9. Input Pulse Definition

**Signetics**

# 10117
## Gate

**Dual 2-Wide 2-3 Input OR-AND/OR-AND-INVERT Gate**
***Product Specification***

**ECL Products**

### DESCRIPTION

The 10117 is a dual 2-wide 2-input OR-AND/OR-AND-INVERT Gate designed for use in data control as a general purpose logic element. All unused inputs can be left open due to integrated pull-down resistors which avoid the need for a supply voltage.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 10117 | 2.3ns | 20mA |

### ORDERING CODE

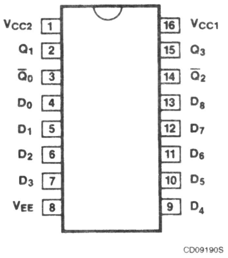
| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} = \text{GND}$, $V_{EE} = -5.2V$<br>$T_A = -30°C$ to $+85°C$ |
|---|---|
| Plastic DIP | 10117N |
| Ceramic DIP | 10117F |

### PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_0 - D_8$ | Data Inputs |
| $\overline{Q}_0$, $\overline{Q}_2$, $Q_1$, $Q_3$ | Data Outputs |

6

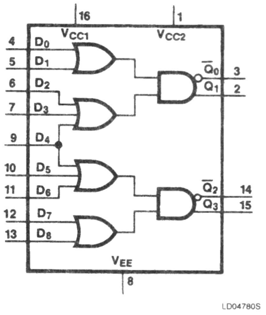
### PIN CONFIGURATION



VCC2 1
Q1 2
Q̄0 3
D0 4
D1 5
D2 6
D3 7
VEE 8
16 VCC1
15 Q3
14 Q̄2
13 D8
12 D7
11 D6
10 D5
9 D4
CD09190S

Figure 1

### LOGIC SYMBOL



16
VCC1
1
VCC2
4 D0
5 D1
6 D2
7 D3
9 D4
10 D5
11 D6
12 D7
13 D8
Q̄0 3
Q1 2
Q̄2 14
Q3 15
VEE
8
LD04780S

Figure 2

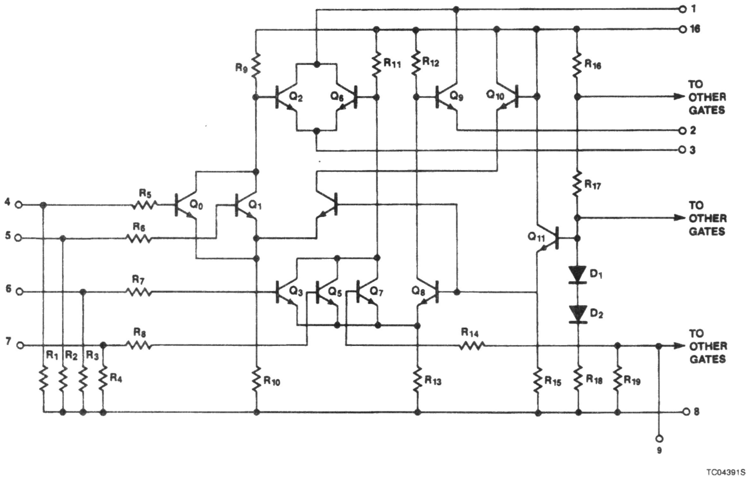
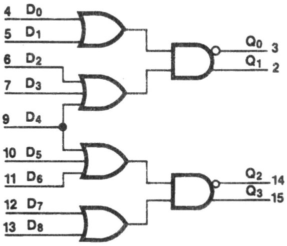

1
16
2
3
4
5
6
7
8
9
TO OTHER GATES
TO OTHER GATES
TO OTHER GATES
$R_1$ $R_2$ $R_3$ $R_4$ $R_5$ $R_6$ $R_7$ $R_8$ $R_9$ $R_{10}$ $R_{11}$ $R_{12}$ $R_{13}$ $R_{14}$ $R_{15}$ $R_{16}$ $R_{17}$ $R_{18}$ $R_{19}$
$Q_0$ $Q_1$ $Q_2$ $Q_3$ $Q_5$ $Q_6$ $Q_7$ $Q_8$ $Q_9$ $Q_{10}$ $Q_{11}$
$D_1$ $D_2$
TC04391S

Figure 3. Circuit Diagram


4 $D_0$
5 $D_1$
6 $D_2$
7 $D_3$
9 $D_4$
10 $D_5$
11 $D_6$
12 $D_7$
13 $D_8$
$Q_0$ 3
$Q_1$ 2
$Q_2$ 14
$Q_3$ 15

$Q_0 = \overline{(D_0 + D_1) \cdot (D_2 + D_3 + D_4)}$
$Q_1 = (D_0 + D_1) \cdot (D_2 + D_3 + D_4)$
$Q_2 = \overline{(D_7 + D_8) \cdot (D_4 + D_5 + D_6)}$
$Q_3 = (D_7 + D_8) \cdot (D_4 + D_5 + D_6)$

**Positive logic: HIGH state = 1**
**LOW state = 0**

LD04791S

Figure 4. Logic Diagram

## Gate

## 10117

**ABSOLUTE MAXIMUM RATINGS** (Operation beyond the limits set forth in this table may impair useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | | 10K ECL | UNIT |
|---|---|---|---|---|
| $V_{EE}$ | Supply voltage | | −8.0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | | 0 to $V_{EE}$ | V |
| $I_O$ | Output current | | −50 | mA |
| $T_S$ | Storage temperature | | −55 to +150 | °C |
| $T_J$ | Maximum junction temperature | Ceramic package | +165 | °C |
| | | Plastic package | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | 10K ECL | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | −5.2 | | V |
| $V_{IH}$ | HIGH level input voltage | $T_A = -30°C$ | | | −890 | mV |
| | | $T_A = +25°C$ | | | −810 | mV |
| | | $T_A = +85°C$ | | | −700 | mV |
| $V_{IHT}$ | HIGH level input threshold voltage | $T_A = -30°C$ | −1205 | | | mV |
| | | $T_A = +25°C$ | −1105 | | | mV |
| | | $T_A = +85°C$ | −1035 | | | mV |
| $V_{ILT}$ | LOW level input threshold voltage | $T_A = -30°C$ | | | −1500 | mV |
| | | $T_A = +25°C$ | | | −1475 | mV |
| | | $T_A = +85°C$ | | | −1440 | mV |
| $V_{IL}$ | LOW level input voltage | $T_A = -30°C$ | −1890 | | | mV |
| | | $T_A = +25°C$ | −1850 | | | mV |
| | | $T_A = +85°C$ | −1825 | | | mV |
| $T_A$ | Operating ambient temperature | | −30 | +25 | +85 | °C |

**NOTE:**
When operating at $V_{EE}$ other than specified voltage (−5.2V), the DC and AC Characteristics will vary slightly from specified values.
(See table of DC Characteristics)

6

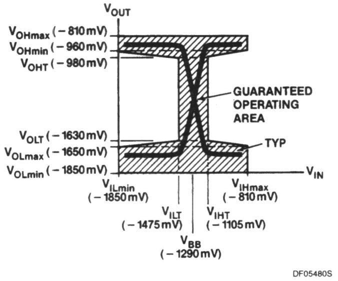
| PARAMETER | | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | | $T_A = -30°C$ | −1060 | | −890 | mV | For $Q_1$ & $Q_3$ outputs, apply $V_{IHmax}$ to all inputs.<br>For $\overline{Q}_0$ & $\overline{Q}_2$ outputs, apply $V_{ILmin}$ to all inputs. |
| | | | $T_A = +25°C$ | −960 | | −810 | mV | |
| | | | $T_A = +85°C$ | −890 | | −700 | mV | |
| $V_{OHT}$ | HIGH level output threshold voltage | | $T_A = -30°C$ | −1080 | | | mV | For $Q_1$ input, apply $V_{IHT}$ to $D_0$ input with $V_{ILmin}$ applied to $D_1$ input and $V_{IHmax}$ applied to all other inputs.<br>For $\overline{Q}_0$ output, apply $V_{ILT}$ to $D_0$ input with $V_{ILmin}$ applied to $D_1$ input and $V_{IHmax}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | −980 | | | mV | |
| | | | $T_A = +85°C$ | −910 | | | mV | |
| $V_{OLT}$ | LOW level output threshold voltage | | $T_A = -30°C$ | | | −1655 | mV | For $Q_1$ input, apply $V_{ILT}$ to $D_0$ input with $V_{ILmin}$ applied to $D_1$ input and $V_{IHmax}$ applied to all other inputs.<br>For $\overline{Q}_0$ output, apply $V_{IHT}$ to $D_0$ input with $V_{ILmin}$ applied to $D_1$ input and $V_{IHmax}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | | | −1630 | mV | |
| | | | $T_A = +85°C$ | | | −1595 | mV | |
| $V_{OL}$ | LOW level output voltage | | $T_A = -30°C$ | −1890 | | −1675 | mV | For $Q_1$ & $Q_3$ outputs, apply $V_{ILmin}$ to all inputs.<br>For $\overline{Q}_0$ & $\overline{Q}_2$ outputs, apply $V_{IHmax}$ to all inputs. |
| | | | $T_A = +25°C$ | −1850 | | −1650 | mV | |
| | | | $T_A = +85°C$ | −1825 | | −1615 | mV | |
| $I_{IH}$ | HIGH level input current | $D_4$ input | $T_A = -30°C$ | | | 560 | μA | Apply $V_{IHmax}$ to each input under test, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | | | 350 | μA | |
| | | | $T_A = +85°C$ | | | 350 | μA | |
| | | All other inputs | $T_A = -30°C$ | | | 390 | μA | |
| | | | $T_A = +25°C$ | | | 245 | μA | |
| | | | $T_A = +85°C$ | | | 245 | μA | |
| $I_{IL}$ | LOW level input current | | $T_A = -30°C$ | 0.5 | | | μA | Apply $V_{ILmin}$ to each input under test, one at a time, with $V_{IHmax}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | 0.5 | | | μA | |
| | | | $T_A = +85°C$ | 0.3 | | | μA | |
| $-I_{EE}$ | $V_{EE}$ supply current | | $T_A = -30°C$ | | | 29 | mA | |
| | | | $T_A = +25°C$ | | 20 | 26 | mA | |
| | | | $T_A = +85°C$ | | | 29 | mA | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | | $T_A = +25°C$ | | 0.016 | | V/V | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | | 0.250 | | V/V | |
| $\frac{\Delta V_{BB}}{\Delta V_{EE}}$ | Reference bias voltage compensation | | | | 0.148 | | V/V | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst-case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 5.

# Gate

# 10117



**NOTES:**

$V_{IHmax}$ – Maximum HIGH level input voltage (the most positive $V_{IH}$).
$V_{IHT}$ – HIGH level input threshold voltage.
$V_{ILT}$ – LOW level input threshold voltage.
$V_{ILmin}$ – Minimum LOW level input voltage (the most negative $V_{IL}$).
$V_{OHmax}$ – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition.
$V_{OHmin}$ – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition.
$V_{OHT}$ – HIGH level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLT}$ – LOW level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLmax}$ – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions.
$V_{OLmin}$ – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions.
$V_{BB}$ – Reference Bias voltage. The internally generated reference voltage which is used to set the input and output threshold level.

**Figure 5. Transfer Characteristics**

## AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$

| PARAMETER | $T_A = -30°C$ | | $T_A = +25°C$ | | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Typ | Max | Min | Max | | |
| $t_{PLH}$ Propagation delay | 1.4 | 3.9 | 1.4 | 2.3 | 3.4 | 1.4 | 3.8 | ns | Figs. 6, 7, 8 |
| $t_{PHL}$ $D_n$ to $Q_n$ | 1.4 | 3.9 | 1.4 | 2.3 | 3.4 | 1.4 | 3.8 | ns | |
| $t_{PLH}$ Propagation delay | 1.4 | 3.9 | 1.4 | 2.3 | 3.4 | 1.4 | 3.8 | ns | Figs. 6, 7, 8 |
| $t_{PHL}$ $D_n$ to $\overline{Q}_n$ | 1.4 | 3.9 | 1.4 | 2.3 | 3.4 | 1.4 | 3.8 | ns | |
| $t_{TLH}$ Transition time | 0.9 | 4.1 | 1.1 | 2.2 | 4.0 | 1.1 | 4.6 | ns | Figs. 6, 7, 8 |
| $t_{THL}$ 20% to 80%, 80% to 20% | 0.9 | 4.1 | 1.1 | 2.2 | 4.0 | 1.1 | 4.6 | ns | |

## AC WAVEFORMS

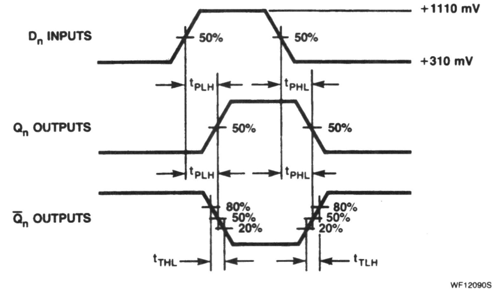
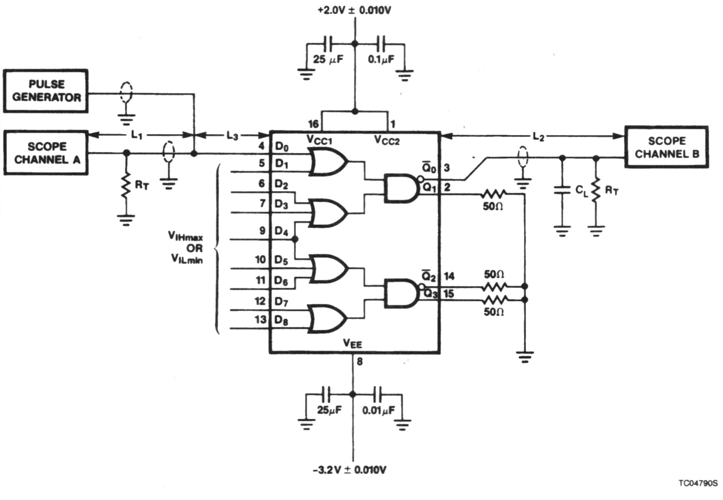


**Figure 6. Propagation Delay and Transition Times**

## TEST CIRCUITS AND WAVEFORMS

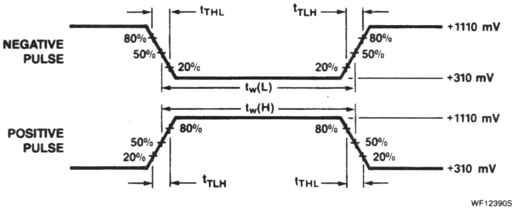


+2.0V ± 0.010V
25 μF
0.1μF
PULSE GENERATOR
SCOPE CHANNEL A
L1
L3
L2
RT
16
1
VCC1
VCC2
4 D0
5 D1
6 D2
7 D3
9 D4
10 D5
11 D6
12 D7
13 D8
VIHmax OR VILmin
Q̄0 3
Q1 2
Q̄2 14
Q3 15
50Ω
50Ω
50Ω
CL
RT
SCOPE CHANNEL B
VEE
8
25μF
0.01μF
-3.2V ± 0.010V
TC04790S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1μF and 25μF from GND to $V_{CC}$, 0.01μF and 25μF from GND to $V_{EE}$ (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than ¼ inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed ¼ inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than ¼ inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance < 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed ¼ inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.

Figure 7. AC Test Circuit for 10117



NEGATIVE PULSE
tTHL
tTLH
80%
50%
20%
20%
80%
50%
+1110 mV
+310 mV
tw(L)
tw(H)
POSITIVE PULSE
80%
80%
50%
20%
50%
20%
+1110 mV
+310 mV
tTLH
tTHL
WF12390S

| INPUT PULSE REQUIREMENTS<br>$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$, $V_T$ = GND (0V) | | | | | |
|---|---|---|---|---|---|
| **Family** | **Amplitude** | **Rep Rate** | **Pulse Width** | **$t_{TLH}$** | **$t_{THL}$** |
| 10K ECL | 800mVp-p | 1MHz | 500ns | 2.0 ±0.2ns | 2.0 ±0.2ns |

Figure 8. Input Pulse Definition

**Signetics**

# 10118
## Gate

**Dual 2-Wide 3-Input OR-AND Gate**
***Product Specification***

**ECL Products**

## DESCRIPTION

The 10118 is a dual 2-Wide 3-Input OR-AND Gate designed for use in data control as a general purpose logic element. All unused inputs can be left open due to integrated pull-down resistors, which avoid the need for a supply voltage.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 10118 | 2.3ns | 20mA |

## ORDERING CODE

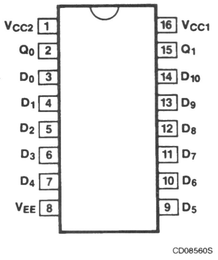
| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V$<br>$T_A = -30°C$ to $+85°C$ |
|---|---|
| Plastic DIP | 10118N |
| Ceramic DIP | 10118F |

## PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_0 - D_{10}$ | Data Inputs |
| $Q_0$, $Q_1$ | Data Outputs |

6

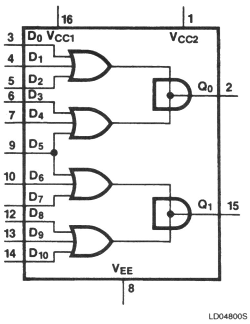
## PIN CONFIGURATION



VCC2 1
Q0 2
D0 3
D1 4
D2 5
D3 6
D4 7
VEE 8
16 VCC1
15 Q1
14 D10
13 D9
12 D8
11 D7
10 D6
9 D5
CD08560S

**Figure 1**

## LOGIC SYMBOL



16
1
3 D0 VCC1
VCC2
4 D1
5 D2
6 D3
7 D4
9 D5
10 D6
D7
12 D8
13 D9
14 D10
Q0 2
Q1 15
VEE
8
LD04800S

**Figure 2**

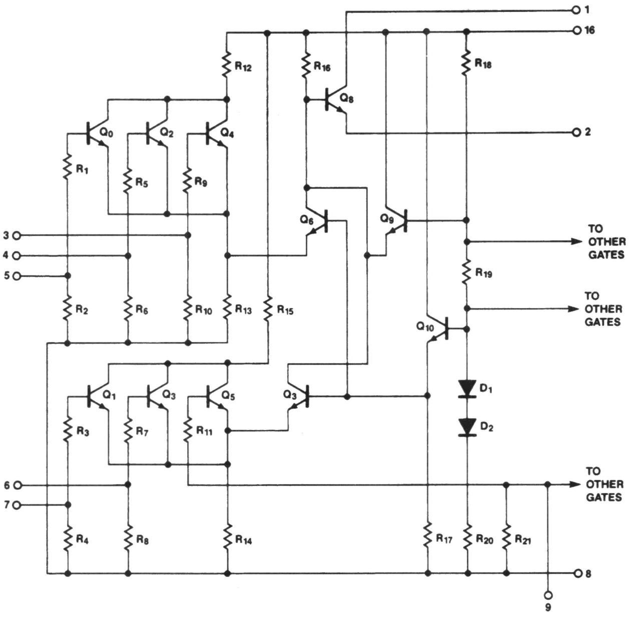
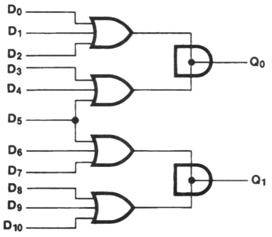

1
16
2
3
4
5
6
7
8
9
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
R17
R18
R19
R20
R21
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q3
Q8
Q9
Q10
D1
D2
TO OTHER GATES
TO OTHER GATES
TO OTHER GATES
TC04400S

Figure 3. Circuit Diagram (One Gate)


D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
Q0
Q1

$Q_1 = (D_0 + D_1 + D_2) \cdot (D_3 + D_4 + D_5)$
$Q_1 = (D_5 + D_6 + D_7) \cdot (D_8 + D_{10} + D_{11})$

Positive logic: HIGH state = 1
LOW state = 0

LD05550S

Figure 4. Logic Diagram

## Gate

## 10118

**ABSOLUTE MAXIMUM RATINGS** (Operation beyond the limits set forth in this table may impair useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | | 10K ECL | UNIT |
|---|---|---|---|---|
| $V_{EE}$ | Supply voltage | | -8.0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | | 0 to $V_{EE}$ | V |
| $I_O$ | Output current | | -50 | mA |
| $T_S$ | Storage temperature | | -55 to +150 | °C |
| $T_J$ | Maximum junction temperature | Ceramic package | +165 | °C |
| | | Plastic package | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | 10K ECL | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | -5.2 | | V |
| $V_{IH}$ | HIGH level input voltage | $T_A$ = -30°C | | | -890 | mV |
| | | $T_A$ = +25°C | | | -810 | mV |
| | | $T_A$ = +85°C | | | -700 | mV |
| $V_{IHT}$ | HIGH level input threshold voltage | $T_A$ = -30°C | -1205 | | | mV |
| | | $T_A$ = +25°C | -1105 | | | mV |
| | | $T_A$ = +85°C | -1035 | | | mV |
| $V_{ILT}$ | LOW level input threshold voltage | $T_A$ = -30°C | | | -1500 | mV |
| | | $T_A$ = +25°C | | | -1475 | mV |
| | | $T_A$ = +85°C | | | -1440 | mV |
| $V_{IL}$ | LOW level input voltage | $T_A$ = -30°C | -1890 | | | mV |
| | | $T_A$ = +25°C | -1850 | | | mV |
| | | $T_A$ = +85°C | -1825 | | | mV |
| $T_A$ | Operating ambient temperature | | -30 | +25 | +85 | °C |

**NOTE:**
When operating at $V_{EE}$ other than specified voltage (-5.2V), the DC and AC Characteristics will vary slightly from specified values. (See table of DC Characteristics)

## Gate

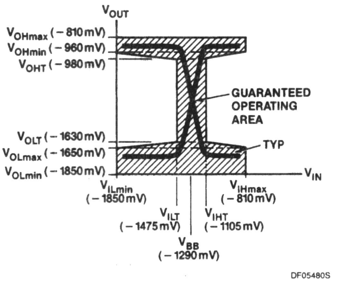
## 10118

**DC ELECTRICAL CHARACTERISTICS** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$, output loading with 50Ω to -2.0V ±0.010V unless otherwise specified$^{1,3}$

| PARAMETER | | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS$^2$ |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | | $T_A = -30°C$ | -1060 | | -890 | mV | Apply $V_{IHmax}$ to all inputs. |
| | | | $T_A = +25°C$ | -960 | | -810 | mV | |
| | | | $T_A = +85°C$ | -890 | | -700 | mV | |
| $V_{OHT}$ | HIGH level output threshold voltage | | $T_A = -30°C$ | -1080 | | | mV | For $Q_0$ output, apply $V_{IHT}$ to $D_0$ input with $V_{ILmin}$ applied to $D_1$ and $D_2$ inputs and $V_{IHmax}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | -980 | | | mV | |
| | | | $T_A = +85°C$ | -910 | | | mV | |
| $V_{OLT}$ | LOW level output threshold voltage | | $T_A = -30°C$ | | | -1655 | mV | For $Q_0$ output, apply $V_{ILT}$ to $D_0$ input with $V_{ILmin}$ applied to $D_1$ and $D_2$ inputs and $V_{IHmax}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | | | -1630 | mV | |
| | | | $T_A = +85°C$ | | | -1595 | mV | |
| $V_{OL}$ | LOW level output voltage | | $T_A = -30°C$ | -2000 | | -1675 | mV | Apply $V_{ILmin}$ to all inputs. |
| | | | $T_A = +25°C$ | -1990 | | -1650 | mV | |
| | | | $T_A = +85°C$ | -1920 | | -1615 | mV | |
| $I_{IH}$ | HIGH level input current | $D_5$ input | $T_A = -30°C$ | | | 560 | μA | Apply $V_{IHmax}$ to each input under test, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | | | 350 | μA | |
| | | | $T_A = +85°C$ | | | 350 | μA | |
| | | All other inputs | $T_A = -30°C$ | | | 390 | μA | Apply $V_{IHmax}$ to each input under test, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | | | 245 | μA | |
| | | | $T_A = +85°C$ | | | 245 | μA | |
| $I_{IL}$ | LOW level input current | | $T_A = -30°C$ | 0.5 | | | μA | Apply $V_{ILmin}$ to each input under test, one at a time, with $V_{IHmax}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | 0.5 | | | μA | |
| | | | $T_A = +85°C$ | 0.3 | | | μA | |
| $-I_{EE}$ | $V_{EE}$ supply current | | $T_A = -30°C$ | | | 29 | mA | |
| | | | $T_A = +25°C$ | | 20 | 26 | mA | |
| | | | $T_A = +85°C$ | | | 29 | mA | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | | $T_A = +25°C$ | | 0.016 | | V/V | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | | 0.250 | | V/V | |
| $\frac{\Delta V_{BB}}{\Delta V_{EE}}$ | Reference bias voltage compensation | | | | 0.148 | | V/V | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst-case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 5.



**NOTES:**

$V_{IHmax}$ – Maximum HIGH level input voltage (the most positive $V_{IH}$).
$V_{IHT}$ – HIGH level input threshold voltage.
$V_{ILT}$ – LOW level input threshold voltage.
$V_{ILmin}$ – Minimum LOW level input voltage (the most negative $V_{IL}$).
$V_{OHmax}$ – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition.
$V_{OHmin}$ – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition.
$V_{OHT}$ – HIGH level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLT}$ – LOW level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLmax}$ – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions.
$V_{OLmin}$ – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions.
$V_{BB}$ – Reference Bias voltage. The internally generated reference voltage which is used to set the input and output threshold level.

**Figure 5. Transfer Characteristics**

## AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$

| PARAMETER | $T_A = -30°C$ | | $T_A = +25°C$ | | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Typ | Max | Min | Max | | |
| $t_{PLH}$ Propagation delay<br>$D_n$ to $Q_n$ | 1.4<br>1.4 | 3.9<br>3.9 | 1.4<br>1.4 | 2.3<br>2.3 | 3.4<br>3.4 | 1.4<br>1.4 | 3.8<br>3.8 | ns<br>ns | Figs. 6, 7, 8 |
| $t_{TLH}$ Transition time<br>$t_{THL}$ 20% to 80%, 80% to 20% | 0.8<br>0.8 | 4.1<br>4.1 | 1.5<br>1.5 | 2.5<br>2.5 | 4.0<br>4.0 | 1.5<br>1.5 | 4.6<br>4.6 | ns<br>ns | Figs. 6, 7, 8 |

## AC WAVEFORMS

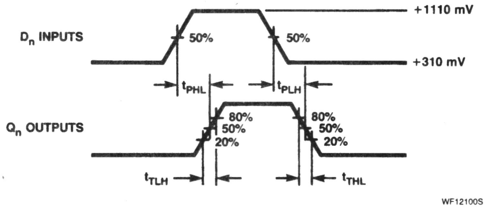
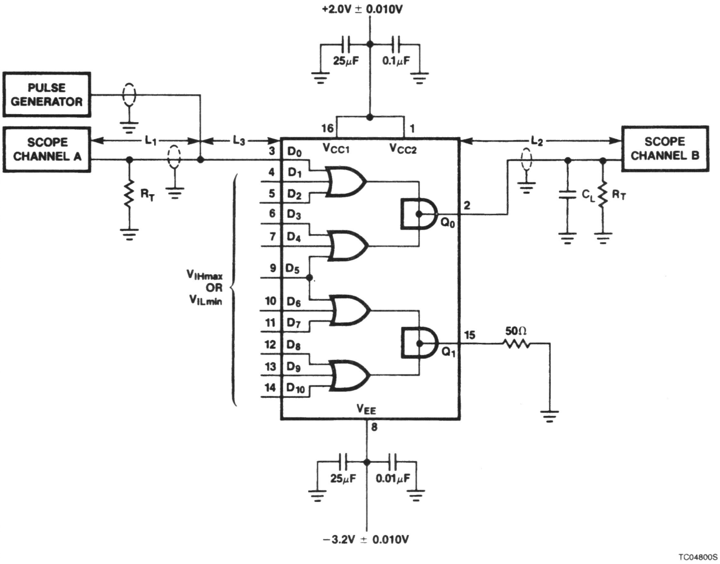


**Figure 6. Propagation Delay and Transition Times**

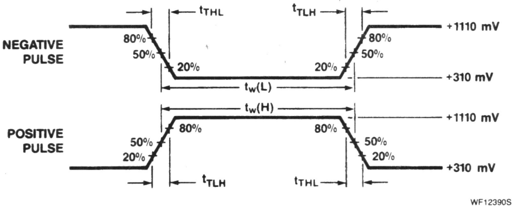
## TEST CIRCUITS AND WAVEFORMS


+2.0V ± 0.010V
25μF
0.1μF
PULSE GENERATOR
SCOPE CHANNEL A
L1
L3
R_T
16
1
3
D0
VCC1
VCC2
4 D1
5 D2
6 D3
7 D4
9 D5
10 D6
11 D7
12 D8
13 D9
14 D10
V_IHmax OR V_ILmin
2
Q0
15
Q1
50Ω
L2
SCOPE CHANNEL B
C_L
R_T
VEE
8
25μF
0.01μF
−3.2V ± 0.010V
TC04800S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1μF and 25μF from GND to $V_{CC}$, 0.01μF and 25μF from GND to $V_{EE}$ (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than ¼ inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed ¼ inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than ¼ inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance < 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed ¼ inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.

Figure 7. AC Test Circuit for 10118


NEGATIVE PULSE
POSITIVE PULSE
t_THL
t_TLH
80%
50%
20%
+1110 mV
+310 mV
t_w(L)
t_w(H)
WF12390S

| INPUT PULSE REQUIREMENTS<br>$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$, $V_T$ = GND (0V) | | | | | |
|---|---|---|---|---|---|
| Family | Amplitude | Rep Rate | Pulse Width | $t_{TLH}$ | $t_{THL}$ |
| 10K ECL | 800mVp-p | 1MHz | 500ns | 2.0 ±0.2ns | 2.0 ±0.2ns |

Figure 8. Input Pulse Definition

**Signetics**

# 10119
## Gate

**4-Wide 4-3-3-3-Input OR-AND Gate**
***Product Specification***

**ECL Products**

### DESCRIPTION

The 10119 is a 4-wide 4-3-3-3-Input OR-AND Gate designed for use in data control as a general purpose logic element. All unused inputs can be left open due to integrated pull-down resistors, which avoid the need for a supply voltage.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT $(-I_{EE})$ |
|---|---|---|
| 10119 | 2.3ns | 20mA |

### ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} = \text{GND}$, $V_{EE} = -5.2\text{V}$<br>$T_A = -30°\text{C}$ to $+85°\text{C}$ |
|---|---|
| Plastic DIP | 10119N |
| Ceramic DIP | 10119F |

### PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_0 - D_{11}$ | Data Inputs |
| Q | Data Output |

### PIN CONFIGURATION

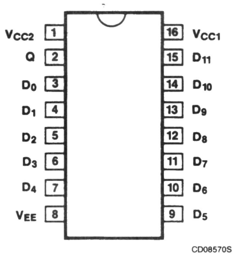

$V_{CC2}$ 1
Q 2
$D_0$ 3
$D_1$ 4
$D_2$ 5
$D_3$ 6
$D_4$ 7
$V_{EE}$ 8
16 $V_{CC1}$
15 $D_{11}$
14 $D_{10}$
13 $D_9$
12 $D_8$
11 $D_7$
10 $D_6$
9 $D_5$
CD08570S

**Figure 1**

### LOGIC SYMBOL

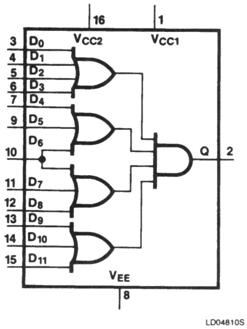

16
1
$V_{CC2}$
$V_{CC1}$
3 $D_0$
4 $D_1$
5 $D_2$
6 $D_3$
7 $D_4$
9 $D_5$
$D_6$
10
11 $D_7$
12 $D_8$
13 $D_9$
14 $D_{10}$
15 $D_{11}$
Q 2
$V_{EE}$
8
LD04810S

**Figure 2**

# Gate

# 10119

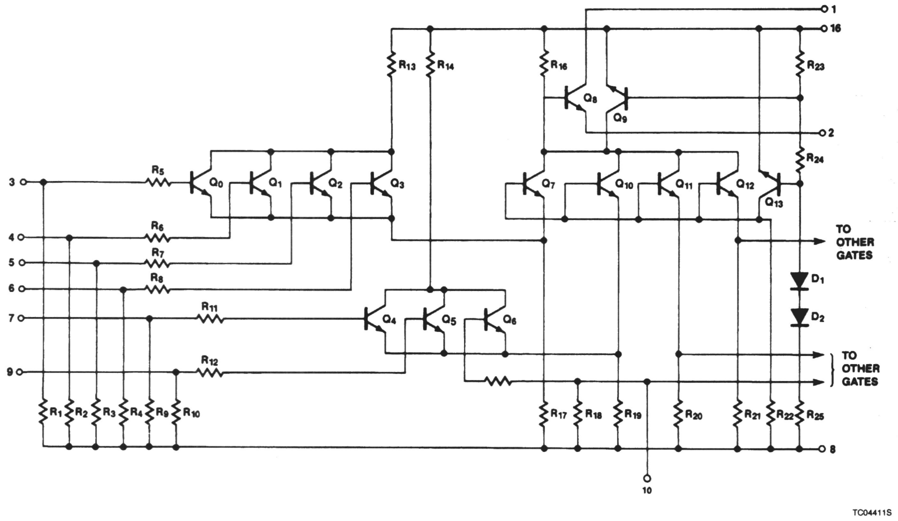
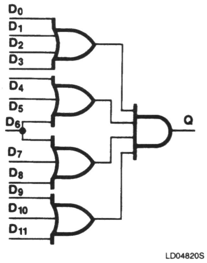

1
16
2
3
4
5
6
7
9
8
10
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R16
R17
R18
R19
R20
R21
R22
R23
R24
R25
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
D1
D2
TO OTHER GATES
TO OTHER GATES
TC04411S

**Figure 3. Circuit Diagram**


D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
Q
LD04820S

$$Q = (D_0 + D_1 + D_2 + D_3) \cdot (D_4 + D_5 + D_6) \cdot (D_6 + D_7 D_8) \cdot (D_9 + D_{10} + D_{11})$$

Positive logic: HIGH state = 1
LOW state = 0

**Figure 4. Logic Diagram**

# Gate

# 10119

## ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | | 10K ECL | UNIT |
|---|---|---|---|---|
| $V_{EE}$ | Supply voltage | | −8.0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | | 0 to $V_{EE}$ | V |
| $I_O$ | Output current | | −50 | mA |
| $T_S$ | Storage temperature | | −55 to +150 | °C |
| $T_J$ | Maximum junction temperature | Ceramic package | +165 | °C |
| | | Plastic package | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | 10K ECL | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | −5.2 | | V |
| $V_{IH}$ | HIGH level input voltage | $T_A$ = −30°C | | | −890 | mV |
| | | $T_A$ = +25°C | | | −810 | mV |
| | | $T_A$ = +85°C | | | −700 | mV |
| $V_{IHT}$ | HIGH level input threshold voltage | $T_A$ = −30°C | −1205 | | | mV |
| | | $T_A$ = +25°C | −1105 | | | mV |
| | | $T_A$ = +85°C | −1035 | | | mV |
| $V_{ILT}$ | LOW level input threshold voltage | $T_A$ = −30°C | | | −1500 | mV |
| | | $T_A$ = +25°C | | | −1475 | mV |
| | | $T_A$ = +85°C | | | −1440 | mV |
| $V_{IL}$ | LOW level input voltage | $T_A$ = −30°C | −1890 | | | mV |
| | | $T_A$ = +25°C | −1850 | | | mV |
| | | $T_A$ = +85°C | −1825 | | | mV |
| $T_A$ | Operating ambient temperature | | −30 | +25 | +85 | °C |

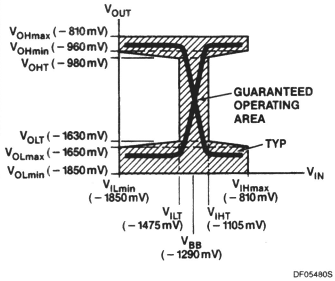
**NOTE:**
When operating at $V_{EE}$ other than specified voltage (−5.2V), the DC and AC Characteristics will vary slightly from specified values.
(See table of DC Characteristics)

**DC ELECTRICAL CHARACTERISTICS** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$, output loading with 50Ω to $-2.0V \pm 0.010V$ unless otherwise specified[1,3]

| PARAMETER | | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | | $T_A = -30°C$ | -1060 | | -890 | mV | Apply $V_{IHmax}$ to all inputs. |
| | | | $T_A = +25°C$ | -960 | | -810 | mV | |
| | | | $T_A = +85°C$ | -890 | | -700 | mV | |
| $V_{OHT}$ | HIGH level output threshold voltage | | $T_A = -30°C$ | -1080 | | | mV | Apply $V_{IHT}$ to $D_0$ input with $V_{ILmin}$ applied to $D_1$, $D_2$, and $D_3$ inputs and $V_{IHmax}$ to all other inputs. |
| | | | $T_A = +25°C$ | -980 | | | mV | |
| | | | $T_A = +85°C$ | -910 | | | mV | |
| $V_{OLT}$ | LOW level output threshold voltage | | $T_A = -30°C$ | | | -1655 | mV | Apply $V_{ILT}$ to $D_0$ input with $V_{ILmin}$ applied to $D_1$, $D_2$, and $D_3$ inputs and $V_{IHmax}$ to all other inputs. |
| | | | $T_A = +25°C$ | | | -1630 | mV | |
| | | | $T_A = +85°C$ | | | -1595 | mV | |
| $V_{OL}$ | LOW level output voltage | | $T_A = -30°C$ | -2000 | | -1675 | mV | Apply $V_{ILmin}$ to all inputs. |
| | | | $T_A = +25°C$ | -1990 | | -1650 | mV | |
| | | | $T_A = +85°C$ | -1920 | | -1615 | mV | |
| $I_{IH}$ | HIGH level input current | $D_6$ input | $T_A = -30°C$ | | | 560 | mV | Apply $V_{ILmax}$ to each input under test, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | | | 350 | mV | |
| | | | $T_A = +85°C$ | | | 350 | mV | |
| | | Other inputs | $T_A = -30°C$ | | | 390 | mV | |
| | | | $T_A = +25°C$ | | | 245 | mV | |
| | | | $T_A = +85°C$ | | | 245 | mV | |
| $I_{IL}$ | LOW level input current | | $T_A = -30°C$ | 0.5 | | | μA | Apply $V_{ILmin}$ to each input under test, one at a time, with $V_{IHmax}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | 0.5 | | | μA | |
| | | | $T_A = +85°C$ | 0.3 | | | μA | |
| $-I_{EE}$ | $V_{EE}$ supply current | | $T_A = -30°C$ | | | 29 | mA | |
| | | | $T_A = +25°C$ | | 20 | 26 | mA | |
| | | | $T_A = +85°C$ | | | 29 | mA | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | | $T_A = +25°C$ | | 0.016 | | V/V | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | | 0.250 | | V/V | |
| $\frac{\Delta V_{BB}}{\Delta V_{EE}}$ | Reference bias voltage compensation | | | | 0.148 | | V/V | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst-case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 5.



**NOTES:**

| | |
|---|---|
| $V_{IHmax}$ | – Maximum HIGH level input voltage (the most positive $V_{IH}$). |
| $V_{IHT}$ | – HIGH level input threshold voltage. |
| $V_{ILT}$ | – LOW level input threshold voltage. |
| $V_{ILmin}$ | – Minimum LOW level input voltage (the most negative $V_{IL}$). |
| $V_{OHmax}$ | – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition. |
| $V_{OHmin}$ | – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition. |
| $V_{OHT}$ | – HIGH level output threshold voltage with the inputs set to their respective threshold levels. |
| $V_{OLT}$ | – LOW level output threshold voltage with the inputs set to their respective threshold levels. |
| $V_{OLmax}$ | – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions. |
| $V_{OLmin}$ | – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions. |
| $V_{BB}$ | – Reference Bias voltage. The internally generated reference voltage which is used to set the input and output threshold level. |

Figure 5. Transfer Characteristics

## AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$

| PARAMETER | $T_A = -30°C$ | | $T_A = +25°C$ | | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Typ | Max | Min | Max | | |
| $t_{PLH}$ Propagation delay | 1.4 | 3.9 | 1.4 | 2.3 | 3.4 | 1.4 | 3.8 | ns | Figs. 6, 7, 8 |
| $t_{PHL}$ $D_n$ to Q | 1.4 | 3.9 | 1.4 | 2.3 | 3.4 | 1.4 | 3.8 | ns | |
| $t_{TLH}$ Transition time | 0.8 | 4.1 | 1.5 | 2.5 | 4.0 | 1.5 | 4.6 | ns | Figs. 6, 7, 8 |
| $t_{THL}$ 20% to 80%, 80% to 20% | 0.8 | 4.1 | 1.5 | 2.5 | 4.0 | 1.5 | 4.6 | ns | |

## AC WAVEFORMS

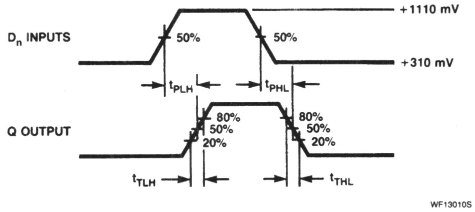
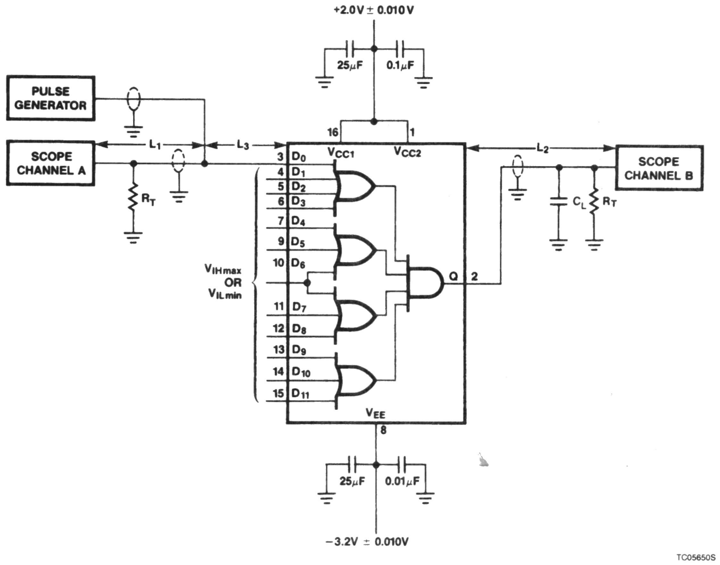


Figure 6. Propagation Delay and Transition Times

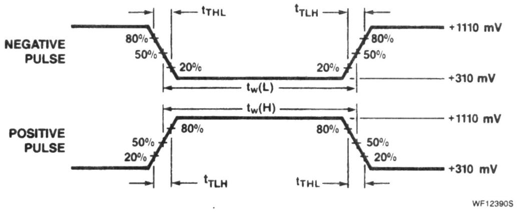
## TEST CIRCUITS AND WAVEFORMS


+2.0V ± 0.010V
25µF
0.1µF
PULSE GENERATOR
SCOPE CHANNEL A
L1
L3
$R_T$
16
1
$V_{CC1}$
$V_{CC2}$
3 $D_0$
4 $D_1$
5 $D_2$
6 $D_3$
7 $D_4$
9 $D_5$
10 $D_6$
$V_{IHmax}$ OR $V_{ILmin}$
11 $D_7$
12 $D_8$
13 $D_9$
14 $D_{10}$
15 $D_{11}$
Q
2
$V_{EE}$
8
25µF
0.01µF
−3.2V ± 0.010V
L2
SCOPE CHANNEL B
$C_L$
$R_T$
TC05650S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1µF and 25µF from GND to $V_{CC}$, 0.01µF and 25µF from GND to $V_{EE}$ (0.01 and 0.1µF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than ¼ inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed ¼ inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than ¼ inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance < 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed ¼ inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.

Figure 7. AC Test Circuit for 10119


$t_{THL}$
$t_{TLH}$
NEGATIVE PULSE
80%
50%
20%
20%
80%
50%
+1110 mV
+310 mV
$t_w(L)$
$t_w(H)$
POSITIVE PULSE
80%
80%
50%
20%
50%
20%
+1110 mV
+310 mV
$t_{TLH}$
$t_{THL}$
WF12390S

**INPUT PULSE REQUIREMENTS**
**$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$, $V_T$ = GND (0V)**

| Family | Amplitude | Rep Rate | Pulse Width | $t_{TLH}$ | $t_{THL}$ |
|---|---|---|---|---|---|
| 10K ECL | 800mVp-p | 1MHz | 500ns | 2.0 ± 0.2ns | 2.0 ± 0.2ns |

Figure 8. Input Pulse Definition

**Signetics**

# 10121
## Gate

**4-Wide OR-AND/OR-AND-INVERT Gate**
***Product Specification***

**ECL Products**

## DESCRIPTION

The 10121 is a 4-Wide OR-AND/OR-AND-INVERT Gate designed for use in data control as a general purpose logic element. All unused inputs can be left open due to integrated pull-down resistors, which avoid the need for a supply voltage.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 10121 | 2.3ns | 20mA |

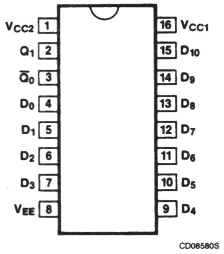
## ORDERING CODE

| PACKAGES | COMMERCIAL RANGES $V_{CC1} = V_{CC2} = \text{GND}$, $V_{EE} = -5.2V$ $T_A = -30°C$ to $+85°C$ |
|---|---|
| Plastic DIP | 10121N |
| Ceramic DIP | 10121F |

## PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_0 - D_{10}$ | Data Inputs |
| $\overline{Q}_0$, $Q_1$ | Data Outputs |

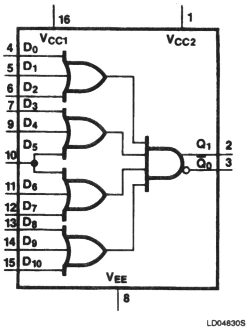
## PIN CONFIGURATION



VCC2 1
Q1 2
Q̄0 3
D0 4
D1 5
D2 6
D3 7
VEE 8
16 VCC1
15 D10
14 D9
13 D8
12 D7
11 D6
10 D5
9 D4
CD08580S

Figure 1

## LOGIC SYMBOL



16
1
VCC1
VCC2
4 D0
5 D1
6 D2
7 D3
9 D4
D5
10
11 D6
12 D7
13 D8
14 D9
15 D10
Q1 2
Q̄0 3
VEE
8
LD04830S

Figure 2

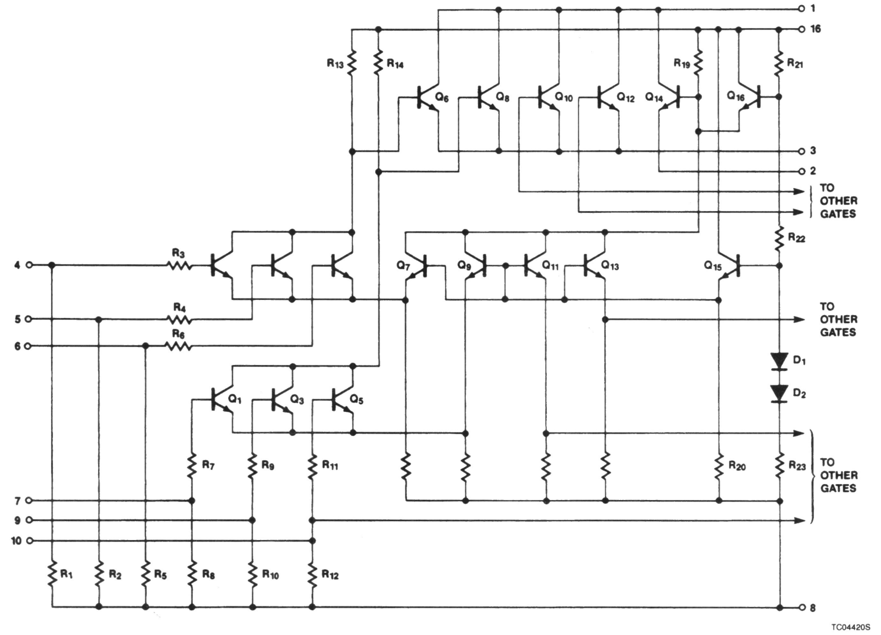
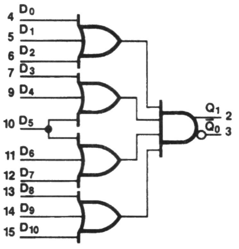

1
16
3
2
4
5
6
7
9
10
8
R13
R14
R19
R21
R22
R3
R4
R6
R7
R9
R11
R20
R23
R1
R2
R5
R8
R10
R12
Q6
Q8
Q10
Q12
Q14
Q16
Q7
Q9
Q11
Q13
Q15
Q1
Q3
Q5
D1
D2
TO OTHER GATES
TO OTHER GATES
TO OTHER GATES
TC04420S

Figure 3. Circuit Diagram


4 D0
5 D1
6 D2
7 D3
9 D4
10 D5
11 D6
12 D7
13 D8
14 D9
15 D10
Q1 2
Q̄0 3

$Q_1 = (D_0 + D_1 + D_2) \cdot (D_3 + D_4 + D_5)$
$\cdot (D_5 + D_6 + D_7) \cdot (D_8 + D_9 + D_{10})$

$Q_0 = \overline{Q}_1$

Positive logic: HIGH state = 1
LOW state = 0

LD05491S

Figure 4. Logic Diagram

# Gate

# 10121

**ABSOLUTE MAXIMUM RATINGS** (Operation beyond the limits set forth in this table may impair useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | | 10K ECL | UNIT |
|---|---|---|---|---|
| $V_{EE}$ | Supply voltage | | −8.0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | | 0 to $V_{EE}$ | V |
| $I_O$ | Output current | | −50 | mA |
| $T_S$ | Storage temperature | | −55 to +150 | °C |
| $T_J$ | Maximum junction temperature | Ceramic package | +165 | °C |
| | | Plastic package | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | 10K ECL | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | −5.2 | | V |
| $V_{IH}$ | HIGH level input voltage | $T_A = -30°C$ | | | −890 | mV |
| | | $T_A = +25°C$ | | | −810 | mV |
| | | $T_A = +85°C$ | | | −700 | mV |
| $V_{IHT}$ | HIGH level input threshold voltage | $T_A = -30°C$ | −1205 | | | mV |
| | | $T_A = +25°C$ | −1105 | | | mV |
| | | $T_A = +85°C$ | −1035 | | | mV |
| $V_{ILT}$ | LOW level input threshold voltage | $T_A = -30°C$ | | | −1500 | mV |
| | | $T_A = +25°C$ | | | −1475 | mV |
| | | $T_A = +85°C$ | | | −1440 | mV |
| $V_{IL}$ | LOW level input voltage | $T_A = -30°C$ | −1890 | | | mV |
| | | $T_A = +25°C$ | −1850 | | | mV |
| | | $T_A = +85°C$ | −1825 | | | mV |
| $T_A$ | Operating ambient temperature | | −30 | +25 | +85 | °C |

**NOTE:**
When operating at $V_{EE}$ other than specified voltage (−5.2V), the DC and AC Characteristics will vary slightly from specified values.
(See table of DC Characteristics)

## Gate

## 10121

**DC ELECTRICAL CHARACTERISTICS** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$, output loading with 50Ω to −2.0V ±0.010V unless otherwise specified[1, 3]

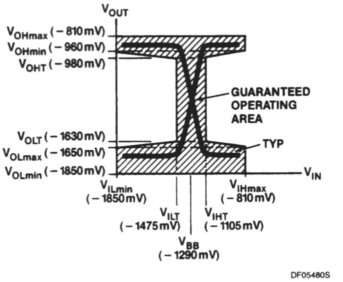
| PARAMETER | | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | | $T_A = -30°C$ | −1060 | | −780 | mV | For $Q_1$ output, apply $V_{IHmax}$ to all inputs.<br>For $\overline{Q}_0$ output, apply $V_{ILmin}$ to all inputs. |
| | | | $T_A = +25°C$ | −960 | | −700 | mV | |
| | | | $T_A = +85°C$ | −890 | | −590 | mV | |
| $V_{OHT}$ | HIGH level output threshold voltage | | $T_A = -30°C$ | −1080 | | | mV | For $Q_1$ output, apply $V_{IHT}$ to $D_0$ input with $V_{ILmin}$ applied to $D_1$ and $D_2$ inputs and $V_{IHmax}$ applied to all other inputs.<br>For $\overline{Q}_0$ output, apply $V_{ILT}$ to $D_0$ input with $V_{ILmin}$ applied to $D_1$ and $D_2$ and $V_{IHmax}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | −980 | | | mV | |
| | | | $T_A = +85°C$ | −910 | | | mV | |
| $V_{OLT}$ | LOW level output threshold voltage | | $T_A = -30°C$ | | | −1655 | mV | For $Q_1$ output, apply $V_{ILT}$ to $D_0$ input with $V_{ILmin}$ applied to $D_1$ and $D_2$ inputs and $V_{IHmax}$ applied to all other inputs.<br>For $\overline{Q}_0$ output, apply $V_{IHT}$ to $D_0$ inputs with $V_{ILmin}$ applied to $D_1$ and $D_2$ inputs and $V_{IHmax}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | | | −1630 | mV | |
| | | | $T_A = +85°C$ | | | −1595 | mV | |
| $V_{OL}$ | LOW level output voltage | | $T_A = -30°C$ | −2000 | | −1675 | mV | For $Q_1$ output, apply $V_{ILmin}$ to all inputs.<br>For $\overline{Q}_0$ output, apply $V_{IHmax}$ to all inputs. |
| | | | $T_A = +25°C$ | −1990 | | −1650 | mV | |
| | | | $T_A = +85°C$ | −1920 | | −1615 | mV | |
| $I_{IH}$ | HIGH level input current | $D_5$ input | $T_A = -30°C$ | | | 495 | μA | Apply $V_{IHmax}$ to each input under test, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | | | 310 | μA | |
| | | | $T_A = +85°C$ | | | 310 | μA | |
| | | Other inputs | $T_A = -30°C$ | | | 390 | μA | |
| | | | $T_A = +25°C$ | | | 245 | μA | |
| | | | $T_A = +85°C$ | | | 245 | μA | |
| $I_{IL}$ | LOW level input current | | $T_A = -30°C$ | 0.5 | | | μA | Apply $V_{ILmin}$ to each input under test one at a time with $V_{IHmax}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | 0.5 | | | μA | |
| | | | $T_A = +85°C$ | 0.3 | | | μA | |
| $-I_{EE}$ | $V_{EE}$ supply current | | $T_A = -30°C$ | | | 29 | mA | |
| | | | $T_A = +25°C$ | | 20 | 26 | mA | |
| | | | $T_A = +85°C$ | | | 29 | mA | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | | $T_A = +25°C$ | | 0.016 | | V/V | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | | 0.250 | | V/V | |
| $\frac{\Delta V_{BB}}{\Delta V_{EE}}$ | Reference bias voltage compensation | | | | 0.148 | | V/V | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst-case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 5.

## Gate

## 10121



**NOTES:**

$V_{IHmax}$ – Maximum HIGH level input voltage (the most positive $V_{IH}$).

$V_{IHT}$ – HIGH level input threshold voltage.

$V_{ILT}$ – LOW level input threshold voltage.

$V_{ILmin}$ – Minimum LOW level input voltage (the most negative $V_{IL}$).

$V_{OHmax}$ – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition.

$V_{OHmin}$ – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition.

$V_{OHT}$ – HIGH level output threshold voltage with the inputs set to their respective threshold levels.

$V_{OLT}$ – LOW level output threshold voltage with the inputs set to their respective threshold levels.

$V_{OLmax}$ – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions.

$V_{OLmin}$ – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions.

$V_{BB}$ – Reference Bias voltage. The internally generated reference voltage which is used to set the input and output threshold level.

**Figure 5. Transfer Characteristics**

## AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$

| PARAMETER | $T_A = -30°C$ | | $T_A = +25°C$ | | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Typ | Max | Min | Max | | |
| $t_{PLH}$ Propagation delay | 1.4 | 3.9 | 1.4 | 2.3 | 3.4 | 1.4 | 3.8 | ns | Figs. 6, 7, 8 |
| $D_n$ to $\overline{Q}_0$, $Q_1$ | 1.4 | 3.9 | 1.4 | 2.3 | 3.4 | 1.4 | 3.8 | ns | |
| $t_{TLH}$ Transition time | 0.9 | 4.1 | 1.1 | 2.5 | 4.0 | 1.1 | 4.6 | ns | Figs. 6, 7, 8 |
| $t_{THL}$ 20% to 80%, 80% to 20% | 0.9 | 4.1 | 1.1 | 2.5 | 4.0 | 1.1 | 4.6 | ns | |

## AC WAVEFORMS

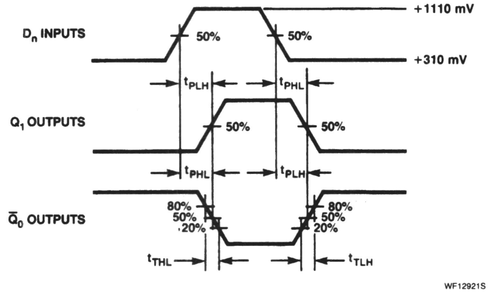
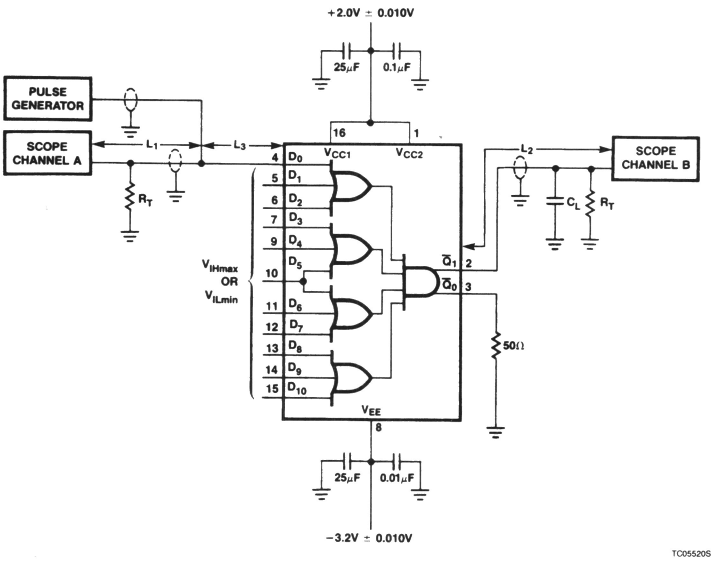


**Figure 6. Propagation Delay and Transition Times**

# Gate

# 10121

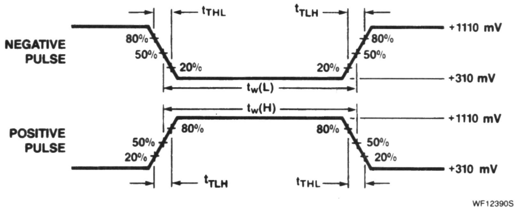
## TEST CIRCUITS AND WAVEFORMS


+2.0V ± 0.010V
25μF
0.1μF
PULSE GENERATOR
SCOPE CHANNEL A
L1
L3
R_T
16
1
4 D0
5 D1
6 D2
7 D3
9 D4
10 D5
11 D6
12 D7
13 D8
14 D9
15 D10
VCC1
VCC2
V_IHmax OR V_ILmin
Q̄1 2
Q̄0 3
VEE
8
L2
SCOPE CHANNEL B
C_L
R_T
50Ω
25μF
0.01μF
−3.2V ± 0.010V
TC05520S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1μF and 25μF from GND to $V_{CC}$, 0.01μF and 25μF from GND to $V_{EE}$ (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than ¼ inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed ¼ inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than ¼ inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance < 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed ¼ inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.

Figure 7. AC Test Circuit for 10121


NEGATIVE PULSE
POSITIVE PULSE
t_THL
t_TLH
80%
50%
20%
t_w(L)
t_w(H)
+1110 mV
+310 mV
WF12390S

| INPUT PULSE REQUIREMENTS<br>$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$, $V_T$ = GND (0V) | | | | | |
|---|---|---|---|---|---|
| **Family** | **Amplitude** | **Rep Rate** | **Pulse Width** | **$t_{TLH}$** | **$t_{THL}$** |
| 10K ECL | 800mVp-p | 1MHz | 500ns | 2.0 ±0.2ns | 2.0 ±0.2ns |

Figure 8. Input Pulse Definition

Signetics

# 10123
## Bus Driver

**Triple 4-3-3-Input Bus Driver**
***Product Specification***

### DESCRIPTION

The 10123 consists of three NOR Gates for use as Drivers. Each can drive a bus with characteristic impedance of not less than 25Ω, such as the case of a bus terminated at both ends in 50Ω. When the output is LOW it presents a high impedance to the bus so that its characteristic impedance is not reduced. All unused inputs can be left open due to integrated pull-down resistors which avoid the need for a supply voltage.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 10123 | 3.0ns | 71mA |

### ORDERING CODE

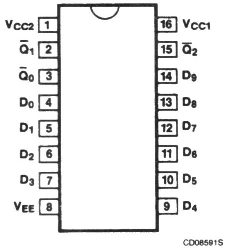
| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V$<br>$T_A = -30°C$ to $+85°C$ |
|---|---|
| Plastic DIP | 10123N |
| Ceramic DIP | 10123F |

### PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_0 - D_9$ | Data Inputs |
| $\overline{Q}_0 - \overline{Q}_2$ | Data Outputs |

6

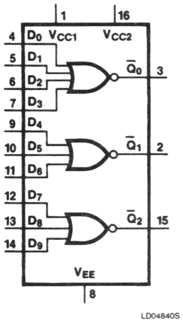
### PIN CONFIGURATION



VCC2 1
Q̄1 2
Q̄0 3
D0 4
D1 5
D2 6
D3 7
VEE 8
16 VCC1
15 Q̄2
14 D9
13 D8
12 D7
11 D6
10 D5
9 D4
CD08591S

Figure 1

### LOGIC SYMBOL

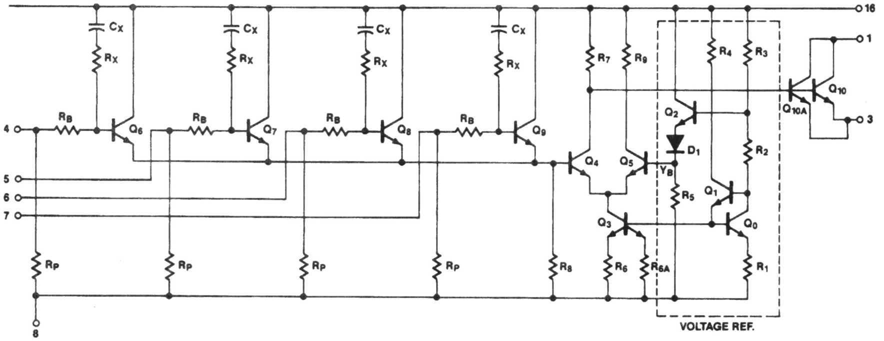


1
16
D0 VCC1
VCC2
4
5 D1
6 D2
7 D3
Q̄0 3
9 D4
10 D5
11 D6
Q̄1 2
12 D7
13 D8
14 D9
Q̄2 15
VEE
8
LD04840S

Figure 2

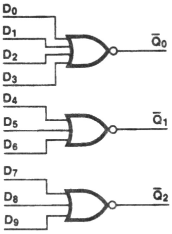
# Bus Driver

# 10123


16
1
3
4
5
6
7
8
Cx
Rx
RB
Rp
Q6
Q7
Q8
Q9
Q4
Q5
Q3
Q2
Q1
Q0
Q10
Q10A
R7
R9
R4
R3
R2
R5
R6
R6A
R8
R1
D1
YB
VOLTAGE REF.

TC04431S

Figure 3. Circuit Diagram (One Gate)


D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
$\overline{Q}_0$
$\overline{Q}_1$
$\overline{Q}_2$

$Q_1 = \overline{D_0 + D_1 + D_2 + D_3}$
$Q_1 = \overline{D_4 + D_5 + D_6}$
$Q_2 = \overline{D_7 + D_8\ D_9}$

Positive logic: HIGH state = 1
LOW state = 0

LD04850S

Figure 4. Logic Diagrams

## ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | | 10K ECL | UNIT |
|---|---|---|---|---|
| $V_{EE}$ | Supply voltage | | −8.0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | | 0 to $V_{EE}$ | V |
| $I_O$ | Output current | | −90 | mA |
| $T_S$ | Storage temperature | | −55 to +150 | °C |
| $T_J$ | Maximum junction temperature | Ceramic package | +165 | °C |
| | | Plastic package | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | 10K ECL | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | −5.2 | | V |
| $V_{IH}$ | HIGH level input voltage | $T_A$ = −30°C | | | −890 | mV |
| | | $T_A$ = +25°C | | | −810 | mV |
| | | $T_A$ = +85°C | | | −700 | mV |
| $V_{IHT}$ | HIGH level input threshold voltage | $T_A$ = −30°C | −1205 | | | mV |
| | | $T_A$ = +25°C | −1105 | | | mV |
| | | $T_A$ = +85°C | −1035 | | | mV |
| $V_{ILT}$ | LOW level input threshold voltage | $T_A$ = −30°C | | | −1500 | mV |
| | | $T_A$ = +25°C | | | −1475 | mV |
| | | $T_A$ = +85°C | | | −1440 | mV |
| $V_{IL}$ | LOW level input voltage | $T_A$ = −30°C | −1890 | | | mV |
| | | $T_A$ = +25°C | −1850 | | | mV |
| | | $T_A$ = +85°C | −1825 | | | mV |
| $T_A$ | Operating ambient temperature | | −30 | +25 | +85 | °C |

**NOTE:**
When operating at $V_{EE}$ other than specified voltage (−5.2V), the DC and AC Characteristics will vary slightly from specified values. (See table of DC Characteristics)

## DC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$, output loading with 25Ω to −2.1V ±0.010V unless otherwise specified[1,3]

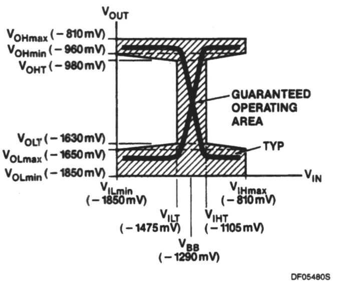
| PARAMETER | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | $T_A = -30°C$ | −1060 | | −890 | mV | Apply $V_{ILmin}$ to all inputs. |
| | | $T_A = +25°C$ | −960 | | −810 | mV | |
| | | $T_A = +85°C$ | −890 | | −700 | mV | |
| $V_{OHT}$ | HIGH level output threshold voltage | $T_A = -30°C$ | −1080 | | −2010 | mV | Apply $V_{ILT}$ to one input of each gate, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | $T_A = +25°C$ | −980 | | −2010 | mV | |
| | | $T_A = +85°C$ | −910 | | −2010 | mV | |
| $V_{OLT}$ | LOW level output threshold voltage | $T_A = -30°C$ | | | −2010 | mV | Apply $V_{IHT}$ to one input of each gate, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | $T_A = +25°C$ | | | −2010 | mV | |
| | | $T_A = +85°C$ | | | −2010 | mV | |
| $V_{OL}$ | LOW level output voltage | $T_A = -30°C$ | −2100 | | −2030 | mV | Apply $V_{IHmax}$ to all inputs. |
| | | $T_A = +25°C$ | −2100 | | −2030 | mV | |
| | | $T_A = +85°C$ | −2100 | | −2030 | mV | |
| $I_{IH}$ | HIGH level input current | $T_A = -30°C$ | | | 350 | μA | Apply $V_{IHmax}$ to each input under test, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | $T_A = +25°C$ | | | 220 | μA | |
| | | $T_A = +85°C$ | | | 220 | μA | |
| $I_{IL}$ | LOW level input current | $T_A = -30°C$ | 0.5 | | | μA | Apply $V_{IHmax}$ to each input under test, one at a time, with $V_{IHmax}$ applied to all other inputs. |
| | | $T_A = +25°C$ | 0.5 | | | μA | |
| | | $T_A = +85°C$ | 0.3 | | | μA | |
| $-I_{EE}$ | $V_{EE}$ supply current | $T_A = -30°C$ | | | 82 | mA | Apply $V_{IHmax}$ to all inputs. |
| | | $T_A = +25°C$ | | 71 | 75 | mA | |
| | | $T_A = +85°C$ | | | 82 | mA | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | $T_A = +25°C$ | | 0.016 | | V/V | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | 0.250 | | V/V | |
| $\frac{\Delta V_{BB}}{\Delta V_{EE}}$ | Reference Bias voltage compensation | | | 0.148 | | V/V | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst-case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 5.

## Bus Driver

## 10123


$V_{OUT}$
$V_{OHmax}$ (−810mV)
$V_{OHmin}$ (−960mV)
$V_{OHT}$ (−980mV)
GUARANTEED OPERATING AREA
$V_{OLT}$ (−1630mV)
$V_{OLmax}$ (−1650mV)
$V_{OLmin}$ (−1850mV)
TYP
$V_{IN}$
$V_{ILmin}$ (−1850mV)
$V_{IHmax}$ (−810mV)
$V_{ILT}$ (−1475mV)
$V_{IHT}$ (−1105mV)
$V_{BB}$ (−1290mV)
DF05480S

**NOTES:**

$V_{IHmax}$ – Maximum HIGH level input voltage (the most positive $V_{IH}$).
$V_{IHT}$ – HIGH level input threshold voltage.
$V_{ILT}$ – LOW level input threshold voltage.
$V_{ILmin}$ – Minimum LOW level input voltage (the most negative $V_{IL}$).
$V_{OHmax}$ – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition.
$V_{OHmin}$ – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition.
$V_{OHT}$ – HIGH level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLT}$ – LOW level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLmax}$ – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions.
$V_{OLmin}$ – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions.
$V_{BB}$ – Reference bias voltage (the internally generated reference voltage which is used to set the input and output threshold level).

**Figure 5. Transfer Characteristics**

## AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = +2.1V \pm 0.010V$, $V_{EE} = -3.1V \pm 0.010V$

| PARAMETER | $T_A = -30°C$ | | $T_A = +25°C$ | | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Typ | Max | Min | Max | | |
| $t_{PLH}$ Propagation delay | 1.2 | 4.6 | 1.2 | 3.0 | 4.4 | 1.2 | 4.8 | ns | Figs. 6, 7, 8 |
| $t_{PHL}$ $D_n$ to $\overline{Q}_n$ | 1.2 | 4.6 | 1.2 | 3.0 | 4.4 | 1.2 | 4.8 | ns | |
| $t_{TLH}$ Transition time | 1.0 | 3.7 | 1.0 | 2.5 | 3.5 | 1.0 | 3.9 | ns | Figs. 6, 7, 8 |
| $t_{THL}$ 20% to 80%, 80% to 20% | 1.0 | 3.7 | 1.0 | 2.5 | 3.5 | 1.0 | 3.9 | ns | |

## AC WAVEFORMS

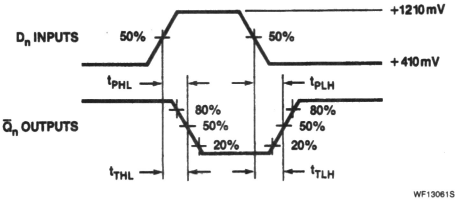
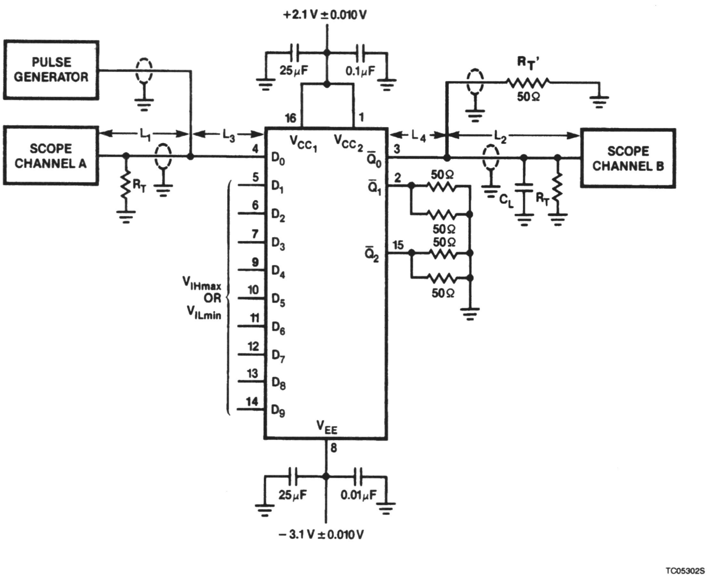

$D_n$ INPUTS
50%
50%
+1210mV
+410mV
$t_{PHL}$
$t_{PLH}$
$\overline{Q}_n$ OUTPUTS
80%
50%
20%
80%
50%
20%
$t_{THL}$
$t_{TLH}$
WF13061S

**Figure 6. Propagation Delay and Transition Times**

# Bus Driver

# 10123

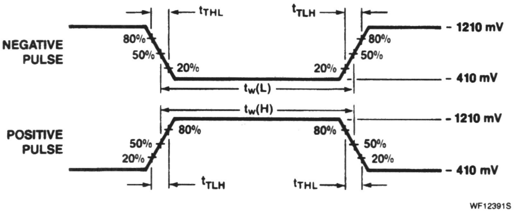
## TEST CIRCUITS AND WAVEFORMS


+2.1 V ± 0.010 V
PULSE GENERATOR
SCOPE CHANNEL A
$L_1$
$L_3$
$R_T$
25μF
0.1μF
16
1
4
$V_{CC_1}$
$V_{CC_2}$
$D_0$
5
$D_1$
6
$D_2$
7
$D_3$
9
$D_4$
10
$D_5$
11
$D_6$
12
$D_7$
13
$D_8$
14
$D_9$
$V_{IHmax}$ OR $V_{ILmin}$
$V_{EE}$
8
25μF
0.01μF
−3.1 V ± 0.010 V
3
$\bar{Q}_0$
2
$\bar{Q}_1$
15
$\bar{Q}_2$
50Ω
50Ω
50Ω
50Ω
$L_4$
$L_2$
$R_T$'
50Ω
$C_L$
$R_T$
SCOPE CHANNEL B
TC05302S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2.1V \pm 0.010V$, $V_{EE} = -3.1V \pm 0.010V$
2. Decoupling 0.1μF and 25μF from GND to $V_{CC}$, 0.01μF and 25μF from GND to $V_{EE}$. (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 25Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$ and $L_4$, the distance from the DUT input and output pins to the junction of their respective interconnecting cables, should not exceed 1/4 inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope. $R_T$ = 50Ω termination resistor at the end of a 50Ω impedance line, the length of which is irrelevant but should be kept as short as possible to reduce stray capacitance.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance $\leqslant$ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ±1% or better.

Figure 7. AC Test Circuit for 10123


NEGATIVE PULSE
POSITIVE PULSE
$t_{THL}$
$t_{TLH}$
80%
50%
20%
$t_w(L)$
$t_w(H)$
− 1210 mV
− 410 mV
WF12391S

| INPUT PULSE REQUIREMENTS<br>$V_{CC1} = V_{CC2} = +2.1V \pm 0.010V$, $V_{EE} = -3.1V \pm 0.010V$, $V_T$ = GND (0V) | | | | | |
|---|---|---|---|---|---|
| Family | Amplitude | Rep Rate | Pulse Width | $t_{TLH}$ | $t_{THL}$ |
| 10K ECL | 800mVp-p | 1MHz | 500ns | 2.0 ± 0.2ns | 2.0 ± 0.2ns |

Figure 8. Input Pulse Definition

# 10124
## Translator

**Quad TTL-to-ECL Translator**
***Product Specification***

**ECL Products**

## DESCRIPTION

The 10124 is a Quad TTL – ECL Translator with an individual Data and a common Select TTL-compatable input on each gate. When the Select input is in the LOW state, all ECL non-inverting outputs are in a LOW state and inverting outputs are in a HIGH state.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 10124 | 3.5ns | 53mA |

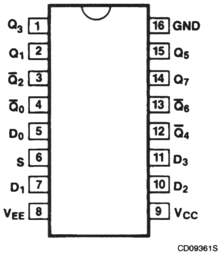
## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = +5V$, GND = 0V, $V_{EE} = -5.2V$ $T_A = -30°C$ to $+85°C$ |
|---|---|
| Plastic DIP | 10124N |
| Ceramic DIP | 10124F |

## PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_0 - D_3$ | Data Inputs (Schottky TTL) |
| S | Select Input (Schottky TTL) |
| $Q_1$, $Q_3$, $Q_5$, $Q_7$ | Data Outputs (AND) (10K ECL) |
| $\overline{Q}_0$, $\overline{Q}_2$, $\overline{Q}_4$, $\overline{Q}_6$ | Data Outputs (NAND) (10K ECL) |

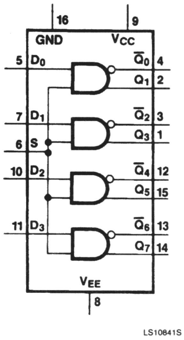
## PIN CONFIGURATION



$Q_3$ 1
$Q_1$ 2
$\overline{Q}_2$ 3
$\overline{Q}_0$ 4
$D_0$ 5
S 6
$D_1$ 7
$V_{EE}$ 8
16 GND
15 $Q_5$
14 $Q_7$
13 $\overline{Q}_6$
12 $\overline{Q}_4$
11 $D_3$
10 $D_2$
9 $V_{CC}$
CD09361S

**Figure 1**

## LOGIC SYMBOL



16
9
GND
$V_{CC}$
5 $D_0$
$\overline{Q}_0$ 4
$Q_1$ 2
7 $D_1$
$\overline{Q}_2$ 3
6 S
$Q_3$ 1
10 $D_2$
$\overline{Q}_4$ 12
$Q_5$ 15
11 $D_3$
$\overline{Q}_6$ 13
$Q_7$ 14
$V_{EE}$
8
LS10841S

**Figure 2**

## Translator

## 10124

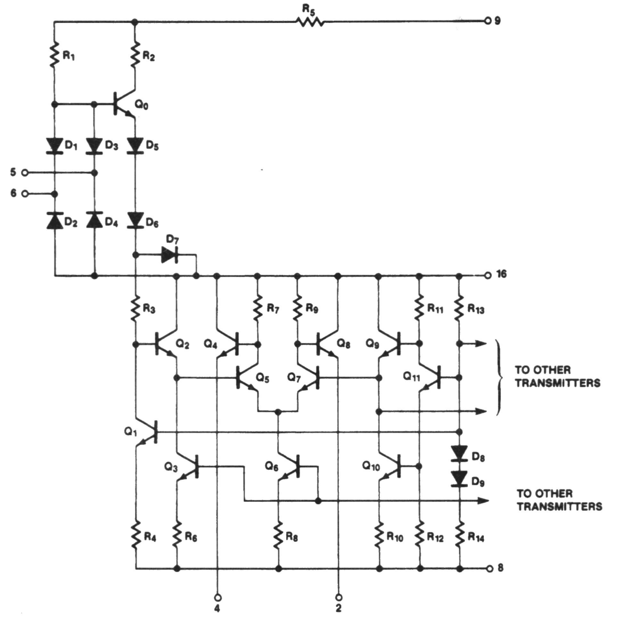
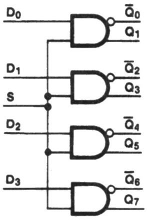

R5
9
R1
R2
Q0
D1
D3
D5
5
6
D2
D4
D6
D7
16
R3
R7
R9
R11
R13
Q2
Q4
Q8
Q9
Q5
Q7
Q11
TO OTHER TRANSMITTERS
Q1
Q3
Q6
Q10
D8
D9
TO OTHER TRANSMITTERS
R4
R6
R8
R10
R12
R14
8
4
2
TC04440S

Figure 3. Circuit Diagram


D0
$\overline{Q_0}$
Q1
D1
$\overline{Q_2}$
Q3
S
D2
$\overline{Q_4}$
Q5
D3
$\overline{Q_6}$
Q7

$Q_0 = \overline{D_0 \cdot S}$
$Q_1 = D_0 \cdot S$
$Q_2 = \overline{D_1 \cdot S}$
$Q_3 = D_1 \cdot S$

$Q_4 = \overline{D_2 \cdot S}$
$Q_5 = D_2 \cdot S$
$Q_6 = \overline{D_3 \cdot S}$
$Q_8 = D_3 \cdot S$

**Positive Logic**
**H = HIGH state = 1**
**L = LOW state = 0**

LD05511S

Figure 4. Logic Diagram

## Translator

## 10124

**ABSOLUTE MAXIMUM RATINGS** (Operation beyond the limits set forth in this table may impair useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | | 10K ECL | UNIT |
|---|---|---|---|---|
| $V_{EE}$ | Supply voltage (negative) | | −8.0 | V |
| $V_{CC}$ | Supply voltage (positive) | | +7.0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more positive than $V_{CC3}$) | | 0 to $V_{CC}$ | V |
| $I_O$ | Output current | | −50 | mA |
| $T_S$ | Storage temperature | | −55 to +150 | °C |
| $T_J$ | Maximum junction temperature | Ceramic package | +165 | °C |
| | | Plastic package | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | 10K ECL | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | |
| GND | Device ground (common) | | 0 | 0 | 0 | V |
| $V_{CC}$ | Supply voltage (positive) | | | 5.0 | | V |
| $V_{EE}$ | Supply voltage (negative) | | | −5.2 | | V |
| $V_{IH}$ | HIGH level input voltage | $T_A = -30°C$ | 2.0 | | 4.0 | V |
| | | $T_A = +25°C$ | 1.8 | | 4.0 | V |
| | | $T_A = +85°C$ | 1.8 | | 4.0 | V |
| $V_{IHT}$ | HIGH level input threshold voltage | $T_A = -30°C$ | 2.0 | | | V |
| | | $T_A = +25°C$ | 1.8 | | | V |
| | | $T_A = +85°C$ | 1.8 | | | V |
| $V_{ILT}$ | LOW level input threshold voltage | $T_A = -30°C$ | | | 1.1 | V |
| | | $T_A = +25°C$ | | | 1.1 | V |
| | | $T_A = +85°C$ | | | 0.9 | V |
| $V_{IL}$ | LOW level input voltage | $T_A = -30°C$ | 0.4 | | 1.1 | V |
| | | $T_A = +25°C$ | 0.4 | | 1.1 | V |
| | | $T_A = +85°C$ | 0.4 | | 0.8 | V |
| $T_A$ | Operating ambient temperature | | −30 | +25 | +85 | °C |

**NOTE:**
When operating at $V_{EE}$ other than specified voltage (−5.2V), the DC and AC Characteristics will vary slightly from specified values. (See table of DC Characteristics)

**DC ELECTRICAL CHARACTERISTICS** GND = 0V, $V_{CC}$ = +5.0V ±0.010V, $V_{EE}$ = −5.2V ±0.010V, $T_A$ = −30°C to +85°C, output loading with 50Ω to −2.0V ±0.010V unless otherwise specified[1,3]

| PARAMETER | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | $T_A$ = −30°C | −1060 | | −890 | mV | For $Q_n$ outputs, apply $V_{IHmax}$ to all inputs.<br>For $\overline{Q}_n$ outputs, apply $V_{ILmin}$ to all inputs. |
| | | $T_A$ = +25°C | −960 | | −810 | mV | |
| | | $T_A$ = +85°C | −890 | | −700 | mV | |
| $V_{OHT}$ | HIGH level output threshold voltage | $T_A$ = −30°C | −1080 | | | mV | For $Q_n$ outputs, apply $V_{IHT}$ to $D_1$ input with $V_{IHmax}$ applied to all other inputs.<br>For $\overline{Q}_n$ outputs, apply $V_{ILT}$ to $D_1$ input with $V_{IHmax}$ applied to all other inputs. |
| | | $T_A$ = +25°C | −980 | | | mV | |
| | | $T_A$ = +85°C | −910 | | | mV | |
| $V_{OLT}$ | LOW level output threshold voltage | $T_A$ = −30°C | | | −1655 | mV | For $Q_n$ outputs, apply $V_{ILT}$ to $D_1$ input with $V_{IHmax}$ applied to all other inputs.<br>For $\overline{Q}_n$ outputs, apply $V_{IHT}$ to $D_1$ input with $V_{IHmax}$ applied to all other inputs. |
| | | $T_A$ = +25°C | | | −1630 | mV | |
| | | $T_A$ = +85°C | | | −1595 | mV | |
| $V_{OL}$ | LOW level output voltage | $T_A$ = −30°C | −1890 | | −1675 | mV | For $Q_n$ outputs, apply $V_{ILmin}$ to all inputs.<br>For $\overline{Q}_n$ outputs, apply $V_{IHmax}$ to all inputs. |
| | | $T_A$ = +25°C | −1850 | | −1650 | mV | |
| | | $T_A$ = +85°C | −1825 | | −1615 | mV | |
| $-I_{EE}$ | $V_{EE}$ supply current | $T_A$ = −30°C | | | 72 | mA | Apply $V_{IHmax}$ to all inputs. |
| | | $T_A$ = +25°C | | 53 | 66 | mA | |
| | | $T_A$ = +85°C | | | 72 | mA | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | $T_A$ = +25°C | | 0.016 | | V/V | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | 0.250 | | V/V | |
| $\frac{\Delta V_{BB}}{\Delta V_{EE}}$ | Reference Bias voltage—compensation | | | 0.148 | | V/V | |

**NOTES:**

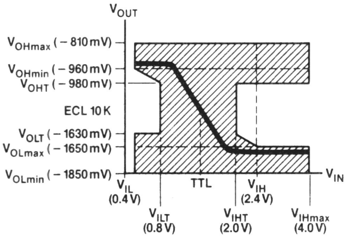
1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst-case testing guidelines, refer to Section 3 Testing, DC testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 5.

# Translator

# 10124

**DC ELECTRICAL CHARACTERISTICS** GND = 0V, $V_{CC} = +5.0V \pm 0.010V$, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$. Output loading with 50Ω to −2.0V ±0.010V unless otherwise specified

| PARAMETER | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|
| $V_{IK}$ | Clamp input voltage | S input | | | −1.5 | V | Apply −20mA to S input. |
| | | other inputs | | | | | Apply −10mA to each input under test, one at a time. |
| $V_{BIN}$ | Input breakdown voltage | | 5.5 | | | V | Apply 1.0mA to each input under test, one at a time. |
| $I_F$ | Forward current | S input | | | −12.8 | mA | Apply VF(0.40V) to S input and VR(2.4V) to all other inputs. |
| | | other inputs | | | −3.2 | mA | Apply VF(0.40V) to each input under test, one at a time, with VR(2.4V) applied to all other inputs. |
| $I_R$ | Reverse current | S input | | | 200 | μA | Apply VR(2.4V) to S input with VF(0.4V) to all other inputs. |
| | | other inputs | | | 50 | μA | Apply VR(2.4V) to each input under test, one at a time with VF(0.4V) to all other inputs. |
| $I_{CCH}$ | Supply current HIGH (positive) | $T_A = -30°C$ | | | 16 | mA | Apply $V_{IHmax}$ to all inputs. |
| | | $T_A = +25°C$ | | | 16 | mA | |
| | | $T_A = +85°C$ | | | 18 | mA | |
| $I_{CCL}$ | Supply current LOW (positive) | | | | 25 | mA | Ground all inputs. |



**NOTES:**

$V_{IHmax}$ – Maximum HIGH level input voltage (the most positive $V_{IH}$).
$V_{IHT}$ – HIGH level input threshold voltage.
$V_{ILT}$ – LOW level input threshold voltage.
$V_{ILmin}$ – Minimum LOW level input voltage (the most negative $V_{IL}$).
$V_{OHmax}$ – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition.
$V_{OHmin}$ – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition.
$V_{OHT}$ – HIGH level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLT}$ – LOW level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLmax}$ – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions.
$V_{OLmin}$ – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions.
$V_{BB}$ – Reference Bias voltage. The internally generated reference voltage which is used to set the input and output threshold level.

**Figure 5. Transfer Characteristics**

# Translator

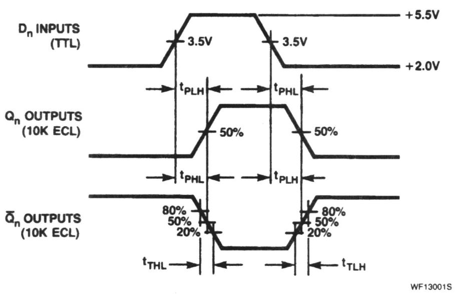
# 10124

## AC ELECTRICAL CHARACTERISTICS

GND = +2.0V ±0.010V, $V_{CC}$ = +7.0V ±0.010V, $V_{EE}$ = −3.2V ±0.010V, $V_T$ = System Gnd.

| PARAMETER | $T_A$ = −30°C | | $T_A$ = +25°C | | | $T_A$ = +85°C | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Typ | Max | Min | Max | | |
| $t_{PLH}$ Propagation delay | 1.0 | 6.5 | 1.0 | 3.5 | 6.0 | 1.0 | 6.5 | ns | Figs. 6, 7, 8 |
| $t_{PHL}$ $D_n$ to $Q_n$, $\overline{Q}_n$ | 1.0 | 6.5 | 1.0 | 3.5 | 6.0 | 1.0 | 6.5 | ns | |
| $t_{TLH}$ Transition time | 1.3 | 4.1 | 1.3 | 2.5 | 3.9 | 1.3 | 4.1 | ns | Figs. 6, 7, 8 |
| $t_{THL}$ 20% to 80%, 80% to 20% | 1.3 | 4.1 | 1.3 | 2.5 | 3.9 | 1.3 | 4.1 | ns | |

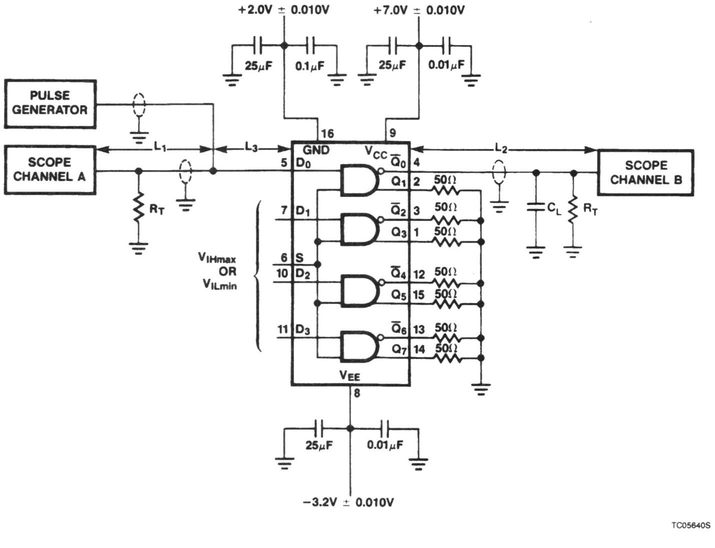
## AC WAVEFORMS



Dn INPUTS (TTL)
+5.5V
3.5V
3.5V
+2.0V
tPLH
tPHL
Qn OUTPUTS (10K ECL)
50%
50%
tPHL
tPLH
Q̄n OUTPUTS (10K ECL)
80%
50%
20%
80%
50%
20%
tTHL
tTLH
WF13001S

Figure 6. Propagation Delay and Transition Times

## TEST CIRCUITS AND WAVEFORMS



+2.0V ± 0.010V
+7.0V ± 0.010V
25μF
0.1μF
25μF
0.01μF
PULSE GENERATOR
SCOPE CHANNEL A
L1
L3
L2
RT
16
9
GND
VCC
5 D0
Q̄0 4
Q1 2
Q̄2 3
Q3 1
7 D1
6 S
10 D2
11 D3
Q̄4 12
Q5 15
Q̄6 13
Q7 14
50Ω
VIHmax OR VILmin
VEE
8
SCOPE CHANNEL B
CL
RT
25μF
0.01μF
−3.2V ± 0.010V
TC05640S

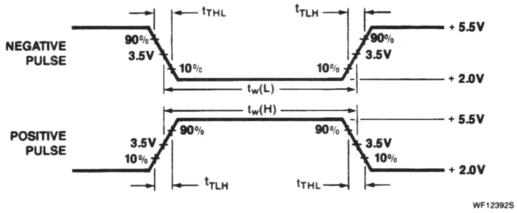
**NOTES:**

1. GND = +2.0V ±0.010V, $V_{CC}$ = +7.0V ±0.010V, $V_{EE}$ = −3.2V + 0.010V.
2. Decoupling 0.1μF and 25μF from GND to Sys. Gnd., 0.01μF and 25μF from $V_{CC}$ to Sys. Gnd. and from $V_{EE}$ to Sys. Gnd. (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than ¼ inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to Sys. Gnd.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed ¼ inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than ¼ inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance < 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed ¼ inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ±1% or better.

Figure 7. AC Test Circuit for 10124

# Translator

# 10124


$t_{THL}$
$t_{TLH}$
NEGATIVE PULSE
90%
3.5V
10%
10%
90%
3.5V
+5.5V
+2.0V
$t_w(L)$
$t_w(H)$
POSITIVE PULSE
3.5V
10%
90%
90%
3.5V
10%
+5.5V
+2.0V
$t_{TLH}$
$t_{THL}$
WF12392S

**INPUT PULSE REQUIREMENTS**
**GND = +2.0V ±0.010V, $V_{CC}$ = +7.0V ±0.010V, $V_{EE}$ = −3.2V ±0.010V,**
**$V_T$ = Sys. Gnd.(0V)**

| Family | Amplitude | Rep Rate | Pulse Width | $t_{TLH}$ | $t_{THL}$ |
|---|---|---|---|---|---|
| 10K ECL | 800mVp-p | 1MHz | 500ns | 2.0 ±0.2ns | 2.0 ±0.2ns |

Figure 8. Input Pulse Definition

Signetics

# 10125
## Gate

**Quad ECL-to-TTL Translator**
***Product Specification***

**ECL Products**

## DESCRIPTION

The 10125 is a Quad ECL – TTL Translator for interfacing data between two different logic systems. It also provides a separate Reference Bias Voltage output ($V_{BB}$) to be used in case of single-ended input busing. Input and output levels are, respectively, ECL 10K and TTL Schottky. This device features a peak common-mode rejection voltage of ± 1V.

The 10125 outputs are designed to go to a LOW logic level whenever both inputs are left open.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 10125 | 3.5ns | 30mA |

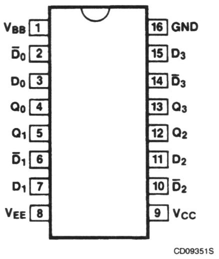
## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>GND = 0V, $V_{CC}$ = +5.0V, $V_{EE}$ = −5.2V<br>$T_A$ = −30°C to +85°C |
|---|---|
| Plastic DIP | 10125N |
| Ceramic DIP | 10125F |

## PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_0 - D_3$, $\overline{D}_0 - \overline{D}_3$ | Data Inputs (ECL 10K) |
| $V_{BB}$ | Reference Bias Voltage Output (ECL 10K) |
| $Q_0 - Q_3$ | Data Outputs (Schottky TTL) |

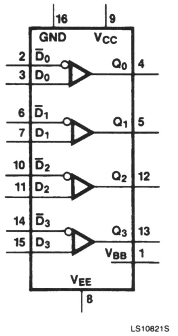
## PIN CONFIGURATION



$V_{BB}$ 1
$\overline{D}_0$ 2
$D_0$ 3
$Q_0$ 4
$Q_1$ 5
$\overline{D}_1$ 6
$D_1$ 7
$V_{EE}$ 8
16 GND
15 $D_3$
14 $\overline{D}_3$
13 $Q_3$
12 $Q_2$
11 $D_2$
10 $\overline{D}_2$
9 $V_{CC}$
CD09351S

Figure 1

## LOGIC SYMBOL



16
9
GND
$V_{CC}$
2 $\overline{D}_0$
3 $D_0$
$Q_0$ 4
6 $\overline{D}_1$
7 $D_1$
$Q_1$ 5
10 $\overline{D}_2$
11 $D_2$
$Q_2$ 12
14 $\overline{D}_3$
15 $D_3$
$Q_3$ 13
$V_{BB}$ 1
$V_{EE}$
8
LS10821S

Figure 2

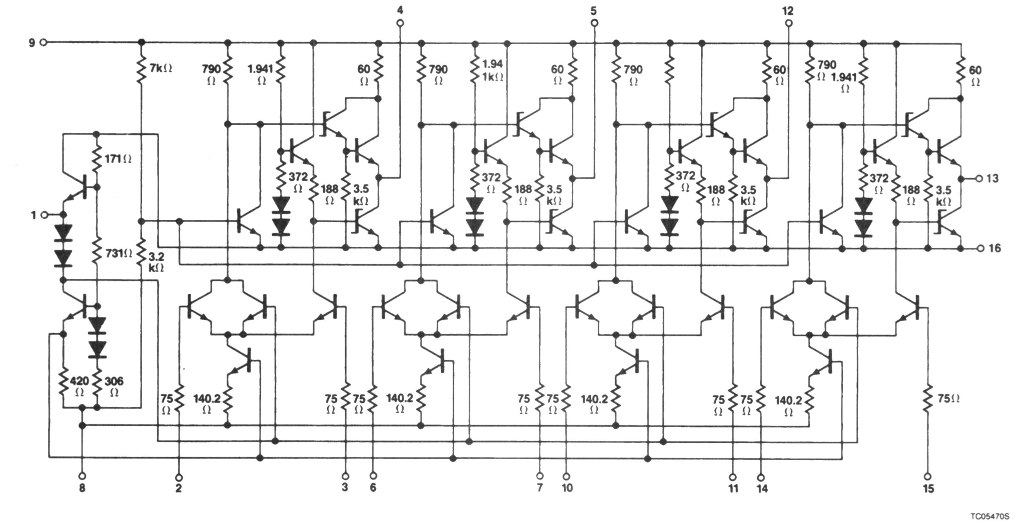
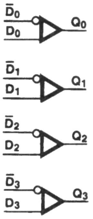

4
5
12
9
1
13
16
8
2
3
6
7
10
11
14
15
7kΩ
790 Ω
1.941 Ω
60 Ω
1.94 1kΩ
171Ω
731Ω
3.2 kΩ
372 Ω
188 Ω
3.5 kΩ
420 Ω
306 Ω
75 Ω
140.2 Ω
75Ω
TC05470S

**Figure 3. Schematic Diagram**


$\overline{D}_0$
$D_0$
$Q_0$
$\overline{D}_1$
$D_1$
$Q_1$
$\overline{D}_2$
$D_2$
$Q_2$
$\overline{D}_3$
$D_3$
$Q_3$

$Q_0 = D_0$
$Q_1 = D_1$
$Q_2 = D_2$
$Q_3 = D_3$
**Positive Logic:**
**HIGH state = 1**
**LOW state = 0**

LD05482S

**Figure 4. Logic Diagram**

**ABSOLUTE MAXIMUM RATINGS** (Operation beyond the limits set forth in this table may impair useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | | 10K ECL | UNIT |
|---|---|---|---|---|
| $V_{EE}$ | Supply voltage (negative) | | −8.0 | V |
| $V_{CC}$ | Supply voltage (positive) | | +7.0 | V |
| $V_{IN(ECL)}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | | 0 to $V_{EE}$ | V |
| $V_{OUT}$ (TTL) | Voltage applied to output in HIGH state | | −0.5 to $+V_{CC}$ | V |
| $T_S$ | Storage temperature | | −55 to +150 | °C |
| $T_J$ | Maximum junction temperature | Ceramic package | +165 | °C |
| | | Plastic package | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | 10K ECL | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | |
| GND | Device ground (common) | | 0 | 0 | 0 | V |
| $V_{CC}$ | Supply Voltage (positive) | | | +5.0 | | V |
| $V_{EE}$ | Supply voltage (negative) | | | −5.2 | | V |
| $V_{IH}$ | HIGH level input voltage | $T_A$ = −30°C | | | −890 | mV |
| | | $T_A$ = +25°C | | | −810 | mV |
| | | $T_A$ = +85°C | | | −700 | mV |
| $V_{IHT}$ | HIGH level input threshold voltage | $T_A$ = −30°C | −1205 | | | mV |
| | | $T_A$ = +25°C | −1105 | | | mV |
| | | $T_A$ = +85°C | −1035 | | | mV |
| $V_{ILT}$ | LOW level input threshold voltage | $T_A$ = −30°C | | | −1500 | mV |
| | | $T_A$ = +25°C | | | −1475 | mV |
| | | $T_A$ = +85°C | | | −1440 | mV |
| $V_{IL}$ | LOW level input voltage | $T_A$ = −30°C | −1890 | | | mV |
| | | $T_A$ = +25°C | −1850 | | | mV |
| | | $T_A$ = +85°C | −1825 | | | mV |
| $T_A$ | Operating ambient temperature | | −30 | +25 | +85 | °C |

## DC OPERATING CONDITIONS FOR COMMON-MODE REJECTION TEST

GND = 0V, $V_{CC}$ = +5.0V ± 0.010V, $V_{EE}$ = −5.2V ± 0.010V

| PARAMETER | | | 10K ECL | | | |
|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | Unit |
| $V_{IHH}$ | $V_{IHmax}$ + 1.0V | $T_A$ = −30°C | | | +110 | mV |
| | | $T_A$ = +25°C | | | +190 | mV |
| | | $T_A$ = +85°C | | | +300 | mV |
| $V_{IHL}$ | $V_{IHmax}$ − 1.0V | $T_A$ = −30°C | | | −1890 | mV |
| | | $T_A$ = +25°C | | | −1810 | mV |
| | | $T_A$ = +85°C | | | −1700 | mV |
| $V_{ILH}$ | $V_{ILmin}$ + 1.0V | $T_A$ = −30°C | −890 | | | mV |
| | | $T_A$ = +25°C | −850 | | | mV |
| | | $T_A$ = +85°C | −825 | | | mV |
| $V_{ILL}$ | $V_{ILmin}$ − 1.0V | $T_A$ = −30°C | −2890 | | | mV |
| | | $T_A$ = +25°C | −2850 | | | mV |
| | | $T_A$ = +85°C | −2825 | | | mV |

**NOTE:**
When operating at $V_{EE}$ other than specified voltage (−5.2V), the DC and AC Characteristics will vary slightly from specified values. (See table of DC Characteristics)

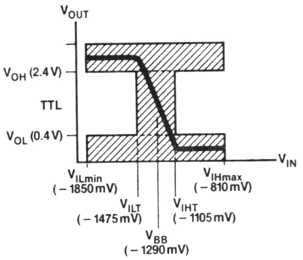
# Gate · 10125

**DC ELECTRICAL CHARACTERISTICS** GND = 0V, $V_{CC}$ = +5.0V ±0.010V, $V_{EE}$ = −5.2V ±0.010V, $T_A$ = −30°C to +85°C unless otherwise specified[1,4]

| PARAMETER | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | | 2.5 | | | V | Apply $V_{IHmax}$ to all non-inverting inputs with $V_{BB}$ applied to all inverting inputs. Force −2.0mA on measured output. (Refer to Fig. 7.) |
| $V_{OHT}$ | HIGH level output threshold voltage | | 2.5 | | | V | Apply $V_{IHT}$ to each non-inverting input, one at time, with $V_{ILmin}$ applied to all other non-inverting input and $V_{BB}$ applied to all inverting inputs. Force −2.0mA on measured output. (Refer to Fig. 7.) |
| $V_{OHT}$ | LOW level output threshold voltage | | | | 0.5 | V | Apply $V_{ILT}$ to each non-inverting input one at time, with $V_{IHmax}$ applied to all other non-inverting input and $V_{BB}$ applied to all inverting inputs. Force 20mA on measured output. (Refer to Fig. 7.) |
| $V_{OL}$ | LOW level output voltage | | | | 0.5 | V | Apply $V_{ILmin}$ to all non-inverting inputs with $V_{BB}$ applied to all inverting inputs. Force 20mA on measured output. (Refer to Fig. 7.) |
| $V_{BB}$ | Reference Bias voltage | | −1420 | | −1280 | mV | Connect all inverting inputs to $V_{BB}$ pin during test. All other inputs are not connected. |
| | | | −1350 | −1290 | −1230 | mV | |
| | | | −1295 | | −1150 | mV | |
| $V_{OH}$ | HIGH level output voltage for CMR test | | 2.5 | | | V | Apply $V_{IHH}$ to $D_n$ and $V_{ILH}$ to $\overline{D}_n$ inputs.<br>Apply $V_{IHL}$ to $D_n$ and $V_{ILL}$ to $\overline{D}_n$ inputs.<br>Force −2.0mA on measured output. |
| $V_{OL}$ | LOW level output voltage for CMR test | | | | 0.5 | V | Apply $V_{IHH}$ to $\overline{D}_n$ and $V_{ILH}$ to $D_n$ inputs.<br>Apply $V_{IHL}$ to $\overline{D}_n$ and $V_{ILL}$ to $D_n$ inputs.<br>Force +20mA on measured output. |
| $V_{OLS1}$ | Indeterminate input protection test | | | | 0.5 | V | Apply $V_{EE}$ to all inputs. Force 20mA on measured output. |
| $V_{OLS2}$ | Indeterminate input protection test | | | | 0.5 | V | All inputs left floating. Force 20mA on measured output. |
| $I_{IH}$ | HIGH level input current | $T_A$ = −30°C | | | 180 | μA | Apply $V_{IHmax}$ to each input under test, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | $T_A$ = +25°C | | | 115 | μA | |
| | | $T_A$ = +85°C | | | 115 | μA | |
| $-I_{CBO}$ | Input leakage current | $T_A$ = −30°C | | | 1.5 | μA | Apply $V_{EE}$ to each inverting input under test, one at a time, with $V_{ILmin}$ applied to all other inverting inputs and $V_{BB}$ applied to all non-inverting inputs. (Refer to Fig. 7.) |
| | | $T_A$ = +25°C | | | 1.0 | μA | |
| | | $T_A$ = +85°C | | | 1.0 | μA | |
| $-I_{EE}$ | $V_{EE}$ supply current | $T_A$ = −30°C | | | 44 | mA | Apply $V_{BB}$ to all $\overline{D}_n$ inputs and $V_{ILmin}$ to all $D_n$ inputs. |
| | | $T_A$ = +25°C | | 30 | 40 | mA | |
| | | $T_A$ = +85°C | | | 44 | mA | |
| $I_{OS}$ | Short circuit[3] current | $T_A$ = −30°C | | | 40 | mA | Apply $V_{ILmin}$ to all $\overline{D}_n$ inputs with $V_{BB}$ applied to all $D_n$ inputs. Test each output, one at a time, with all other outputs unloaded. Force 0V (GND) on measured output[3]. |
| | | $T_A$ = +25°C | | | 40 | mA | |
| | | $T_A$ = +85°C | | | 40 | mA | |
| $I_{CCH}$ | Supply current HIGH | | | | 52 | mA | Apply $V_{IHmax}$ to all $\overline{D}_n$ inputs with $V_{BB}$ applied to $D_n$ inputs. |
| $I_{CCL}$ | Supply current LOW | | | | 39 | mA | Apply $V_{ILmin}$ to all $\overline{D}_n$ inputs with $V_{BB}$ applied to $D_n$ inputs. |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to Section 3 Testing, DC Testing.
3. Not more than one output should be shorted at a time. For testing $I_{OS}$, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, $I_{OS}$ tests should be performed last.
4. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 5.



**NOTES:**

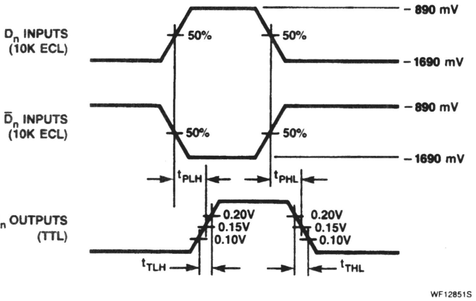
$V_{IHmax}$ – Maximum HIGH level input voltage (the most positive $V_{IH}$).
$V_{IHT}$ – HIGH level input threshold voltage.
$V_{ILT}$ – LOW level input threshold voltage.
$V_{ILmin}$ – Minimum LOW level input voltage (the most negative $V_{IL}$).
$V_{OH}$ – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition.
$V_{OL}$ – Maximum LOW level output voltage (the mos t positive $V_{OL}$) under the specified input and loading conditions.
$V_{BB}$ – Reference Bias voltage. The internally generated reference voltage which is used to set the input and output threshold level.

**Figure 5. Transfer Characteristics**

## AC ELECTRICAL CHARACTERISTICS $GND_1 = +2.0V \pm 0.010V$, $V_{CC} = +7.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$

| PARAMETER | | $T_A = -30°C$ | | $T_A = +25°C$ | | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Typ | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 1.0 | 6.0 | 1.0 | 4.5 | 6.0 | 1.0 | 6.0 | ns | Figs. 6, 7, 9 |
| $t_{PHL}$ | $D_n$ to $Q_n$ | 1.0 | 6.0 | 1.0 | 4.5 | 6.0 | 1.0 | 6.0 | ns | |
| $t_{TLH}$ | Transition time | 0.5 | 3.3 | 0.5 | — | 3.3 | 0.5 | 3.3 | ns | Figs. 6, 7, 9 |
| $t_{THL}$ | 10% to 90%, 90% to 10% | 0.5 | 3.3 | 0.5 | — | 3.3 | 0.5 | 3.3 | ns | |

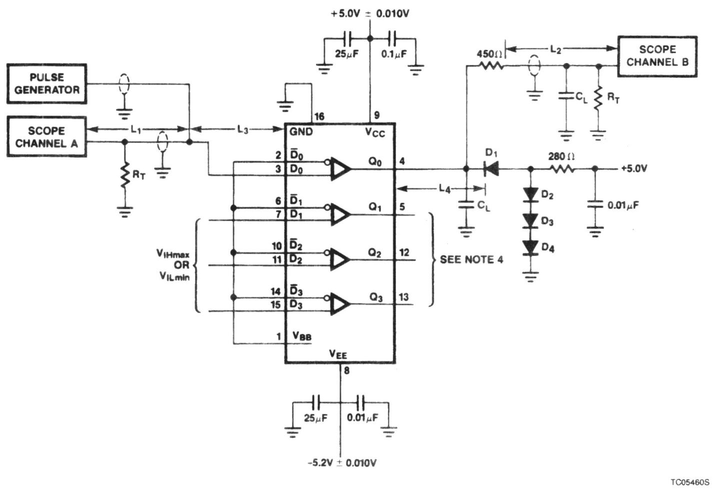
## AC WAVEFORMS


$D_n$ INPUTS (10K ECL)
$\bar{D}_n$ INPUTS (10K ECL)
$Q_n$ OUTPUTS (TTL)
50%
50%
50%
50%
−890 mV
−1690 mV
−890 mV
−1690 mV
$t_{PLH}$
$t_{PHL}$
0.20V
0.15V
0.10V
0.20V
0.15V
0.10V
$t_{TLH}$
$t_{THL}$
WF12851S

**NOTE:**
The output waveform in Figure 6 is shown with the actual output voltages of the test circuit of Figure 5 which are attenuated by a factor of 10 as a result of the voltage divider formed by the 450Ω resistor and $R_T$.

**Figure 6. Propagation Delay and Transition Times**

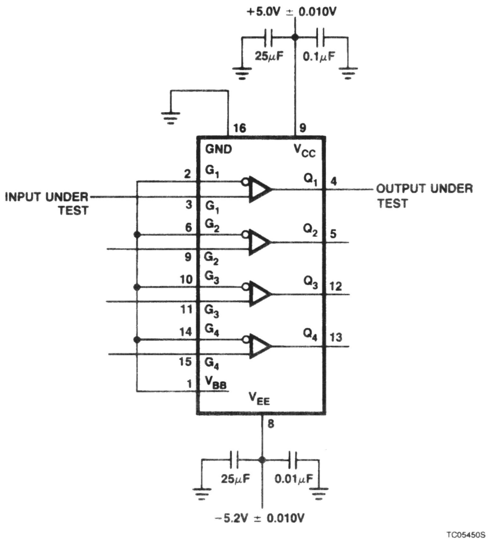
## TEST CIRCUITS AND WAVEFORMS


+5.0V ± 0.010V
25µF
0.1µF
PULSE GENERATOR
SCOPE CHANNEL A
L1
L3
RT
16
9
GND
VCC
2 $\bar{D}_0$
3 $D_0$
$Q_0$
4
6 $\bar{D}_1$
7 $D_1$
$Q_1$
5
10 $\bar{D}_2$
11 $D_2$
$Q_2$
12
14 $\bar{D}_3$
15 $D_3$
$Q_3$
13
1 VBB
VEE
8
VIHmax OR VILmin
SEE NOTE 4
450Ω
L2
SCOPE CHANNEL B
CL
RT
D1
280Ω
+5.0V
L4
CL
D2
D3
D4
0.01µF
25µF
0.01µF
-5.2V ± 0.010V
TC05460S

**NOTES:**

1. GND = System Gnd (0V), $V_{CC}$ = +5.0V ±0.010V, $V_{EE}$ = −5.2V + 0.010V.
2. Decoupling 0.1µF and 25µF from GND to $V_{CC}$, 0.01µF and 25µF from GND to $V_{EE}$ (0.01 and 0.1µF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than ¼ inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded identically to output under test, substituting a 50Ω termination for the scope.
5. $L_1$ and $L_2$ equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed ¼ inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than ¼ inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance ≤ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed ¼ inch (6mm) in length (refer to section on AC setup procedure).
10. $D_1$ through $D_4$ are High Frequency (low capacitance) switching diodes, MMD7000 or equivalent.

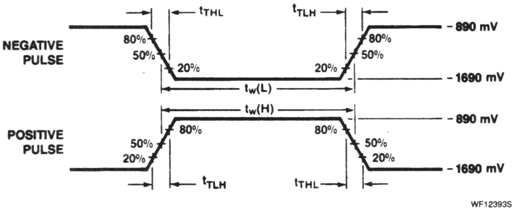
Figure 7. AC Test Circuit 10125


+5.0V ± 0.010V
25µF
0.1µF
16
9
GND
VCC
INPUT UNDER TEST
2 G1
3 G1
6 G2
9 G2
10 G3
11 G3
14 G4
15 G4
1 VBB
Q1 4
Q2 5
Q3 12
Q4 13
OUTPUT UNDER TEST
VEE
8
25µF
0.01µF
−5.2V ± 0.010V
TC05450S

**NOTES:**

1. GND = 0V, $V_{CC}$ = +5.0 ±0.010V, $V_{EE}$ = −5.2V ±0.010V
2. Decoupling 0.1µF and 25µF from GND to $V_{EE}$, 0.01µF and 25µF from GND to $V_T$ (0.01 and 0.1µF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT, and lead length should be kept to less than ¼ inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are open.

Figure 8. DC Test Circuit for 10125


NEGATIVE PULSE
POSITIVE PULSE
$t_{THL}$
$t_{TLH}$
80%
50%
20%
$t_w(L)$
$t_w(H)$
-890 mV
-1690 mV
WF12393S

| INPUT PULSE REQUIREMENTS<br>GND = 0V, $V_{CC}$ = +5.0V ±0.010V, $V_{EE}$ = −5.2V ±0.010V, $V_T$ = GND (0V) | | | | | |
|---|---|---|---|---|---|
| **Family** | **Amplitude** | **Rep Rate** | **Pulse Width** | **$t_{TLH}$** | **$t_{THL}$** |
| 10K ECL | 800mVp-p | 1MHz | 500ns | 2.0 ±0.2ns | 2.0 ±0.2ns |

**Figure 9. Input Pulse Definition**

# 10130
## Latch

**Dual D-Type Latch**
***Product Specification***

**ECL Products**

### DESCRIPTION

The 10130 is a clocked Dual D-Type Latch. Each element can be clocked separately by holding the common clock in the LOW state and using the clock enable inputs for the clocking function. The outputs are latched when the level of the clock is HIGH. All unused inputs must be tied to $V_{IL}$ or $V_{EE}$.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 10130 | 2.5ns | 30mA |

### ORDERING CODE

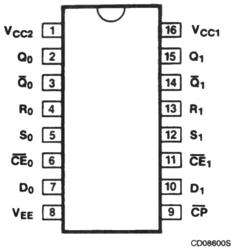
| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} = GND$; $V_{EE} = -5.2V$<br>$T_A = -30°C$ to $+85°C$ |
|---|---|
| Plastic DIP | 10130N |
| Ceramic DIP | 10130F |

### PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_0$, $D_1$ | Data Inputs |
| $\overline{CP}$ | Clock Input |
| $\overline{CE}_0$, $\overline{CE}_1$ | Clock Enable Inputs |
| $S_0$, $S_1$ | Set Inputs |
| $R_0$, $R_1$ | Reset Inputs |
| $Q_0$, $Q_1$, $\overline{Q}_0$, $\overline{Q}_1$ | Data Outputs |

6

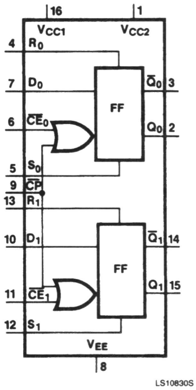
### PIN CONFIGURATION



VCC2 1
Q0 2
Q̄0 3
R0 4
S0 5
C̄Ē0 6
D0 7
VEE 8
16 VCC1
15 Q1
14 Q̄1
13 R1
12 S1
11 C̄Ē1
10 D1
9 C̄P̄
CD08600S

**Figure 1**

### LOGIC SYMBOL



16
1
VCC1
VCC2
4 R0
7 D0
6 C̄Ē0
5 S0
9 C̄P̄
13 R1
10 D1
11 C̄Ē1
12 S1
FF
FF
Q̄0 3
Q0 2
Q̄1 14
Q1 15
VEE
8
LS10830S

**Figure 2**

# Latch

# 10130

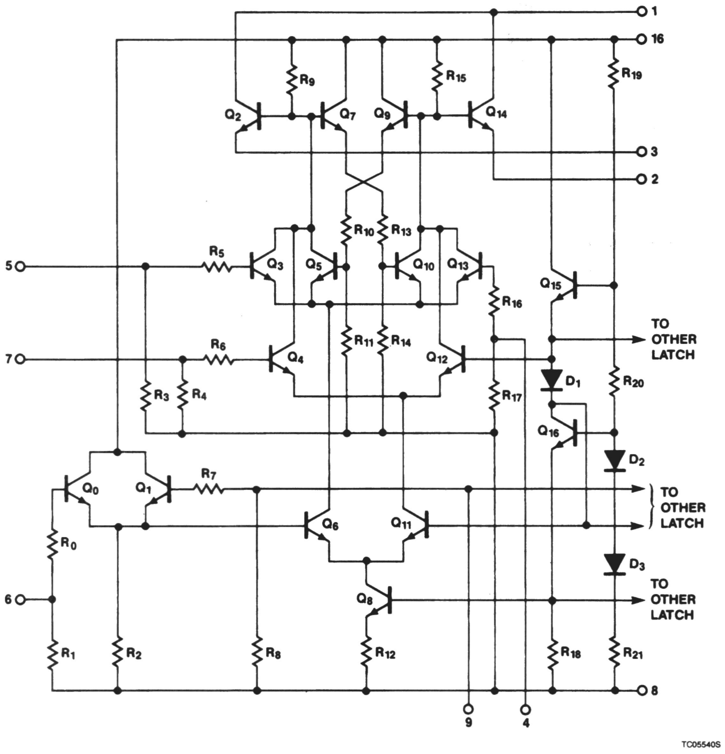

1
16
3
2
5
7
6
8
9
4
R0
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
R17
R18
R19
R20
R21
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
Q16
D1
D2
D3
TO OTHER LATCH
TO OTHER LATCH
TO OTHER LATCH
TC05540S

Figure 3. Circuit Diagram (One Latch)

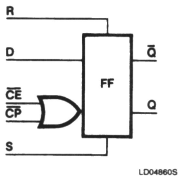

R
D
CE
CP
S
FF
Q̄
Q
LD04860S

Figure 4. Logic Function

## FUNCTION TABLES

### SYNCHRONOUS OPERATION

| $D_n$ | $\overline{CP}$ | $\overline{C}_E$ | $Q_{n+1}$* |
|---|---|---|---|
| L | L | L | L |
| L | L | H | $Q_n$ |
| L | H | L | $Q_n$ |
| L | H | H | $Q_n$ |
| H | L | L | H |
| H | L | H | $Q_n$ |
| H | H | L | $Q_n$ |
| H | H | H | $Q_n$ |

* R and S = LOW

### ASYNCHRONOUS OPERATION

| R | S | $Q_1$ |
|---|---|---|
| L | L | Q |
| L | H | H |
| H | L | L |
| H | H | N |

$\overline{CP}$ or $\overline{C}_E$ = HIGH
Positive Logic:
H = HIGH state (the more positive voltage) = 1
L = LOW state (the less positive voltage) = 0
N = Not allowed

## Latch

## 10130

**ABSOLUTE MAXIMUM RATINGS** (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | | 100K ECL | UNIT |
|---|---|---|---|---|
| $V_{EE}$ | Supply voltage ($V_{CC1} = V_{CC2} =$ GND) | | -8.0 to 0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | | 0 to $V_{EE}$ | V |
| $I_O$ | Output source current | | -50 | mA |
| $T_S$ | Storage temperature | | -55 to +150 | °C |
| $T_J$ | Maximum junction temperature | Ceramic package | +165 | °C |
| | | Plastic package | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | 10K ECL | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | -5.2 | | V |
| $V_{IH}$ | HIGH level input voltage | $T_A = -30°C$ | | | -890 | mV |
| | | $T_A = +25°C$ | | | -810 | mV |
| | | $T_A = +85°C$ | | | -700 | mV |
| $V_{IHT}$ | HIGH level input threshold voltage | $T_A = -30°C$ | -1205 | | | mV |
| | | $T_A = +25°C$ | -1105 | | | mV |
| | | $T_A = +85°C$ | -1035 | | | mV |
| $V_{ILT}$ | LOW level input threshold voltage | $T_A = -30°C$ | | | -1500 | mV |
| | | $T_A = +25°C$ | | | -1475 | mV |
| | | $T_A = +85°C$ | | | -1440 | mV |
| $V_{IL}$ | LOW level input voltage | $T_A = -30°C$ | -1890 | | | mV |
| | | $T_A = +25°C$ | -1850 | | | mV |
| | | $T_A = +85°C$ | -1825 | | | mV |
| $T_A$ | Operating ambient temperature | | -30 | +25 | +85 | °C |

**NOTE:**
When operating at $V_{EE}$ other than specified voltage (-5.2V), the DC and AC Characteristics will vary slightly from specified values.
(See table of DC Characteristics)

## DC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2}$ = GND, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$, output loading with 50Ω to −2.0V ±0.010V unless otherwise specified[1,3]

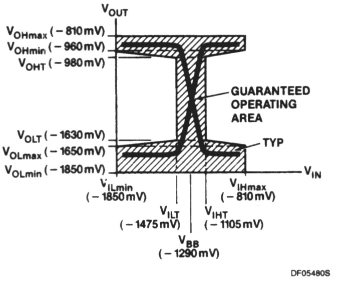
| PARAMETER | | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | | $T_A = -30°C$ | -1060 | | -890 | mV | For $Q_n$ output, apply $V_{IHmax}$ to each $D_n$ input, one at a time, with $V_{ILmin}$ applied to all other inputs.<br>For $\overline{Q}_n$ output, apply $V_{ILmin}$ to all inputs. |
| | | | $T_A = +25°C$ | -960 | | -810 | mV | |
| | | | $T_A = +85°C$ | -890 | | -700 | mV | |
| $V_{OHT}$ | HIGH level output threshold voltage | | $T_A = -30°C$ | -1080 | | | mV | For $Q_n$ output, apply $V_{IHT}$ to each $D_n$ input, one at a time, with $V_{ILmin}$ applied to all other inputs.<br>For $\overline{Q}_n$ output, apply $V_{ILT}$ to each $D_n$ input, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | -980 | | | mV | |
| | | | $T_A = +85°C$ | -910 | | | mV | |
| $V_{OLT}$ | LOW level output threshold voltage | | $T_A = -30°C$ | | | -1655 | mV | For $Q_n$ output, apply $V_{ILT}$ to each $D_n$ input, one at a time, with $V_{ILmin}$ applied to all other inputs.<br>For $\overline{Q}_n$ output, apply $V_{IHT}$ to each $D_n$ input, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | | | -1630 | mV | |
| | | | $T_A = +85°C$ | | | -1595 | mV | |
| $V_{OL}$ | LOW level output voltage | | $T_A = -30°C$ | -1890 | | -1675 | mV | For $Q_n$ output, apply $V_{ILmin}$ to all inputs.<br>For $\overline{Q}_n$ output, apply $V_{IHmax}$ to each $D_n$ input, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | -1850 | | -1650 | mV | |
| | | | $T_A = +85°C$ | -1825 | | -1615 | mV | |
| $I_{IH}$ | HIGH level input current | $\overline{CE}_0, \overline{CE}_1$ inputs | $T_A = -30°C$ | | | 360 | μA | Apply $V_{IHmax}$ to each input under test, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | | | 220 | μA | |
| | | | $T_A = +85°C$ | | | 220 | μA | |
| | | $\overline{CP}$ input | $T_A = -30°C$ | | | 425 | μA | Apply $V_{IHmax}$ to $\overline{CP}$ input with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | | | 265 | μA | |
| | | | $T_A = +85°C$ | | | 265 | μA | |
| | | $D_n$ inputs | $T_A = -30°C$ | | | 455 | μA | Apply $V_{IHmax}$ to each $D_n$ input under test, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | | | 285 | μA | |
| | | | $T_A = +85°C$ | | | 285 | μA | |
| | | $R_n$ inputs | $T_A = -30°C$ | | | 455 | μA | Apply $V_{IHmax}$ to $S_n$ and CP inputs and $R_n$ input under test, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | | | 285 | μA | |
| | | | $T_A = +85°C$ | | | 285 | μA | |
| | | $S_n$ inputs | $T_A = -30°C$ | | | 455 | μA | Apply $V_{IHmax}$ to $R_n$ and CP inputs and $S_n$ input under test, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | | | 285 | μA | |
| | | | $T_A = +85°C$ | | | 285 | μA | |
| $I_{IL}$ | LOW level input current | | $T_A = -30°C$ | 0.5 | | | μA | Apply $V_{ILmin}$ to each input under test, one at a time, with $V_{IHmax}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | 0.5 | | | μA | |
| | | | $T_A = +85°C$ | 0.3 | | | μA | |
| $-I_{EE}$ | $V_{EE}$ supply current | | $T_A = -30°C$ | | | 38 | mA | |
| | | | $T_A = +25°C$ | | 30 | 35 | mA | |
| | | | $T_A = +85°C$ | | | 38 | mA | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | | $T_A = +25°C$ | | 0.016 | | V/V | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | | 0.230 | | V/V | |
| $\frac{\Delta V_{BB}}{\Delta V_{EE}}$ | Reference bias voltage compensation | | | | 0.140 | | V/V | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst-case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 5.

# Latch

# 10130



**NOTES:**

| | |
|---|---|
| $V_{IHmax}$ | – Maximum HIGH level input voltage (the most positive $V_{IH}$). |
| $V_{IHT}$ | – HIGH level input threshold voltage. |
| $V_{ILT}$ | – LOW level input threshold voltage. |
| $V_{ILmin}$ | – Minimum LOW level input voltage (the most negative $V_{IL}$). |
| $V_{OHmax}$ | – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition. |
| $V_{OHmin}$ | – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition. |
| $V_{OHT}$ | – HIGH level output threshold voltage with the inputs set to their respective threshold levels. |
| $V_{OLT}$ | – LOW level output threshold voltage with the inputs set to their respective threshold levels. |
| $V_{OLmax}$ | – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions. |
| $V_{OLmin}$ | – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions. |
| $V_{BB}$ | – Reference bias voltage. The internally generated reference voltage which is used to set the input and output threshold level. |

**Figure 5. Transfer Characteristics**

## AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$

| PARAMETER | $T_A = -30°C$ | | $T_A = +25°C$ | | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Typ | Max | Min | Max | | |
| $t_{PLH}$ Propagation delay | 1.0 | 3.6 | 1.0 | 2.5 | 3.5 | 1.0 | 3.8 | ns | Figs. 6, 8, 9 |
| $t_{PHL}$ $D_n$ to $Q_n$, $\overline{Q}_n$ | 1.0 | 3.6 | 1.0 | 2.5 | 3.5 | 1.0 | 3.8 | ns | |
| $t_{PLH}$ Propagation delay | 1.0 | 3.6 | 1.0 | 2.7 | 3.5 | 1.0 | 3.9 | ns | |
| $t_{PHL}$ $R_n$ to $Q_n$, $\overline{Q}_n$ | 1.0 | 3.6 | 1.0 | 2.7 | 3.5 | 1.0 | 3.9 | ns | |
| $t_{PLH}$ Propagation delay | 1.0 | 3.6 | 1.0 | 2.7 | 3.5 | 1.0 | 3.9 | ns | |
| $t_{PHL}$ $S_n$ to $Q_n$, $\overline{Q}_n$ | 1.0 | 3.6 | 1.0 | 2.7 | 3.5 | 1.0 | 3.9 | ns | |
| $t_{PLH}$ Propagation delay | 1.0 | 4.3 | 1.0 | — | 4.0 | 1.0 | 4.1 | ns | |
| $t_{PHL}$ $\overline{CP}$, $\overline{CE}_n$ to $Q_n$, $\overline{Q}_n$ | 1.0 | 4.3 | 1.0 | — | 4.0 | 1.0 | 4.1 | ns | |
| $t_s$ Setup time $D_n$ to $\overline{CP}$, $\overline{CE}_n$ | 2.5 | — | 2.5 | — | — | 2.5 | — | ns | Figs. 7, 8, 9 |
| $t_h$ Hold time $D_n$ to $\overline{CP}$, $\overline{CE}_n$ | 1.5 | — | 1.5 | — | — | 1.5 | — | ns | |
| $t_{TLH}$ Transition time | 1.0 | 3.6 | 1.1 | 2.7 | 3.5 | 1.1 | 3.8 | ns | Figs. 6, 8, 9 |
| $t_{THL}$ 20% to 80%, 80% to 20% | 1.0 | 3.6 | 1.1 | 2.7 | 3.5 | 1.1 | 3.8 | ns | |

## AC WAVEFORMS

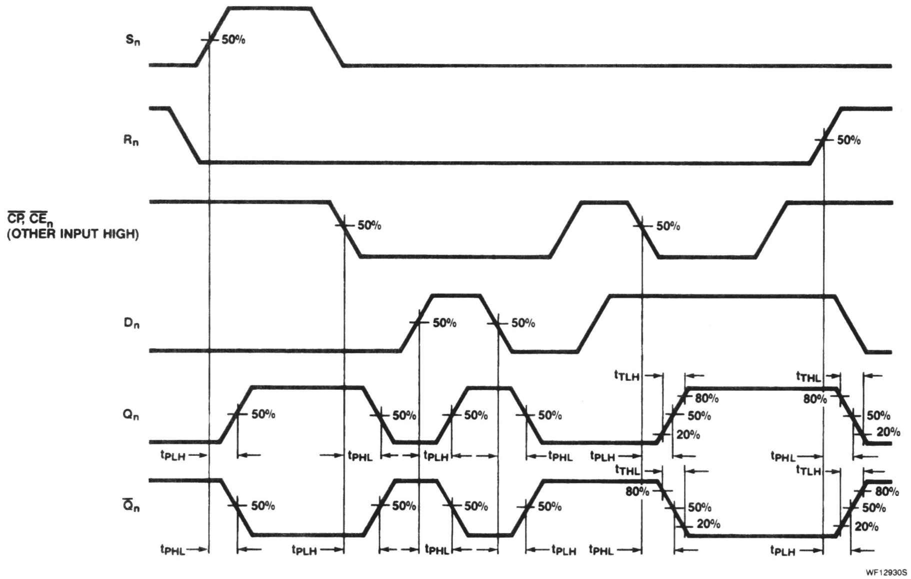

Sn
Rn
CP, CEn
(OTHER INPUT HIGH)
Dn
Qn
Q̄n
50%
80%
20%
tPLH
tPHL
tTLH
tTHL
WF12930S

Figure 6. Propagation Delay and Transition Times

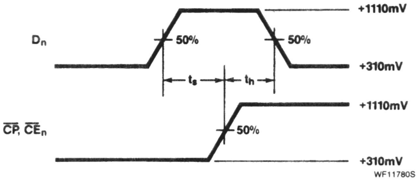
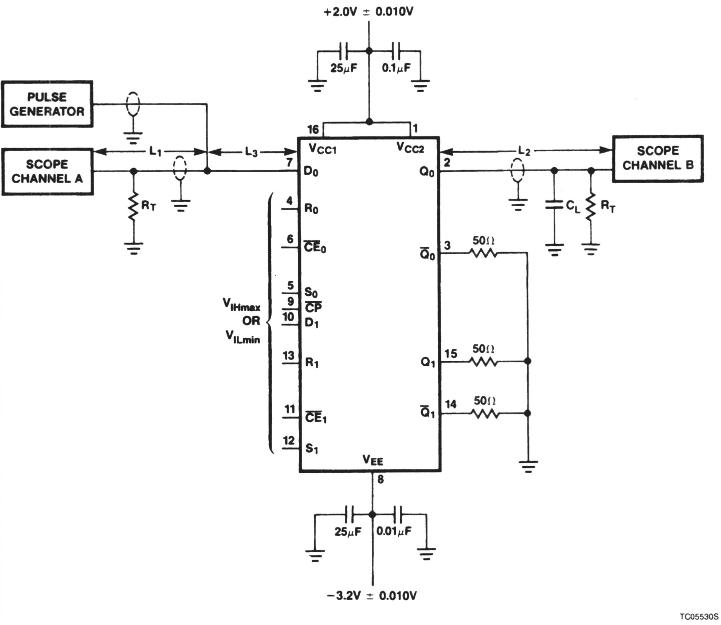

Dn
CP, CEn
50%
ts
th
+1110mV
+310mV
WF11780S

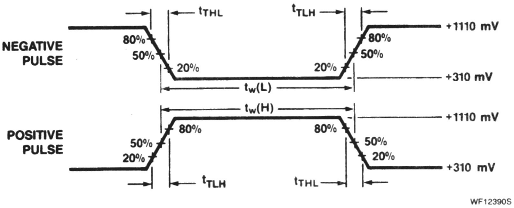
Figure 7. Setup and Hold Times

## TEST CIRCUITS AND WAVEFORMS


+2.0V ± 0.010V
25μF
0.1μF
PULSE GENERATOR
SCOPE CHANNEL A
L1
L3
RT
16
1
VCC1
VCC2
7
D0
Q0
2
L2
SCOPE CHANNEL B
CL
RT
4
R0
6
CE0
3
Q0
50Ω
5
S0
9
CP
10
D1
VIHmax OR VILmin
13
R1
Q1
15
50Ω
11
CE1
Q1
14
50Ω
12
S1
VEE
8
25μF
0.01μF
−3.2V ± 0.010V
TC05530S

**NOTES:**
1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1μF and 25μF from GND to $V_{CC}$, 0.01μF and 25μF from GND to $V_{EE}$ (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than ¼ inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed ¼ inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than ¼ inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance ≤ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed ¼ inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.

**Figure 8. AC Test Circuit for 10130**


tTHL
tTLH
NEGATIVE PULSE
80%
50%
20%
20%
80%
50%
+1110 mV
+310 mV
tw(L)
tw(H)
POSITIVE PULSE
80%
80%
50%
20%
50%
20%
+1110 mV
+310 mV
tTLH
tTHL
WF12390S

**INPUT PULSE REQUIREMENTS**
$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$, $V_T$ = GND (0V)

| Family | Amplitude | Rep Rate | Pulse Width | $t_{TLH}$ | $t_{THL}$ |
|---|---|---|---|---|---|
| 10K ECL | 800mVp-p | 1MHz | 500ns | 2.0 ± 0.2ns | 2.0 ± 0.2ns |

**Figure 9. Input Pulse Definition**

Signetics

# 10131
## Flip-Flop

**Dual D-Type Master-Slave Flip-Flop**
***Product Specification***

**ECL Products**

### DESCRIPTION

The 10131 is a Dual Master-Slave Flip-Flop. Each flip-flop can be clocked separately by holding the common Clock in the LOW state and using the Clock Enable inputs for the clocking function. The output states of the flip-flops register the data present at the $D_n$ inputs on the rising edge of Clock. All unused inputs must be tied LOW to $V_{IL}$ or $V_{EE}$.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 10131 | 3.0ns | 45mA |

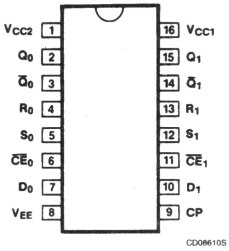
### ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC1} = V_{CC2} = GND$; $V_{EE} = -5.2V$ $T_A = -30°C$ to $+85°C$ |
|---|---|
| Plastic DIP | 10131N |
| Ceramic DIP | 10131F |

### PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_0$, $D_1$ | Data Inputs |
| CP | Clock Input |
| $\overline{CE}_0$, $\overline{CE}_1$ | Clock Enable Inputs |
| $S_0$, $S_1$ | Set Inputs |
| $R_0$, $R_1$ | Reset Inputs |
| $Q_0$, $Q_1$, $\overline{Q}_0$, $\overline{Q}_1$ | Data Outputs |

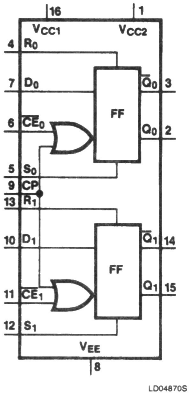
### PIN CONFIGURATION



$V_{CC2}$ 1
$Q_0$ 2
$\overline{Q}_0$ 3
$R_0$ 4
$S_0$ 5
$\overline{CE}_0$ 6
$D_0$ 7
$V_{EE}$ 8
16 $V_{CC1}$
15 $Q_1$
14 $\overline{Q}_1$
13 $R_1$
12 $S_1$
11 $\overline{CE}_1$
10 $D_1$
9 CP
CD08610S

Figure 1

### LOGIC SYMBOL



16
1
$V_{CC1}$
$V_{CC2}$
4 $R_0$
7 $D_0$
6 $\overline{CE}_0$
5 $S_0$
9 CP
13 $R_1$
10 $D_1$
11 $\overline{CE}_1$
12 $S_1$
FF
FF
$\overline{Q}_0$ 3
$Q_0$ 2
$\overline{Q}_1$ 14
$Q_1$ 15
$V_{EE}$
8
LD04870S

Figure 2

# Flip-Flop 10131

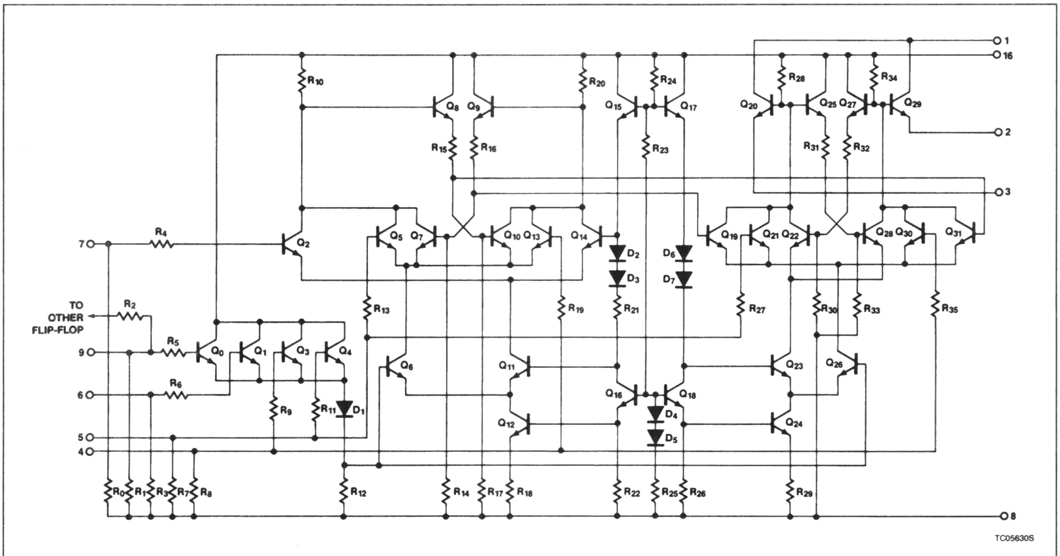

1
16
2
3
7
9
6
5
4
8
TO OTHER FLIP-FLOP
R0
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
R17
R18
R19
R20
R21
R22
R23
R24
R25
R26
R27
R28
R29
R30
R31
R32
R33
R34
R35
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
Q16
Q17
Q18
Q19
Q20
Q21
Q22
Q23
Q24
Q25
Q26
Q27
Q28
Q29
Q30
Q31
D1
D2
D3
D4
D5
D6
D7
TC05630S

**Figure 3. Circuit Diagram**

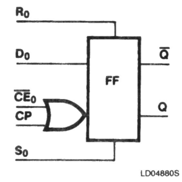

R0
D0
$\overline{CE}_0$
$\overline{CP}$
S0
FF
$\overline{Q}$
Q
LD04880S

**Figure 4. Logic Function (One Flip-flop)**

## FUNCTION TABLES

### SYNCHRONOUS OPERATION

| $D_n$ | CP | $\overline{C}_E$* | $Q_{n+1}$** |
|---|---|---|---|
| L | L | L | $Q_n$ |
| L | L | H | $Q_n$ |
| L | H | L | L |
| L | H | H | $Q_n$ |
| H | L | L | $Q_n$ |
| H | L | H | $Q_n$ |
| H | H | L | H |
| H | H | H | $Q_n$ |

*Conditions for CP and $\overline{CE}$ may be interchanged. In this table $\overline{CE}$ is static, while for CP and H represent a transition from LOW to HIGH between $t_n$ and $t_{n+1}$.
**R and S = LOW.

### ASYNCHRONOUS OPERATION

| R | S | $Q_{n+1}$ |
|---|---|---|
| L | L | $Q_n$ |
| L | H | H |
| H | L | L |
| H | H | N |

Positive Logic:
H = HIGH state (the more positive voltage) = 1
L = LOW state (the less positive voltage) = 0
N = not allowed.

# Flip-Flop 10131

**ABSOLUTE MAXIMUM RATINGS** (Operation beyond the limits set forth in this table may impair useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | | 10K ECL | UNIT |
|---|---|---|---|---|
| $V_{EE}$ | Supply voltage | | -8.0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | | 0 to $V_{EE}$ | V |
| $I_O$ | Output source current | | -50 | mA |
| $T_S$ | Storage temperature | | -55 to +150 | °C |
| $T_J$ | Maximum junction temperature | Ceramic package | +165 | °C |
| | | Plastic package | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | 10K ECL | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | -5.2 | | V |
| $V_{IH}$ | HIGH level input voltage | $T_A$ = -30°C | | | -890 | mV |
| | | $T_A$ = +25°C | | | -810 | mV |
| | | $T_A$ = +85°C | | | -700 | mV |
| $V_{IHT}$ | HIGH level input threshold voltage | $T_A$ = -30°C | -1205 | | | mV |
| | | $T_A$ = +25°C | -1105 | | | mV |
| | | $T_A$ = +85°C | -1035 | | | mV |
| $V_{ILT}$ | LOW level input threshold voltage | $T_A$ = -30°C | | | -1500 | mV |
| | | $T_A$ = +25°C | | | -1475 | mV |
| | | $T_A$ = +85°C | | | -1440 | mV |
| $V_{IL}$ | LOW level input voltage | $T_A$ = -30°C | -1890 | | | mV |
| | | $T_A$ = +25°C | -1850 | | | mV |
| | | $T_A$ = +85°C | -1825 | | | mV |
| $T_A$ | Operating ambient temperature | | -30 | +25 | +85 | °C |

**NOTE:**
When operating at $V_{EE}$ other than specified voltage (-5.2V), the DC and AC Characteristics will vary slightly from specified values.
(See table of DC Characteristics)

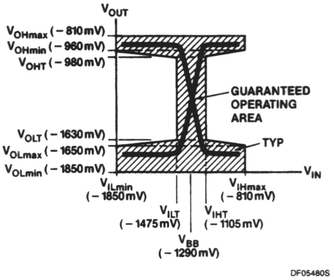
## DC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2}$ = GND, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$, output loading with 50Ω to $-2.0V \pm 0.010V$ unless otherwise specified[1,3]

| PARAMETER | | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | | $T_A = -30°C$ | -1060 | | -890 | mV | For Q outputs, apply $V_{IHmax}$ to $S_n$ inputs with $V_{ILmin}$ applied to all other inputs. For $\overline{Q}$ outputs, apply $V_{IHmax}$ to $R_n$ inputs with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | -960 | | -810 | mV | |
| | | | $T_A = +85°C$ | -890 | | -700 | mV | |
| $V_{OHT}$ | HIGH level output threshold voltage | | $T_A = -30°C$ | -1080 | | | mV | For Q outputs, apply $V_{IHT}$ to $S_n$ inputs with $V_{ILmin}$ applied to all other inputs. For $\overline{Q}$ outputs, apply $V_{IHT}$ to $R_n$ inputs, with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | -980 | | | mV | |
| | | | $T_A = +85°C$ | -910 | | | mV | |
| $V_{OLT}$ | LOW level output threshold voltage | | $T_A = -30°C$ | | | -1655 | mV | For Q outputs, apply $V_{IHT}$ to $R_n$ inputs, with $V_{ILmin}$ applied to all other inputs. For $\overline{Q}$ outputs, apply $V_{IHT}$ to $S_n$ inputs with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | | | -1630 | mV | |
| | | | $T_A = +85°C$ | | | -1595 | mV | |
| $V_{OL}$ | LOW level output voltage | | $T_A = -30°C$ | -1890 | | -1675 | mV | For Q outputs, apply $V_{IHmax}$ to $R_n$ inputs with $V_{ILmin}$ applied to all other inputs. For $\overline{Q}$ outputs, apply $V_{IHmax}$ to $S_n$ inputs with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | -1850 | | -1650 | mV | |
| | | | $T_A = +85°C$ | -1825 | | -1615 | mV | |
| $I_{IH}$ | HIGH level input current | CP input | $T_A = -30°C$ | | | 425 | μA | Apply $V_{IHmax}$ to CP input with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | | | 265 | μA | |
| | | | $T_A = +85°C$ | | | 265 | μA | |
| | | $\overline{CE}_0$, $\overline{CE}_1$ inputs | $T_A = -30°C$ | | | 350 | μA | Apply $V_{IHmax}$ to each input under test, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | | | 220 | μA | |
| | | | $T_A = +85°C$ | | | 220 | μA | |
| | | $D_0$, $D_1$ inputs | $T_A = -30°C$ | | | 390 | μA | |
| | | | $T_A = +25°C$ | | | 245 | μA | |
| | | | $T_A = +85°C$ | | | 245 | μA | |
| | | $R_n$ inputs | $T_A = -30°C$ | | | 525 | μA | For $R_n$ inputs, apply $V_{IHmax}$ to $D_n$ inputs and to $R_n$ input under test with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | | | 330 | μA | |
| | | | $T_A = +85°C$ | | | 330 | μA | |
| | | $S_n$ inputs | $T_A = -30°C$ | | | 525 | μA | For $S_n$ inputs, apply $V_{IHmax}$ to $D_n$ inputs and $S_n$ input under test with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | | | 330 | μA | |
| | | | $T_A = +85°C$ | | | 330 | μA | |
| $I_{IL}$ | LOW level input current | | $T_A = -30°C$ | 0.5 | | | μA | Apply $V_{ILmin}$ to each input under test, one at a time, with $V_{IHmax}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | 0.5 | | | μA | |
| | | | $T_A = +85°C$ | 0.3 | | | μA | |
| $-I_{EE}$ | $V_{EE}$ supply current | | $T_A = -30°C$ | | | 62 | mA | |
| | | | $T_A = +25°C$ | | 45 | 56 | mA | |
| | | | $T_A = +85°C$ | | | 62 | mA | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | | $T_A = +25°C$ | | 0.016 | | V/V | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | | 0.250 | | V/V | |
| $\frac{\Delta V_{BB}}{\Delta V_{EE}}$ | Reference bias voltage compensation | | | | 0.148 | | V/V | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst-case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 5.

## Flip-Flop 10131



**NOTES:**

| | |
|---|---|
| $V_{IHmax}$ | – Maximum HIGH level input voltage (the most positive $V_{IH}$). |
| $V_{IHT}$ | – HIGH level input threshold voltage. |
| $V_{ILT}$ | – LOW level input threshold voltage. |
| $V_{ILmin}$ | – Minimum LOW level input voltage (the most negative $V_{IL}$). |
| $V_{OHmax}$ | – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition. |
| $V_{OHmin}$ | – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition. |
| $V_{OHT}$ | – HIGH level output threshold voltage with the inputs set to their respective threshold levels. |
| $V_{OLT}$ | – LOW level output threshold voltage with the inputs set to their respective threshold levels. |
| $V_{OLmax}$ | – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions. |
| $V_{OLmin}$ | – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions. |
| $V_{BB}$ | – Reference bias voltage (the internally generated reference voltage which is used to set the input and output threshold level). |

**Figure 5. Transfer Characteristics**

## AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$

| PARAMETER | $T_A = -30°C$ | | $T_A = +25°C$ | | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Typ | Max | Min | Max | | |
| $f_{MAX}$ Maximum clock frequency | 125 | | 125 | 160 | | 125 | | MHz | Figs. 6, 8, 10 |
| $t_{PLH}$ Propagation delay | 1.7 | 4.6 | 1.8 | 3.0 | 4.5 | 1.8 | 5.0 | ns | Figs. 6, 9, 10 |
| $t_{PHL}$ $D_n$ to $Q_n$, $\overline{Q}_n$ | 1.7 | 4.6 | 1.8 | 3.0 | 4.5 | 1.8 | 5.0 | ns | |
| $t_{PLH}$ Propagation delay | 1.7 | 4.4 | 1.8 | 2.8 | 4.3 | 1.8 | 4.8 | ns | |
| $t_{PHL}$ $R_n$ to $Q_n$, $\overline{Q}_n$ | 1.7 | 4.4 | 1.8 | 2.8 | 4.3 | 1.8 | 4.8 | ns | |
| $t_{PLH}$ Propagation delay | 1.7 | 4.4 | 1.8 | 2.8 | 4.3 | 1.8 | 4.8 | ns | |
| $t_{PHL}$ $S_n$ to $Q_n$, $\overline{Q}_n$ | 1.7 | 4.4 | 1.8 | 2.8 | 4.3 | 1.8 | 4.8 | ns | |
| $t_s$ Setup time $D_n$ to CP | 2.5 | | 2.5 | | | 2.5 | | ns | Figs. 7, 9, 10 |
| $t_h$ Hold time $D_n$ to CP | 1.5 | | 1.5 | | | 1.5 | | ns | |
| $t_{TLH}$ Transition time | 1.0 | 4.6 | 1.1 | 2.5 | 4.5 | 1.1 | 4.9 | ns | Figs. 6, 9, 10 |
| $t_{THL}$ 20% to 80%, 80% to 20% | 1.0 | 4.6 | 1.1 | 2.5 | 4.5 | 1.1 | 4.9 | ns | |

## AC WAVEFORMS

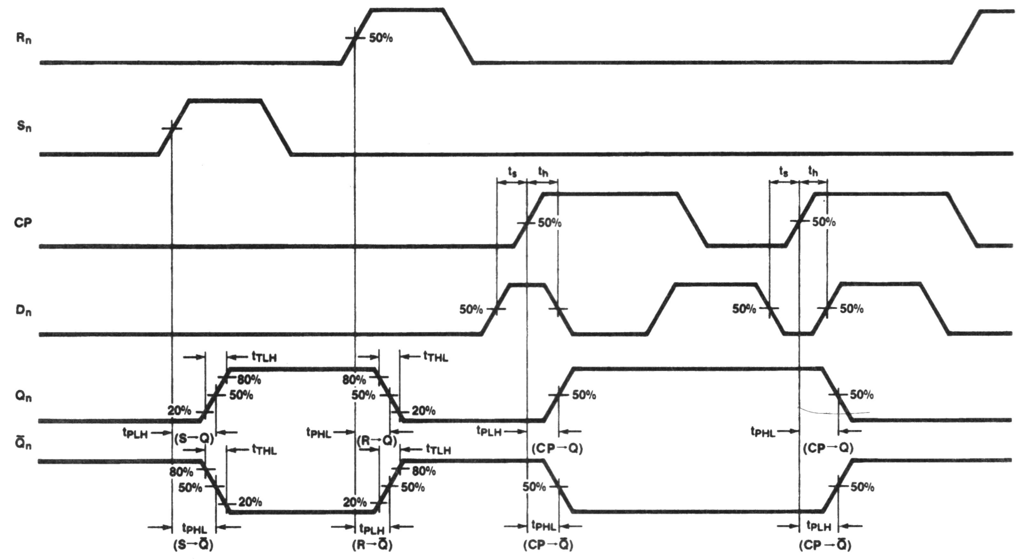

Rn
50%
Sn
CP
ts
th
50%
ts
th
50%
Dn
50%
50%
50%
Qn
tTLH
tTHL
80%
50%
20%
80%
50%
20%
50%
50%
tPLH
(S→Q)
tPHL
(R→Q)
tPLH
(CP→Q)
tPHL
(CP→Q)
Q̄n
tTHL
tTLH
80%
50%
20%
20%
80%
50%
50%
50%
tPHL
(S→Q̄)
tPLH
(R→Q̄)
tPHL
(CP→Q̄)
tPLH
(CP→Q̄)
WF12981S

Figure 6. Propagation Delay and Transition Times

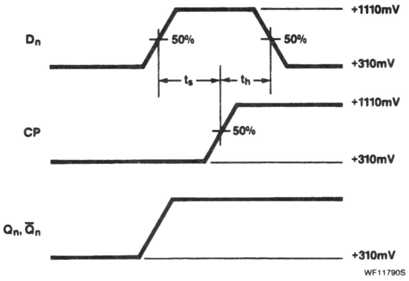
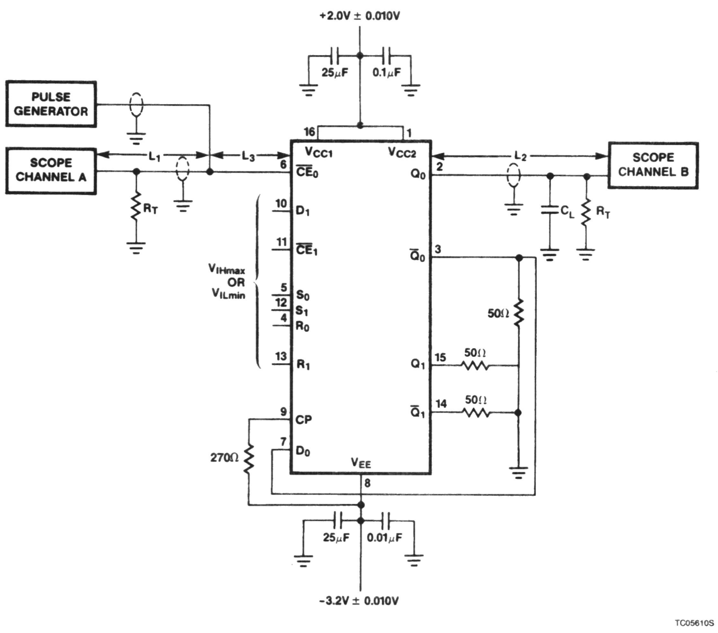

Dn
50%
50%
+1110mV
+310mV
ts
th
CP
50%
+1110mV
+310mV
Qn, Q̄n
+310mV
WF11790S

Figure 7. Setup and Hold Times

## TEST CIRCUITS AND WAVEFORMS


+2.0V ± 0.010V
25μF
0.1μF
PULSE GENERATOR
SCOPE CHANNEL A
L1
L3
RT
16
1
6
VCC1
VCC2
CE0
Q0
2
L2
SCOPE CHANNEL B
CL
RT
10
D1
11
CE1
Q0
3
VIHmax OR VILmin
5
S0
12
S1
4
R0
13
R1
50Ω
Q1
15
50Ω
Q1
14
50Ω
9
CP
7
D0
270Ω
VEE
8
25μF
0.01μF
-3.2V ± 0.010V
TC05610S

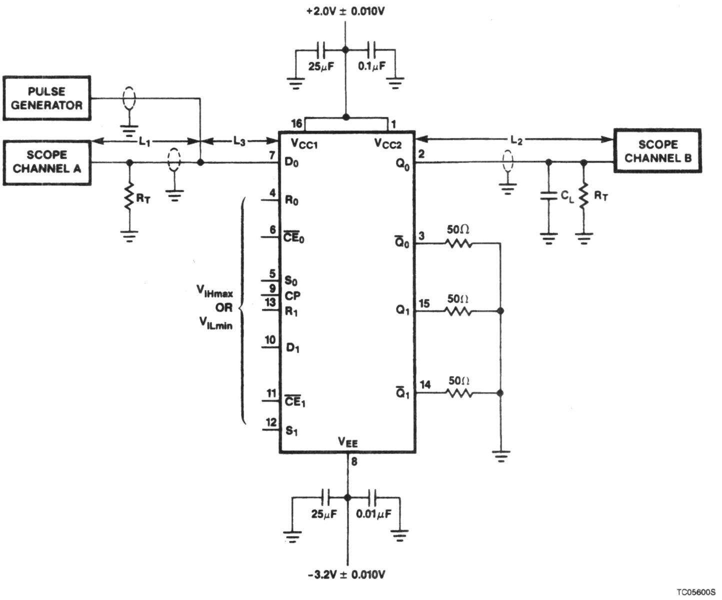
**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V$ ±0.010V, $V_{EE} = -3.2V$ ±0.010V.
2. Decoupling 0.1μF and 25μF from GND to $V_{CC}$, 0.01μF and 25μF from GND to $V_{EE}$. (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance $\leqslant$ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ±1% or better.

Figure 8. AC Test Circuit (Clock Frequency)

## Flip-Flop

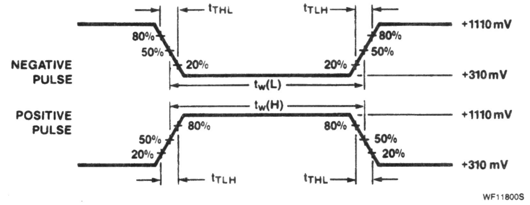
## 10131


+2.0V ± 0.010V
25µF
0.1µF
PULSE GENERATOR
SCOPE CHANNEL A
L1
L3
RT
16
1
VCC1
VCC2
7
D0
2
Q0
L2
SCOPE CHANNEL B
CL
RT
4
R0
6
CE0
3
Q0
50Ω
5
S0
9
CP
13
R1
15
Q1
50Ω
VIHmax OR VILmin
10
D1
11
CE1
14
Q1
50Ω
12
S1
VEE
8
25µF
0.01µF
-3.2V ± 0.010V
TC05600S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1µF and 25µF from GND to $V_{CC}$, 0.01µF and 25µF from GND to $V_{EE}$. (0.01 and 0.1µF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance $\leq$ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.

Figure 9. AC Test Circuit


NEGATIVE PULSE
POSITIVE PULSE
tTHL
tTLH
80%
50%
20%
tw(L)
tw(H)
+1110 mV
+310 mV
+1110 mV
+310 mV
tTLH
tTHL
WF11800S

| INPUT PULSE REQUIREMENTS<br>$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$, $V_T$ = GND (0V) | | | | | |
|---|---|---|---|---|---|
| **Family** | **Amplitude** | **Rep Rate** | **Pulse Width** | **$t_{TLH}$** | **$t_{THL}$** |
| 10K ECL | 800mVp-p | 1MHz | 500ns | 2.0 ± 0.2ns | 2.0 ± 0.2ns |

Figure 10. Input Pulse Definition

**Signetics**

# 10132
## Multiplexer/Latch

**Dual 2-Input Multiplexer With Clocked D-Type Latches and Common Reset**
***Product Specification***

**ECL Products**

## DESCRIPTION

The 10132 is a Dual 2-Input Multiplexer with Clocked D-type Latches and a Common Reset. Latch can be clocked by the common Clock (CP) when the Clock Enable input ($\overline{CE}$) is LOW or by the Clock Enable input when the common Clock is held in the LOW state. The outputs are latched by the positive transition of the Clock. Any change at the data input will be registered at the output only if the Clock is LOW.

Data inputs are selected by a common data Select (S). All unused inputs must be tied LOW to $V_{IL}$ or $V_{EE}$.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 10132 | 3.0ns | 44mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} =$ GND; $V_{EE} = -5.2V$<br>$T_A = -30°C$ to $+85°C$ |
|---|---|
| Plastic DIP | 10132N |
| Ceramic DIP | 10132F |

## PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_0 - D_3$ | Data Inputs |
| CP | Clock Input |
| $\overline{CE}_0$, $\overline{CE}_1$ | Clock Enable Inputs |
| S | Data Select Input |
| R | Reset Inputs |
| $Q_n$, $\overline{Q}_n$ | Data Outputs |

## PIN CONFIGURATION

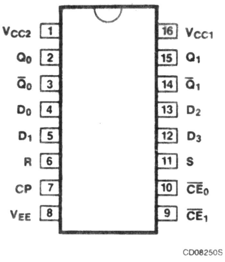

$V_{CC2}$ 1
$Q_0$ 2
$\overline{Q}_0$ 3
$D_0$ 4
$D_1$ 5
R 6
CP 7
$V_{EE}$ 8
16 $V_{CC1}$
15 $Q_1$
14 $\overline{Q}_1$
13 $D_2$
12 $D_3$
11 S
10 $\overline{CE}_0$
9 $\overline{CE}_1$
CD08250S

Figure 1

## LOGIC SYMBOL

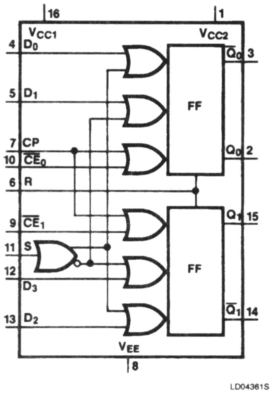

16
1
$V_{CC1}$
$V_{CC2}$
4 $D_0$
$\overline{Q}_0$ 3
5 $D_1$
FF
7 CP
10 $\overline{CE}_0$
$Q_0$ 2
6 R
$Q_1$ 15
9 $\overline{CE}_1$
11 S
12 $D_3$
FF
13 $D_2$
$\overline{Q}_1$ 14
$V_{EE}$
8
LD04361S

Figure 2

# Multiplexer/Latch **10132**

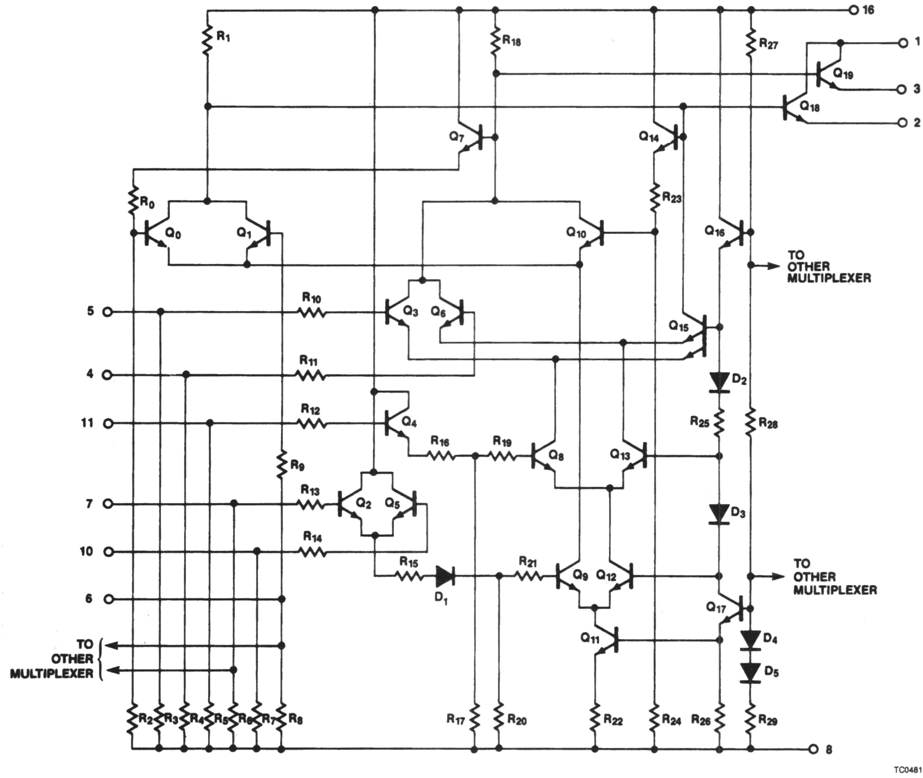

16
1
3
2
5
4
11
7
10
6
8
TO OTHER MULTIPLEXER
TO OTHER MULTIPLEXER
TO OTHER MULTIPLEXER
R1
R18
R27
Q19
Q18
Q7
Q14
R23
R0
Q0
Q1
Q10
Q16
R10
Q3
Q6
Q15
R11
D2
R12
Q4
R25
R28
R16
R19
Q8
Q13
R9
R13
Q2
Q5
D3
R14
R15
D1
R21
Q9
Q12
Q17
Q11
D4
D5
R2
R3
R4
R5
R6
R7
R8
R17
R20
R22
R24
R26
R29
TC04810S

Figure 3. Circuit Diagram (One Multiplexer)

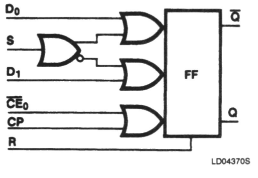

D0
S
D1
$\overline{CE}_0$
CP
R
FF
$\overline{Q}$
Q
LD04370S

Figure 4. Logic Diagram

## FUNCTION TABLE

| R | S | CP* | $\overline{C}_E$* | $Q_{n+1}$ |
|---|---|---|---|---|
| L | L | L | L | $D_0$ |
| L | L | L | H | $Q_n$ |
| L | L | H | L | $Q_n$ |
| L | L | H | H | $Q_n$ |
| L | H | L | L | $D_1$ |
| L | H | L | H | $Q_n$ |
| L | H | H | L | $Q_n$ |
| L | H | H | H | $Q_n$ |
| H | X | X | H | L |
| H | X | H | X | L |
| H | X | L | L | $Q_n$ |

*Conditions for C and $\overline{CE}$ may be interchanged as indicated in the truth table.

## ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | | 10K ECL | UNIT |
|---|---|---|---|---|
| $V_{EE}$ | Supply voltage | | −8.0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | | 0 to $V_{EE}$ | V |
| $I_O$ | Output source current | | −50 | mA |
| $T_S$ | Storage temperature | | −55 to +150 | °C |
| $T_J$ | Maximum junction temperature | Ceramic package | +165 | °C |
| | | Plastic package | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | 10K ECL | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | −5.2 | | V |
| $V_{IH}$ | HIGH level input voltage | $T_A$ = −30°C | | | −890 | mV |
| | | $T_A$ = +25°C | | | −810 | mV |
| | | $T_A$ = +85°C | | | −700 | mV |
| $V_{IHT}$ | HIGH level input threshold voltage | $T_A$ = −30°C | −1205 | | | mV |
| | | $T_A$ = +25°C | −1105 | | | mV |
| | | $T_A$ = +85°C | −1035 | | | mV |
| $V_{ILT}$ | LOW level input threshold voltage | $T_A$ = −30°C | | | −1500 | mV |
| | | $T_A$ = +25°C | | | −1475 | mV |
| | | $T_A$ = +85°C | | | −1440 | mV |
| $V_{IL}$ | LOW level input voltage | $T_A$ = −30°C | −1890 | | | mV |
| | | $T_A$ = +25°C | −1850 | | | mV |
| | | $T_A$ = +85°C | −1825 | | | mV |
| $T_A$ | Operating ambient temperature | | −30 | +25 | +85 | °C |

**NOTE:**

When operating at $V_{EE}$ other than specified voltage (−5.2V), the DC and AC Characteristics will vary slightly from specified values. (See table of DC Characteristics)

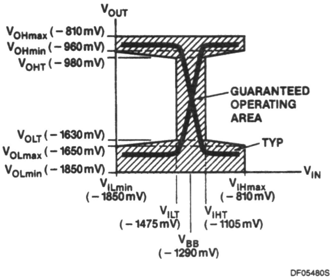
## Multiplexer/Latch 10132

**DC ELECTRICAL CHARACTERISTICS** $V_{CC1} = V_{CC2}$ = GND, $V_{EE}$ = −5.2V ±0.010V, $T_A$ = −30°C to +85°C, output loading with 50Ω to −2.0V ±0.010V unless otherwise specified[1,3]

| PARAMETER | | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | | $T_A$ = −30°C | −1060 | | −890 | mV | For Q outputs, apply $V_{IHmax}$ to $D_0$ input with $V_{ILmin}$ applied to all other inputs.<br>For $\overline{Q}$ outputs, apply $V_{ILmin}$ to all inputs. |
| | | | $T_A$ = +25°C | −960 | | −810 | mV | |
| | | | $T_A$ = +85°C | −890 | | −700 | mV | |
| $V_{OHT}$ | HIGH level output threshold voltage | | $T_A$ = −30°C | −1080 | | | mV | For Q outputs, apply $V_{IHT}$ to $D_0$ input with $V_{ILmin}$ applied to all other inputs.<br>For $\overline{Q}$ outputs, apply $V_{ILT}$ to $D_0$ input with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A$ = +25°C | −980 | | | mV | |
| | | | $T_A$ = +85°C | −910 | | | mV | |
| $V_{OLT}$ | LOW level output threshold voltage | | $T_A$ = −30°C | | | −1655 | mV | For Q outputs, apply $V_{ILT}$ to $D_0$ input with $V_{ILmin}$ applied to all other inputs.<br>For $\overline{Q}$ outputs, apply $V_{IHT}$ to $D_0$ input with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A$ = +25°C | | | −1630 | mV | |
| | | | $T_A$ = +85°C | | | −1595 | mV | |
| $V_{OL}$ | LOW level output voltage | | $T_A$ = −30°C | −1890 | | −1675 | mV | For Q outputs, apply $V_{ILmin}$ to all inputs.<br>For $\overline{Q}$ outputs, apply $V_{IHmax}$ to $D_0$ input with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A$ = +25°C | −1850 | | −1650 | mV | |
| | | | $T_A$ = +85°C | −1825 | | −1615 | mV | |
| $I_{IH}$ | HIGH level input current | $D_n$ inputs | $T_A$ = −30°C | | | 460 | μA | Apply $V_{IHmax}$ to $D_0$ input with $V_{ILmin}$ applied to all other inputs.<br>Apply $V_{IHmax}$ to $D_1$ input and S input with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A$ = +25°C | | | 290 | μA | |
| | | | $T_A$ = +85°C | | | 290 | μA | |
| | | R input | $T_A$ = −30°C | | | 620 | μA | Apply $V_{IHmax}$ to CP and R inputs with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A$ = +25°C | | | 390 | μA | |
| | | | $T_A$ = +85°C | | | 390 | μA | |
| | | CP input | $T_A$ = −30°C | | | 460 | μA | Apply $V_{IHmax}$ to CP input with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A$ = +25°C | | | 290 | μA | |
| | | | $T_A$ = +85°C | | | 290 | μA | |
| | | S, $\overline{CE}_n$ inputs | $T_A$ = −30°C | | | 425 | μA | Apply $V_{IHmax}$ to S or $\overline{CE}_n$ input under test, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A$ = +25°C | | | 265 | μA | |
| | | | $T_A$ = +85°C | | | 265 | μA | |
| $I_{IL}$ | LOW level input current | | $T_A$ = −30°C | 0.5 | | | μA | Apply $V_{ILmin}$ to each input under test, one at a time, with $V_{IHmax}$ applied to all other inputs. |
| | | | $T_A$ = +25°C | 0.5 | | | μA | |
| | | | $T_A$ = +85°C | 0.3 | | | μA | |
| $-I_{EE}$ | $V_{EE}$ supply current | | $T_A$ = −30°C | | | 60 | mA | |
| | | | $T_A$ = +25°C | | 44 | 55 | mA | |
| | | | $T_A$ = +85°C | | | 60 | mA | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | | $T_A$ = +25°C | | 0.016 | | V/V | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | | 0.250 | | V/V | |
| $\frac{\Delta V_{BB}}{\Delta V_{EE}}$ | Reference bias voltage compensation | | | | 0.148 | | V/V | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst-case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 5.



**NOTES:**

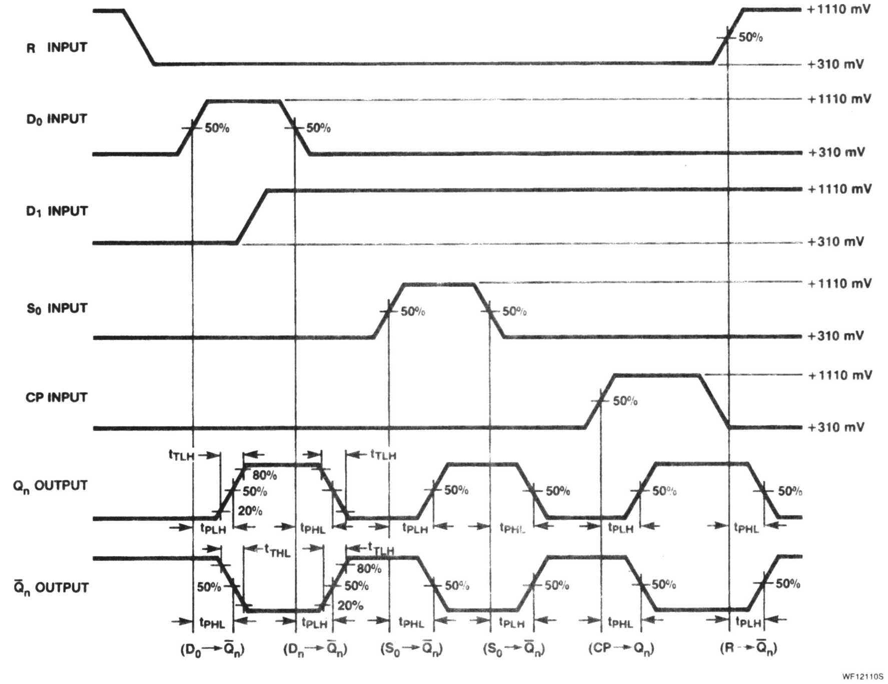
| | |
|---|---|
| $V_{IHmax}$ | – Maximum HIGH level input voltage (the most positive $V_{IH}$). |
| $V_{IHT}$ | – HIGH level input threshold voltage. |
| $V_{ILT}$ | – LOW level input threshold voltage. |
| $V_{ILmin}$ | – Minimum LOW level input voltage (the most negative $V_{IL}$). |
| $V_{OHmax}$ | – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition. |
| $V_{OHmin}$ | – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition. |
| $V_{OHT}$ | – HIGH level output threshold voltage with the inputs set to their respective threshold levels. |
| $V_{OLT}$ | – LOW level output threshold voltage with the inputs set to their respective threshold levels. |
| $V_{OLmax}$ | – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions. |
| $V_{OLmin}$ | – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions. |
| $V_{BB}$ | – Reference bias voltage. The internally generated reference voltage which is used to set the input and output threshold level. |

**Figure 5. Transfer Characteristics**

## AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$

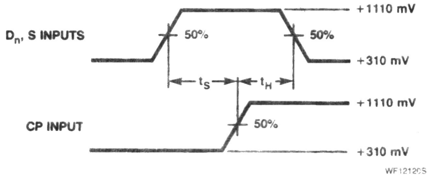
| PARAMETER | | $T_A = -30°C$ | | $T_A = +25°C$ | | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Typ | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 1.0 | 3.6 | 1.0 | 3.0 | 3.3 | 1.0 | 3.7 | ns | Figs. 6, 7, 8 |
| $t_{PHL}$ | $D_n$ to $Q_n$, $\overline{Q}_n$ | 1.0 | 3.6 | 1.0 | 3.0 | 3.3 | 1.0 | 3.7 | ns | |
| $t_{PLH}$ | Propagation delay | 1.0 | 4.0 | 1.0 | | 3.8 | 1.0 | 4.2 | ns | |
| $t_{PHL}$ | R to $Q_n$, $\overline{Q}_n$ | 1.0 | 4.0 | 1.0 | | 3.8 | 1.0 | 4.2 | ns | |
| $t_{PLH}$ | Propagation delay | 1.0 | 6.0 | 1.0 | | 5.7 | 1.0 | 6.3 | ns | |
| $t_{PHL}$ | CP to $Q_n$, $\overline{Q}_n$ | 1.0 | 6.0 | 1.0 | | 5.7 | 1.0 | 6.3 | ns | |
| $t_{PLH}$ | Propagation delay | 1.0 | 4.8 | 1.0 | | 4.6 | 1.0 | 5.0 | ns | |
| $t_{PHL}$ | S to $Q_n$, $\overline{Q}_n$ | 1.0 | 4.8 | 1.0 | | 4.6 | 1.0 | 5.0 | ns | |
| $t_s$ | Setup time $D_n$ to CP | 2.5 | | 2.5 | | | 2.5 | | ns | |
| $t_h$ | Hold time $D_n$ to CP | 1.5 | | 1.5 | | | 1.5 | | ns | |
| $t_s$ | Setup time S to CP | 3.5 | | 3.5 | | | 3.5 | | ns | |
| $t_h$ | Hold time S to CP | 1.0 | | 1.0 | | | 1.0 | | ns | |
| $t_{TLH}$ | Transition time | 1.5 | 3.7 | 1.5 | | 3.5 | 1.5 | 3.8 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 1.5 | 3.7 | 1.5 | | 3.5 | 1.5 | 3.8 | ns | |

## AC WAVEFORMS


R INPUT
D0 INPUT
D1 INPUT
S0 INPUT
CP INPUT
Qn OUTPUT
Q̄n OUTPUT
+1110 mV
+310 mV
50%
80%
20%
tTLH
tTHL
tPLH
tPHL
(D0 → Q̄n)
(Dn → Q̄n)
(S0 → Q̄n)
(S0 → Q̄n)
(CP → Qn)
(R → Q̄n)
WF12110S

**NOTES:**
1. Any change on the data input will be registered at the output only if the clock is LOW.
2. Outputs are latched on the positive transition of the clock.
3. The reset inputs is enabled when the clock is HIGH.

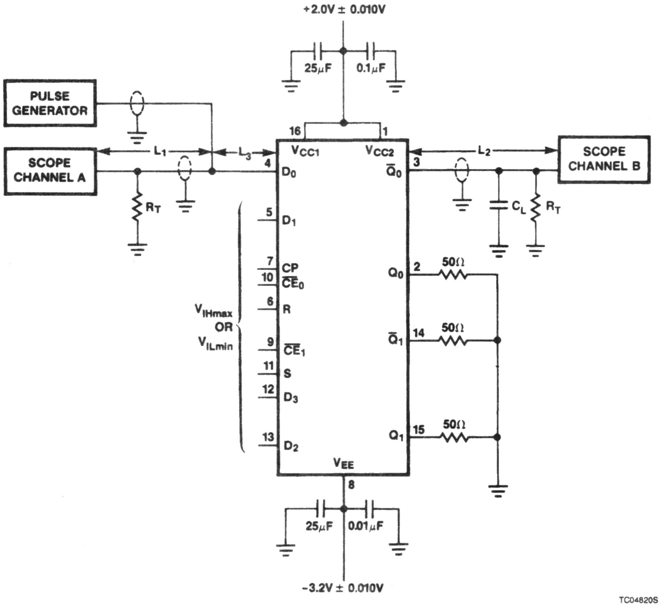
Figure 6. Propagation Delay and Transition Times


Dn, S INPUTS
CP INPUT
+1110 mV
+310 mV
50%
tS
tH
WF12120S

**NOTES:**
1. Any change on the data input will be registered at the output only if the clock is LOW.
2. Outputs are latched on the positive transition of the clock.
3. The reset inputs is enabled when the clock is HIGH.

Figure 7. Setup and Hold Times

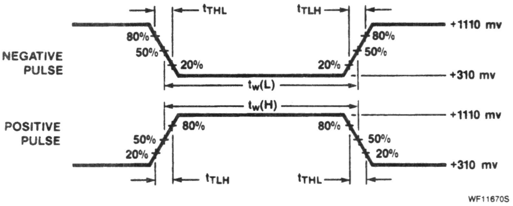
## TEST CIRCUITS AND WAVEFORMS


+2.0V ± 0.010V
25µF
0.1µF
PULSE GENERATOR
SCOPE CHANNEL A
L1
L3
RT
16
1
VCC1
VCC2
4
D0
3
Q̄0
L2
SCOPE CHANNEL B
CL
RT
5
D1
7
CP
10
CE̅0
6
R
9
CE̅1
11
S
12
D3
13
D2
VIHmax
OR
VILmin
Q0
2
50Ω
Q̄1
14
50Ω
Q1
15
50Ω
VEE
8
25µF
0.01µF
-3.2V ± 0.010V
TC04820S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1µF and 25µF from GND to $V_{CC}$, 0.01µF and 25µF from GND to $V_{EE}$ (0.01 and 0.1µF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than ¼ inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed ¼ inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than ¼ inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance ≤ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed ¼ inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.

**Figure 8. Test Circuit**


NEGATIVE PULSE
POSITIVE PULSE
tTHL
tTLH
80%
50%
20%
tw(L)
tw(H)
+1110 mv
+310 mv
WF11670S

| INPUT PULSE REQUIREMENTS<br>$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$, $V_T$ = GND (0V) | | | | | |
|---|---|---|---|---|---|
| **Family** | **Amplitude** | **Rep Rate** | **Pulse Width** | $t_{TLH}$ | $t_{THL}$ |
| 10K ECL | 800mVp-p | 1MHz | 500ns | 2.0 ± 0.2ns | 2.0 ± 0.2ns |

**Figure 9. Input Pulse Definition**

**Signetics**

# 10133
## Latch

**Quad Latch With D-Type Inputs and Enable Outputs**
***Product Specification***

**ECL Products**

## DESCRIPTION

The 10133 is a Quad Latch with D-Type Inputs and Enable Outputs. Data ($D_n$) inputs are registered at output while the clock is HIGH. Data inputs are latched by the negative transition of the clock. All unused inputs must be tied LOW to $V_{IL}$ or $V_{EE}$.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 10133 | 4.0ns | 59.6mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} = \text{GND}$; $V_{EE} = -5.2V$<br>$T_A = -30°C$ to $+85°C$ |
|---|---|
| Plastic DIP | 10133N |
| Ceramic DIP | 10133F |

## PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_0 - D_3$ | Data Inputs |
| $\overline{CP}$ | Clock Input |
| $\overline{CE}_0$, $\overline{CE}_1$ | Clock Enable Inputs |
| $\overline{OE}_0$, $\overline{OE}_1$ | Output Enable Inputs |
| $\overline{Q}_0 - \overline{Q}_3$ | Data Outputs |

## PIN CONFIGURATION

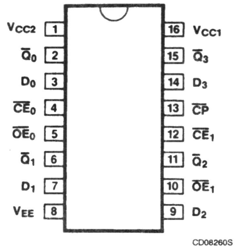

$V_{CC2}$ 1
$\overline{Q}_0$ 2
$D_0$ 3
$\overline{CE}_0$ 4
$\overline{OE}_0$ 5
$\overline{Q}_1$ 6
$D_1$ 7
$V_{EE}$ 8
16 $V_{CC1}$
15 $\overline{Q}_3$
14 $D_3$
13 $\overline{CP}$
12 $\overline{CE}_1$
11 $\overline{Q}_2$
10 $\overline{OE}_1$
9 $D_2$
CD08260S

**Figure 1**

## LOGIC SYMBOL

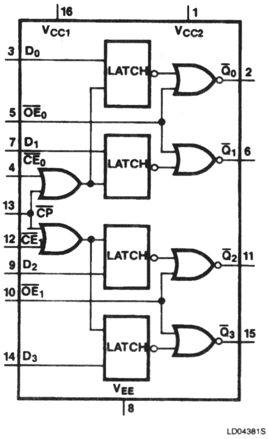

16
$V_{CC1}$
1
$V_{CC2}$
3 $D_0$
LATCH
$\overline{Q}_0$ 2
5 $\overline{OE}_0$
7 $D_1$
4 $\overline{CE}_0$
LATCH
$\overline{Q}_1$ 6
13 $\overline{CP}$
12 $\overline{CE}_1$
LATCH
9 $D_2$
$\overline{Q}_2$ 11
10 $\overline{OE}_1$
LATCH
$\overline{Q}_3$ 15
14 $D_3$
$V_{EE}$
8
LD04381S

**Figure 2**

# Latch 10133

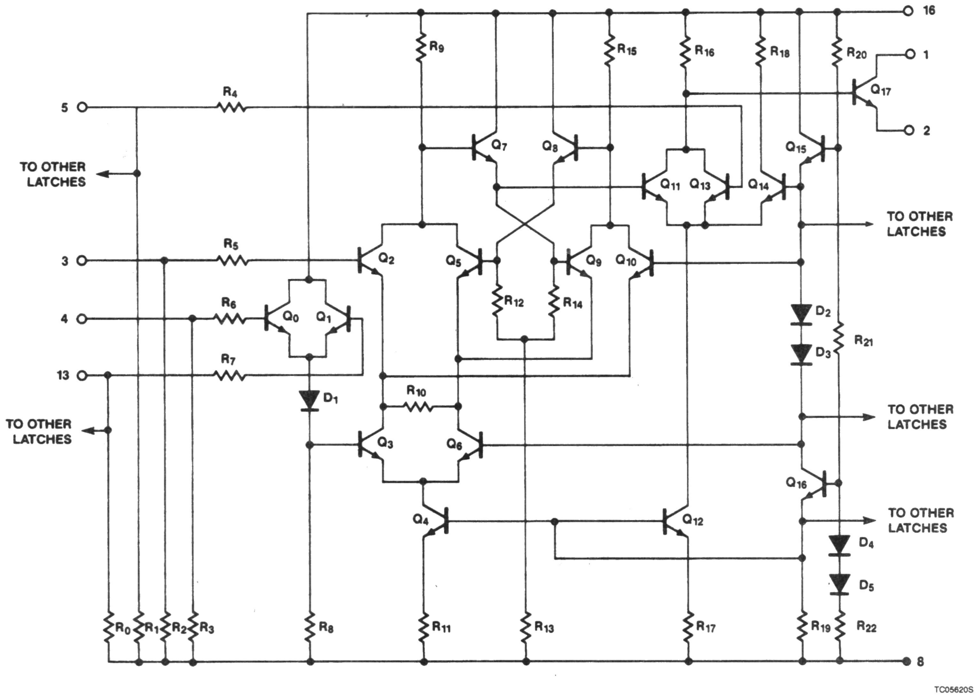

16
1
2
5
3
4
13
8
R0
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
R17
R18
R19
R20
R21
R22
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
Q16
Q17
D1
D2
D3
D4
D5
TO OTHER LATCHES
TO OTHER LATCHES
TO OTHER LATCHES
TO OTHER LATCHES
TO OTHER LATCHES
TC05620S

Figure 3. Circuit Diagram (One Latch)

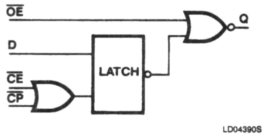

OE
D
CE
CP
LATCH
Q
LD04390S

Figure 4. Logic Diagram

## FUNCTION TABLE

| $\overline{OE}$ | $\overline{CP}$ | $\overline{CE}$ | D | $\overline{Q}_{n+1}$ |
|---|---|---|---|---|
| H | X | X | X | L |
| L | L | L | X | $\overline{Q}_n$ |
| L | L | H | L | L |
| L | H | L | L | L |
| L | H | H | L | L |
| L | L | H | H | H |
| L | H | L | H | H |
| L | H | H | H | H |

Positive Logic:
H = HIGH state (the more positive voltage) = 1
L = LOW state (the less postive voltage) = 0
X = Don't Care

# Latch

# 10133

**ABSOLUTE MAXIMUM RATINGS** (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | | 10K ECL | UNIT |
|---|---|---|---|---|
| $V_{EE}$ | Supply voltage | | −8.0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | | 0 to $V_{EE}$ | V |
| $I_O$ | Output source current | | −50 | mA |
| $T_S$ | Storage temperature | | −55 to +150 | °C |
| $T_J$ | Maximum junction temperature | Ceramic package | +165 | °C |
| | | Plastic package | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | 10K ECL | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | −5.2 | | V |
| $V_{IH}$ | HIGH level input voltage | $T_A$ = −30°C | | | −890 | mV |
| | | $T_A$ = +25°C | | | −810 | mV |
| | | $T_A$ = +85°C | | | −700 | mV |
| $V_{IHT}$ | HIGH level input threshold voltage | $T_A$ = −30°C | −1205 | | | mV |
| | | $T_A$ = +25°C | −1105 | | | mV |
| | | $T_A$ = +85°C | −1035 | | | mV |
| $V_{ILT}$ | LOW level input threshold voltage | $T_A$ = −30°C | | | −1500 | mV |
| | | $T_A$ = +25°C | | | −1475 | mV |
| | | $T_A$ = +85°C | | | −1440 | mV |
| $V_{IL}$ | LOW level input voltage | $T_A$ = −30°C | −1890 | | | mV |
| | | $T_A$ = +25°C | −1850 | | | mV |
| | | $T_A$ = +85°C | −1825 | | | mV |
| $T_A$ | Operating ambient temperature | | −30 | +25 | +85 | °C |

**NOTE:**
When operating at $V_{EE}$ other than specified voltage (−5.2V), the DC and AC Characteristics will vary slightly from specified values. (See table of DC Characteristics)

## Latch

## 10133

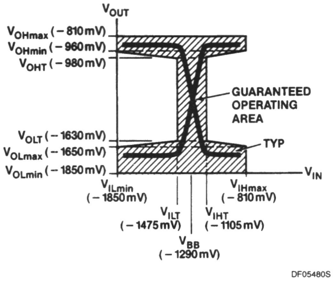
**DC ELECTRICAL CHARACTERISTICS** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$, output loading with 50Ω to −2.0V ±0.010V unless otherwise specified[1,3]

| PARAMETER | | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | | $T_A = -30°C$ | −1060 | | −890 | mV | Apply $V_{IHmax}$ to each $D_n$ input, one at a time, with $V_{ILmin}$ applied to $\overline{OE}_n$ inputs and $V_{IHmax}$ applied to $\overline{CP}$ and $\overline{CE}_n$ inputs. |
| | | | $T_A = +25°C$ | −960 | | −810 | mV | |
| | | | $T_A = +85°C$ | −890 | | −700 | mV | |
| $V_{OHT}$ | HIGH level output threshold voltage | | $T_A = -30°C$ | −1080 | | | mV | Apply $V_{IHT}$ to each $D_n$ input, one at a time, with $V_{ILmin}$ applied to $\overline{OE}_n$ inputs and $V_{IHmax}$ applied to $\overline{CP}$ and $\overline{CE}_n$ inputs. |
| | | | $T_A = +25°C$ | −980 | | | mV | |
| | | | $T_A = +85°C$ | −910 | | | mV | |
| $V_{OLT}$ | LOW level output threshold voltage | | $T_A = -30°C$ | | | −1655 | mV | Apply $V_{ILT}$ to each $D_n$ input, one at a time, with $V_{IHmax}$ applied to $\overline{CP}$ and $\overline{CE}_n$ inputs and $V_{ILmin}$ applied to $\overline{OE}_n$ inputs. |
| | | | $T_A = +25°C$ | | | −1630 | mV | |
| | | | $T_A = +85°C$ | | | −1595 | mV | |
| $V_{OL}$ | LOW level output voltage | | $T_A = -30°C$ | −1890 | | −1675 | mV | Apply $V_{ILmin}$ to each $D_n$ input, one at a time, with $V_{IHmax}$ applied to $\overline{CP}$ and $\overline{CE}_n$ inputs, and $V_{ILmin}$ applied to $\overline{OE}_n$ inputs. |
| | | | $T_A = +25°C$ | −1850 | | −1650 | mV | |
| | | | $T_A = +85°C$ | −1825 | | −1615 | mV | |
| $I_{IH}$ | HIGH level input current | $D_n$ inputs | $T_A = -30°C$ | | | 390 | μA | Apply $V_{IHmax}$ to the $\overline{CP}$ input and to each $D_n$ input under test, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | | | 245 | μA | |
| | | | $T_A = +85°C$ | | | 245 | μA | |
| | | $\overline{CE}_n$ inputs | $T_A = -30°C$ | | | 425 | μA | Apply $V_{IHmax}$ to each $\overline{CE}_n$ input under test, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | | | 265 | μA | |
| | | | $T_A = +85°C$ | | | 265 | μA | |
| | | $\overline{CP}$ input | $T_A = -30°C$ | | | 560 | μA | Apply $V_{IHmax}$ to CP input with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | | | 350 | μA | |
| | | | $T_A = +85°C$ | | | 350 | μA | |
| | | $\overline{OE}_n$ inputs | $T_A = +30°C$ | | | 560 | μA | Apply $V_{IHmax}$ to the $\overline{CP}$ input and to all $D_n$ inputs and to each $\overline{OE}_n$ input under test, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | | | 350 | μA | |
| | | | $T_A = +85°C$ | | | 350 | μA | |
| $I_{IL}$ | LOW level input current | | $T_A = -30°C$ | 0.5 | | | μA | Apply $V_{ILmin}$ to each input under test, one at a time, with $V_{IHmax}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | 0.5 | | | μA | |
| | | | $T_A = +85°C$ | 0.3 | | | μA | |
| $-I_{EE}$ | $V_{EE}$ supply current | | $T_A = -30°C$ | | | 82 | mA | Apply $V_{ILmin}$ to $\overline{CP}$ input. |
| | | | $T_A = +25°C$ | | 59.6 | 72 | mA | |
| | | | $T_A = +85°C$ | | | 82 | mA | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | | $T_A = +25°C$ | | 0.016 | | V/V | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | | 0.250 | | V/V | |
| $\frac{\Delta V_{BB}}{\Delta V_{EE}}$ | Reference bias voltage compensation | | | | 0.148 | | V/V | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst-case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 5.

## Latch 10133



**NOTES:**

$V_{IHmax}$ – Maximum HIGH level input voltage (the most positive $V_{IH}$).
$V_{IHT}$ – HIGH level input threshold voltage.
$V_{ILT}$ – LOW level input threshold voltage.
$V_{ILmin}$ – Minimum LOW level input voltage (the most negative $V_{IL}$).
$V_{OHmax}$ – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition.
$V_{OHmin}$ – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition.
$V_{OHT}$ – HIGH level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLT}$ – LOW level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLmax}$ – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions.
$V_{OLmin}$ – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions.
$V_{BB}$ – Reference bias voltage. The internally generated reference voltage which is used to set the input and output threshold level.

**Figure 5. Transfer Characteristics**

## AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$

| PARAMETER | $T_A = -30°C$ | | $T_A = +25°C$ | | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Typ | Max | Min | Max | | |
| $t_{PLH}$ Propagation delay | 1.0 | 5.6 | 1.0 | 4.0 | 5.4 | 1.1 | 5.9 | ns | Figs. 6, 7, 8 |
| $t_{PHL}$ $D_n$ to $\overline{Q}_n$ | 1.0 | 5.6 | 1.0 | 4.0 | 5.4 | 1.1 | 5.9 | ns | |
| $t_{PLH}$ Propagation delay | 1.0 | 5.4 | 1.0 | 4.0 | 5.4 | 1.2 | 6.0 | ns | |
| $t_{PHL}$ $\overline{CP}$ $\overline{CE}_n$ to $\overline{Q}_n$ | 1.0 | 5.4 | 1.0 | 4.0 | 5.4 | 1.2 | 6.0 | ns | |
| $t_{PLH}$ Propagation delay | 1.0 | 3.2 | 1.0 | 2.0 | 3.1 | 1.0 | 3.4 | ns | |
| $t_{PHL}$ $\overline{OE}_n$ to $\overline{Q}_n$ | 1.0 | 3.2 | 1.0 | 2.0 | 3.1 | 1.0 | 3.4 | ns | |
| $t_s$ Setup time $D_n$ to CP | 2.5 | | 2.5 | 0.7 | | 2.5 | | ns | |
| $t_h$ Hold time $D_n$ to CP | 1.5 | | 1.5 | 0.7 | | 1.5 | | ns | |
| $t_{TLH}$ Transition time | 1.0 | 3.6 | 1.1 | 2.0 | 3.5 | 1.1 | 3.8 | ns | |
| $t_{THL}$ 20% to 80%, 80% to 20% | 1.0 | 3.6 | 1.1 | 2.0 | 3.5 | 1.1 | 3.8 | ns | |

## AC WAVEFORMS

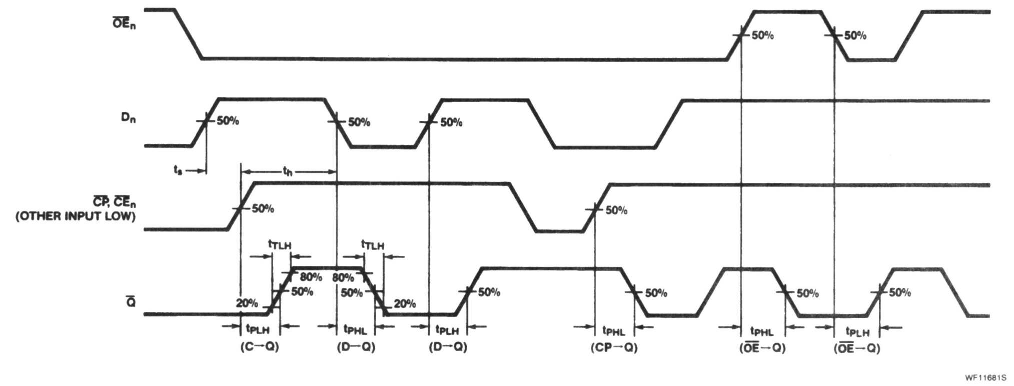
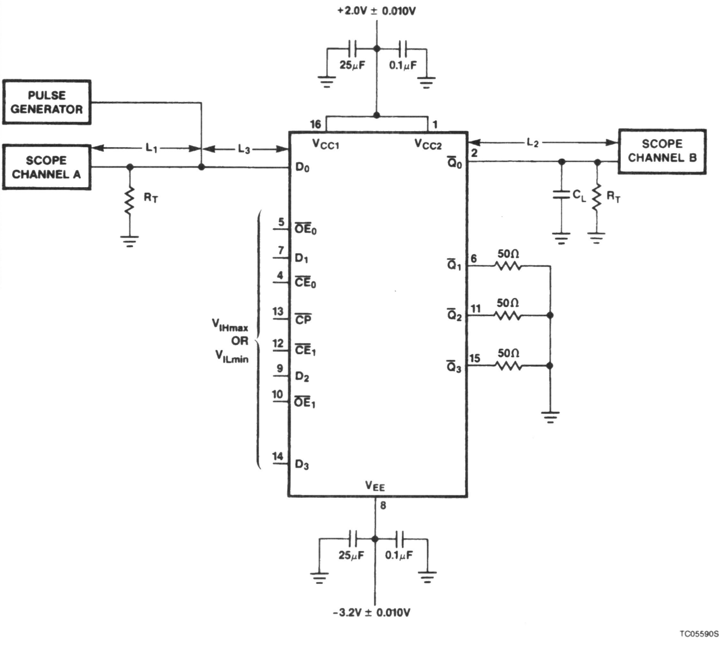

$\overline{OE}_n$
$D_n$
$\overline{CP}$, $\overline{CE}_n$ (OTHER INPUT LOW)
$\overline{Q}$
50%
$t_s$
$t_h$
$t_{TLH}$
$t_{TLH}$
80%
80%
20%
20%
$t_{PLH}$ (C→Q)
$t_{PHL}$ (D→Q)
$t_{PLH}$ (D→Q)
$t_{PHL}$ (CP→Q)
$t_{PHL}$ ($\overline{OE}$→Q)
$t_{PLH}$ ($\overline{OE}$→Q)
WF11681S

Figure 6. Propagation Delay, Setup Time, Hold Time, and Transition Time

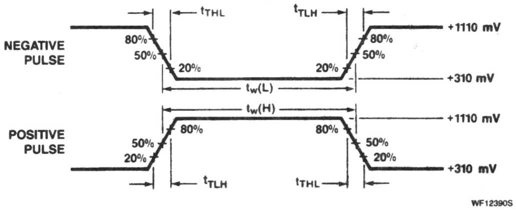
## TEST CIRCUITS AND WAVEFORMS


+2.0V ± 0.010V
25μF
0.1μF
PULSE GENERATOR
SCOPE CHANNEL A
$L_1$
$L_3$
$R_T$
16
1
$V_{CC1}$
$V_{CC2}$
2
$\overline{Q}_0$
$L_2$
SCOPE CHANNEL B
$C_L$
$R_T$
$D_0$
5 $\overline{OE}_0$
7 $D_1$
4 $\overline{CE}_0$
13 $\overline{CP}$
12 $\overline{CE}_1$
9 $D_2$
10 $\overline{OE}_1$
14 $D_3$
$V_{IHmax}$ OR $V_{ILmin}$
6 $\overline{Q}_1$
11 $\overline{Q}_2$
15 $\overline{Q}_3$
50Ω
50Ω
50Ω
$V_{EE}$
8
25μF
0.1μF
-3.2V ± 0.010V
TC05590S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1μF and 25μF from GND to $V_{CC}$, 0.01μF and 25mF from GND to $V_{EE}$ (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than ¼ inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed ¼ inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than ¼ inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance $\leqslant$ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed ¼ inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.

Figure 7. Test Circuit


NEGATIVE PULSE
POSITIVE PULSE
$t_{THL}$
$t_{TLH}$
80%
50%
20%
$t_w(L)$
$t_w(H)$
+1110 mV
+310 mV
WF12390S

| INPUT PULSE REQUIREMENTS<br>$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$, $V_T = GND (0V)$ | | | | | |
|---|---|---|---|---|---|
| **Family** | **Amplitude** | **Rep Rate** | **Pulse Width** | **$t_{TLH}$** | **$t_{THL}$** |
| 10K ECL | 800mVp-p | 1MHz | 500ns | 2.0 ±0.2ns | 2.0 ±0.2ns |

Figure 8. Input Pulse Definition

**Signetics**

**ECL Products**

# 10134
## Multiplexer/Latch

**Dual 2-Input Multiplexer With Clocked D-Type Latches**
***Product Specification***

## DESCRIPTION

The 10134 is a Dual 2-Input Multiplexer with Clocked D-Type Latches. Latches can be clocked by the common Clock (CP) when the Clock Enable input ($\overline{CE}$) is LOW or by the Clock Enable input when the common Clock is held in the LOW state. The outputs are latched by the positive transition of the clock. Any change in the data will be registered at the output only if the clock is LOW.

Data inputs are selected by two Data Select inputs ($S_0$, $S_1$). All unused inputs must be tied LOW to $V_{IL}$ or $V_{EE}$.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 10134 | 3.0ns | 42mA |

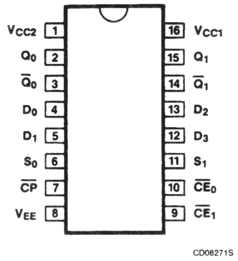
## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} =$ GND; $V_{EE} = -5.2V$<br>$T_A = -30°C$ to $+85°C$ |
|---|---|
| Plastic DIP | 10134N |
| Ceramic DIP | 10134F |

## PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_0 - D_3$ | Data Inputs |
| $\overline{CP}$ | Clock Input |
| $\overline{CE}_0$, $\overline{CE}_1$ | Clock Enable Inputs |
| $S_0$, $S_1$ | Select Inputs |
| $Q_0$, $Q_1$, $\overline{Q}_0$, $\overline{Q}_1$ | Data Outputs |

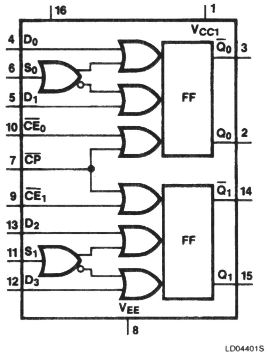
## PIN CONFIGURATION



VCC2 1
Q0 2
Q̄0 3
D0 4
D1 5
S0 6
C̄P̄ 7
VEE 8
16 VCC1
15 Q1
14 Q̄1
13 D2
12 D3
11 S1
10 C̄Ē0
9 C̄Ē1
CD08271S

Figure 1

## LOGIC SYMBOL



16
1
VCC1
4 D0
6 S0
5 D1
10 C̄Ē0
7 C̄P̄
9 C̄Ē1
13 D2
11 S1
12 D3
Q̄0 3
Q0 2
Q̄1 14
Q1 15
FF
FF
VEE
8
LD04401S

Figure 2

## Multiplexer/Latch 10134

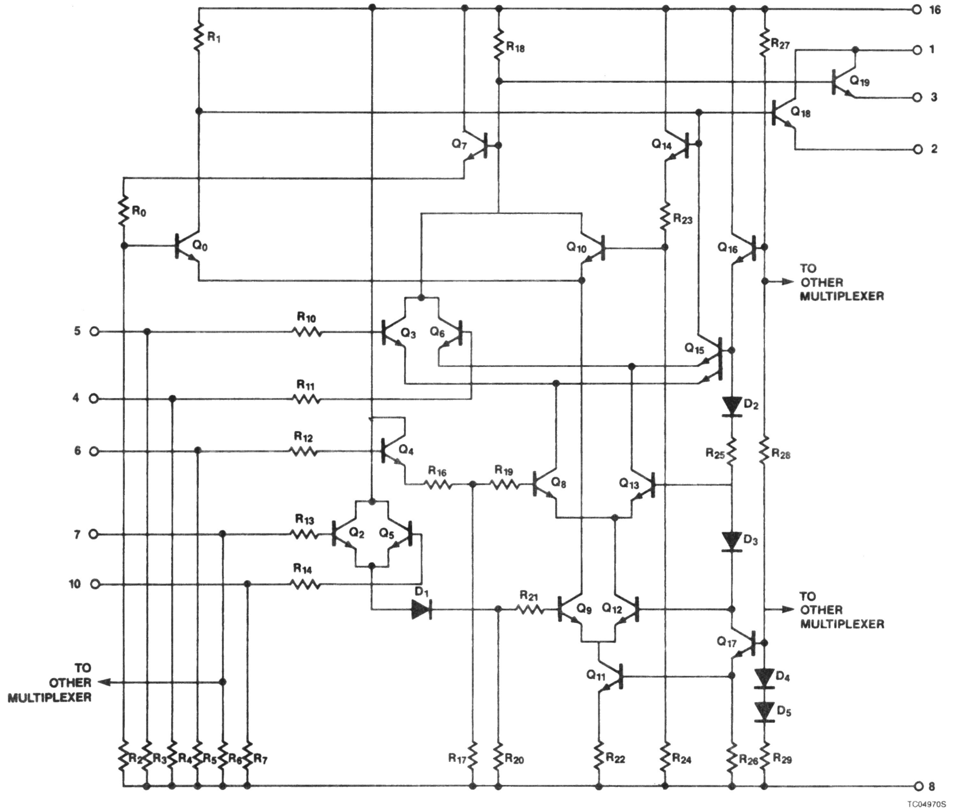

16
R1
R18
R27
1
Q19
3
Q18
2
Q7
Q14
R0
R23
Q0
Q10
Q16
TO OTHER MULTIPLEXER
5
R10
Q3
Q6
Q15
4
R11
D2
6
R12
Q4
R25
R28
R16
R19
Q8
Q13
7
R13
Q2
Q5
D3
10
R14
D1
R21
Q9
Q12
TO OTHER MULTIPLEXER
Q17
TO OTHER MULTIPLEXER
Q11
D4
D5
R2
R3
R4
R5
R6
R7
R17
R20
R22
R24
R26
R29
8
TC04970S

**Figure 3. Circuit Diagram (One Multiplexer)**

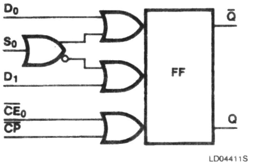

D0
S0
D1
CE0
CP
FF
Q̄
Q
LD04411S

**Figure 4. Logic Function**

### FUNCTION TABLE

| $S_n$ | $\overline{CP}$ | $\overline{CE}_n$ | $Q_{n+1}$ |
|---|---|---|---|
| L | L | L | $D_1$ |
| L | L | H | $Q_n$ |
| L | H | L | $Q_n$ |
| L | H | H | $Q_n$ |
| H | L | L | $D_2$ |
| H | L | H | $Q_n$ |
| H | H | L | $Q_n$ |
| H | H | H | $Q_n$ |

## Multiplexer/Latch 10134

**ABSOLUTE MAXIMUM RATINGS** (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | | 10K ECL | UNIT |
|---|---|---|---|---|
| $V_{EE}$ | Supply voltage | | -8.0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | | 0 to $V_{EE}$ | V |
| $I_O$ | Output source current | | -50 | mA |
| $T_S$ | Storage temperature | | -55 to +150 | °C |
| $T_J$ | Maximum junction temperature | Ceramic package | +165 | °C |
| | | Plastic package | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | 10K ECL | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | -5.2 | | V |
| $V_{IH}$ | HIGH level input voltage | $T_A$ = -30°C | | | -890 | mV |
| | | $T_A$ = +25°C | | | -810 | mV |
| | | $T_A$ = +85°C | | | -700 | mV |
| $V_{IHT}$ | HIGH level input threshold voltage | $T_A$ = -30°C | -1205 | | | mV |
| | | $T_A$ = +25°C | -1105 | | | mV |
| | | $T_A$ = +85°C | -1035 | | | mV |
| $V_{ILT}$ | LOW level input threshold voltage | $T_A$ = -30°C | | | -1500 | mV |
| | | $T_A$ = +25°C | | | -1475 | mV |
| | | $T_A$ = +85°C | | | -1440 | mV |
| $V_{IL}$ | LOW level input voltage | $T_A$ = -30°C | -1890 | | | mV |
| | | $T_A$ = +25°C | -1850 | | | mV |
| | | $T_A$ = +85°C | -1825 | | | mV |
| $T_A$ | Operating ambient temperature | | -30 | +25 | +85 | °C |

**NOTE:**
When operating at $V_{EE}$ other than specified voltage (-5.2V), the DC and AC Characteristics will vary slightly from specified values.
(See table of DC Characteristics)

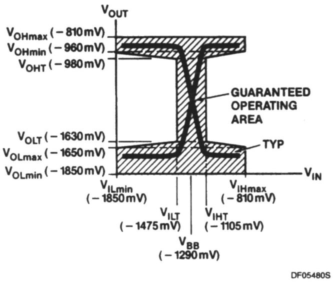
## Multiplexer/Latch 10134

**DC ELECTRICAL CHARACTERISTICS** $V_{CC1} = V_{CC2}$ = GND, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$, output loading with 50Ω to $-2.0V \pm 0.010V$ unless otherwise specified[1,3]

| PARAMETER | | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | | $T_A = -30°C$ | −1060 | | −890 | mV | For $Q_0$ output, apply $V_{IHmax}$ to $D_0$ input with $V_{ILmin}$ applied to $S_0$, $\overline{CE}_0$ and $\overline{CP}$ inputs.<br>For $\overline{Q}_0$ outputs, apply $V_{ILmin}$ to all inputs. |
| | | | $T_A = +25°C$ | −960 | | −810 | mV | |
| | | | $T_A = +85°C$ | −890 | | −700 | mV | |
| $V_{OHT}$ | HIGH level output threshold voltage | | $T_A = -30°C$ | −1080 | | | mV | For $Q_0$ outputs, apply $V_{IHT}$ to $D_0$ input with $V_{ILmin}$ applied to $S_0$, $\overline{CE}_0$ and $\overline{CP}$ inputs.<br>For $\overline{Q}_0$ outputs, apply $V_{ILT}$ to $D_0$ input with $V_{ILmin}$ applied to $S_0$, $\overline{CE}_0$, and $\overline{CP}$ inputs. |
| | | | $T_A = +25°C$ | −980 | | | mV | |
| | | | $T_A = +85°C$ | −910 | | | mV | |
| $V_{OLT}$ | LOW level output threshold voltage | | $T_A = -30°C$ | | | −1655 | mV | For $Q_0$ outputs, apply $V_{ILT}$ to $D_0$ input with $V_{ILmin}$ applied to $S_0$, $\overline{CE}_0$ and $\overline{CP}$ inputs.<br>For $\overline{Q}_0$ outputs, apply $V_{IHT}$ to $D_0$ input with $V_{ILmin}$ applied to $S_0$, $\overline{CE}_0$, and $\overline{CP}$ inputs. |
| | | | $T_A = +25°C$ | | | −1630 | mV | |
| | | | $T_A = +85°C$ | | | −1595 | mV | |
| $V_{OL}$ | LOW level output voltage | | $T_A = -30°C$ | −1890 | | −1675 | mV | For $Q_0$ outputs, apply $V_{ILmin}$ to all inputs.<br>For $\overline{Q}_0$ outputs, apply $V_{IHmax}$ to $D_0$ input with $V_{ILmin}$ applied to $S_0$, $\overline{CE}_0$, and $\overline{CP}$ inputs. |
| | | | $T_A = +25°C$ | −1850 | | −1650 | mV | |
| | | | $T_A = +85°C$ | −1825 | | −1615 | mV | |
| $I_{IH}$ | HIGH level input current | $D_0$ input | $T_A = -30°C$ | | | 460 | µA | Apply $V_{IHmax}$ to $D_0$ input with $V_{ILmin}$ applied to $S_0$ and all other inputs (measure $D_0$ input only). |
| | | | $T_A = +25°C$ | | | 290 | µA | |
| | | | $T_A = +85°C$ | | | 290 | µA | |
| | | $D_1$ input | $T_A = -30°C$ | | | 460 | µA | Apply $V_{IHmax}$ to $D_1$ and $S_0$ inputs with $V_{ILmin}$ applied to all other inputs (measure $D_1$ input only). |
| | | | $T_A = +25°C$ | | | 290 | µA | |
| | | | $T_A = +85°C$ | | | 290 | µA | |
| | | $D_2$ input | $T_A = -30°C$ | | | 460 | µA | Apply $V_{IHmax}$ to $D_2$ input with $V_{ILmin}$ applied to all other inputs (measure $D_2$ input only). |
| | | | $T_A = +25°C$ | | | 290 | µA | |
| | | | $T_A = +85°C$ | | | 290 | µA | |
| | | $D_3$ input | $T_A = -30°C$ | | | 460 | µA | Apply $V_{IHmax}$ to $D_3$ and $S_1$ inputs with $V_{ILmin}$ applied to all other inputs (measure $D_3$ input only). |
| | | | $T_A = +25°C$ | | | 290 | µA | |
| | | | $T_A = +85°C$ | | | 290 | µA | |
| $I_{IH}$ | HIGH level input current | $\overline{CE}_n$, $S_n$ inputs | $T_A = -30°C$ | | | 425 | µA | Apply $V_{IHmax}$ to each input under test, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | | | 265 | µA | |
| | | | $T_A = +85°C$ | | | 265 | µA | |
| | | $\overline{CP}$ input | $T_A = -30°C$ | | | 460 | µA | Apply $V_{IHmax}$ to $\overline{CP}$ input with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | | | 290 | µA | |
| | | | $T_A = +85°C$ | | | 290 | µA | |
| $I_{IL}$ | LOW level input current | | $T_A = -30°C$ | 0.5 | | | µA | Apply $V_{ILmin}$ to each input under test, one at a time, with $V_{IHmax}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | 0.5 | | | µA | |
| | | | $T_A = +85°C$ | 0.3 | | | µA | |
| $-I_{EE}$ | $V_{EE}$ supply current | | $T_A = -30°C$ | | | 60 | mA | |
| | | | $T_A = +25°C$ | | 42 | 55 | mA | |
| | | | $T_A = +85°C$ | | | 60 | mA | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | | $T_A = +25°C$ | | 0.016 | | V/V | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | | 0.250 | | V/V | |
| $\frac{\Delta V_{BB}}{\Delta V_{EE}}$ | Reference bias voltage compensation | | | | 0.148 | | V/V | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst-case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 5.



**NOTES:**

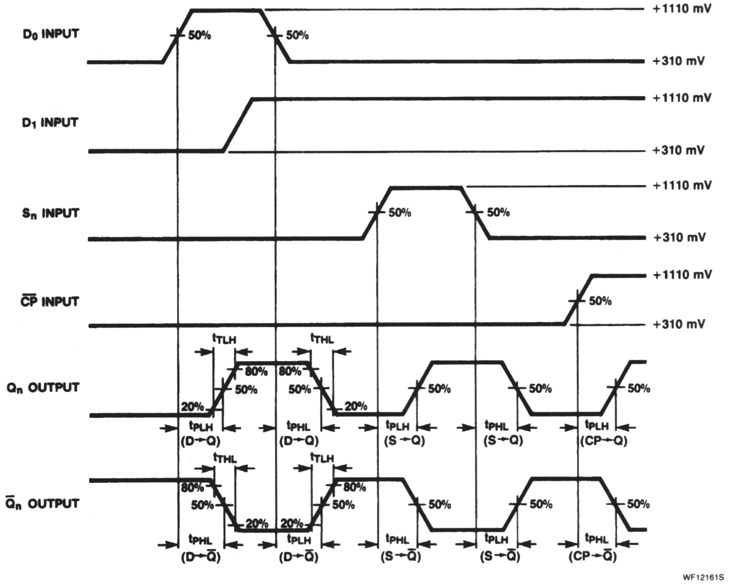
| | |
|---|---|
| $V_{IHmax}$ | – Maximum HIGH level input voltage (the most positive $V_{IH}$). |
| $V_{IHT}$ | – HIGH level input threshold voltage. |
| $V_{ILT}$ | – LOW level input threshold voltage. |
| $V_{ILmin}$ | – Minimum LOW level input voltage (the most negative $V_{IL}$). |
| $V_{OHmax}$ | – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition. |
| $V_{OHmin}$ | – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition. |
| $V_{OHT}$ | – HIGH level output threshold voltage with the inputs set to their respective threshold levels. |
| $V_{OLT}$ | – LOW level output threshold voltage with the inputs set to their respective threshold levels. |
| $V_{OLmax}$ | – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions. |
| $V_{OLmin}$ | – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions. |
| $V_{BB}$ | – Reference bias voltage. The internally generated reference voltage which is used to set the input and output threshold level. |

**Figure 5. Transfer Characteristics**

## AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$

| PARAMETER | $T_A = -30°C$ | | $T_A = +25°C$ | | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Typ | Max | Min | Max | | |
| $t_{PLH}$ Propagation delay<br>$t_{PHL}$ $D_n$ to $Q_n$ | 1.0<br>1.0 | 3.5<br>3.5 | 1.0<br>1.0 | 3.0<br>3.0 | 3.3<br>3.3 | 1.0<br>1.0 | 3.6<br>3.6 | ns<br>ns | Figs. 6, 7, 8 |
| $t_{PLH}$ Propagation delay<br>$t_{PHL}$ $\overline{CP}$ to $Q_n$ | 1.0<br>1.0 | 6.0<br>6.0 | 1.0<br>1.0 | | 5.7<br>5.7 | 1.0<br>1.0 | 6.3<br>6.3 | ns<br>ns | |
| $t_{PLH}$ Propagation delay<br>$t_{PHL}$ $S_n$ to $Q_n$ | 1.0<br>1.0 | 4.8<br>4.8 | 1.0<br>1.0 | | 4.6<br>4.6 | 1.0<br>1.0 | 5.0<br>5.0 | ns<br>ns | |
| $t_s$ Setup time $D_n$ to $\overline{CP}$ | 2.5 | | 2.5 | | | 2.5 | | ns | |
| $t_h$ Hold time $D_n$ to $\overline{CP}$ | 1.5 | | 1.5 | | | 1.5 | | ns | |
| $t_s$ Setup time $S_n$ to $\overline{CP}$ | 3.5 | | 3.5 | | | 3.5 | | ns | |
| $t_h$ Hold time $S_n$ to $\overline{CP}$ | 1.0 | | 1.0 | | | 1.0 | | ns | |
| $t_{TLH}$ Transition time<br>$t_{THL}$ 20% to 80%, 80% to 20% | 1.5<br>1.5 | 3.7<br>3.7 | 1.5<br>1.5 | | 3.5<br>3.5 | 1.5<br>1.5 | 3.8<br>3.8 | ns<br>ns | |

## AC WAVEFORMS


D0 INPUT
D1 INPUT
Sn INPUT
C̄P̄ INPUT
Qn OUTPUT
Q̄n OUTPUT
+1110 mV
+310 mV
50%
80%
20%
tTLH
tTHL
tPLH (D→Q)
tPHL (D→Q)
tPLH (S→Q)
tPHL (S→Q)
tPLH (CP→Q)
tPHL (D→Q̄)
tPLH (D→Q̄)
tPHL (S→Q̄)
tPLH (S→Q̄)
tPHL (CP→Q̄)
WF12161S

NOTES:
1. Any change on the data input will be registered at the output only if the clock is LOW.
2. Outputs are latched on the positive transition of the clock.

Figure 6. Propagation Delays and Transition Times

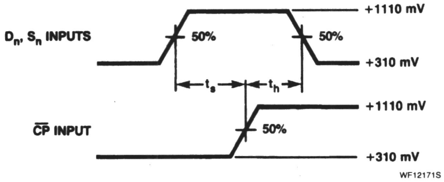
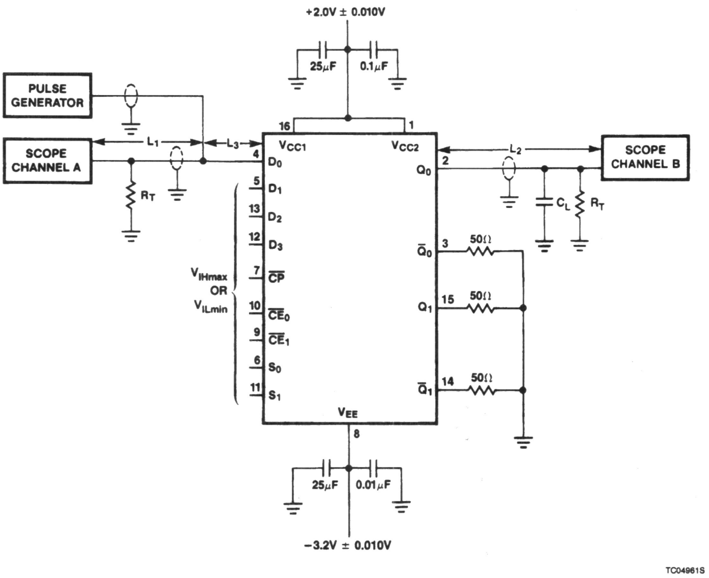

Dn, Sn INPUTS
C̄P̄ INPUT
+1110 mV
+310 mV
50%
ts
th
WF12171S

Figure 7. Setup and Hold Times

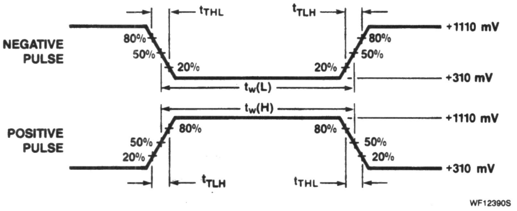
## TEST CIRCUITS AND WAVEFORMS


+2.0V ± 0.010V
25µF
0.1µF
PULSE GENERATOR
SCOPE CHANNEL A
L1
L3
RT
16
1
VCC1
VCC2
4 D0
5 D1
13 D2
12 D3
7 CP
10 CE0
9 CE1
6 S0
11 S1
VIHmax OR VILmin
2 Q0
3 Q̄0
15 Q1
14 Q̄1
50Ω
50Ω
50Ω
L2
SCOPE CHANNEL B
CL
RT
VEE
8
25µF
0.01µF
−3.2V ± 0.010V
TC04961S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1µF and 25µF from GND to $V_{CC}$, 0.01µF and 25µF from GND to $V_{EE}$ (0.01 and 0.1µF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than ¼ inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed ¼ inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than ¼ inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance ≤ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed ¼ inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.

Figure 8. Test Circuit


NEGATIVE PULSE
POSITIVE PULSE
tTHL
tTLH
80%
50%
20%
tw(L)
tw(H)
+1110 mV
+310 mV
+1110 mV
+310 mV
WF12390S

| INPUT PULSE REQUIREMENTS<br>$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$, $V_T$ = GND (0V) | | | | | |
|---|---|---|---|---|---|
| Family | Amplitude | Rep Rate | Pulse Width | $t_{TLH}$ | $t_{THL}$ |
| 10K ECL | 800mVp-p | 1MHz | 500ns | 2.0 ±0.2ns | 2.0 ±0.2ns |

Figure 9. Input Pulse Definition

Signetics

# 10135

## Flip-Flop

**Dual J-K Master-Slave Flip-Flop**
***Product Specification***

**ECL Products**

### DESCRIPTION

The 10135 is a Dual Master-Slave DC coupled J-K Flip-Flop. It contains a common clock and separate $\overline{J}$-$\overline{K}$ inputs which do not affect the output when the Clock is static. The outputs of the 10135 register a change on the $\overline{J}$ or $\overline{K}$ inputs with a positive transition of the Clock. Asynchronous Set (S) and Reset (R) inputs are provided which override the Clock. Unused inputs must be tied LOW to $V_{IL}$ or $V_{EE}$.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 10135 | 3.0ns | 54mA |

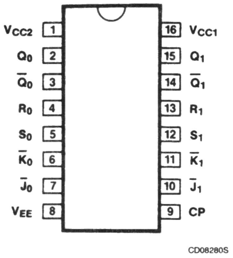
### ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} = \text{GND}$; $V_{EE} = -5.2V$<br>$T_A = -30°C$ to $+85°C$ |
|---|---|
| Plastic DIP | 10135N |
| Ceramic DIP | 10135F |

### PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $\overline{J}_n$, $\overline{K}_n$ | J, K Inputs |
| CP | Clock Input |
| $S_n$, $R_n$ | Set and Reset Inputs |
| $Q_n$, $\overline{Q}_n$ | Data Outputs |

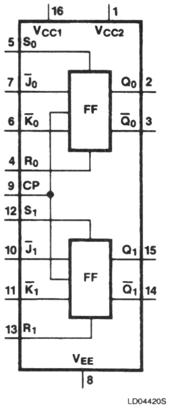
### PIN CONFIGURATION



VCC2 1
Q0 2
Q̄0 3
R0 4
S0 5
K̄0 6
J̄0 7
VEE 8
16 VCC1
15 Q1
14 Q̄1
13 R1
12 S1
11 K̄1
10 J̄1
9 CP
CD08280S

Figure 1

### LOGIC SYMBOL



16
1
VCC1
VCC2
5 S0
7 J̄0
6 K̄0
4 R0
9 CP
12 S1
10 J̄1
11 K̄1
13 R1
FF
FF
Q0 2
Q̄0 3
Q1 15
Q̄1 14
VEE
8
LD04420S

Figure 2

## Flip-Flop 10135

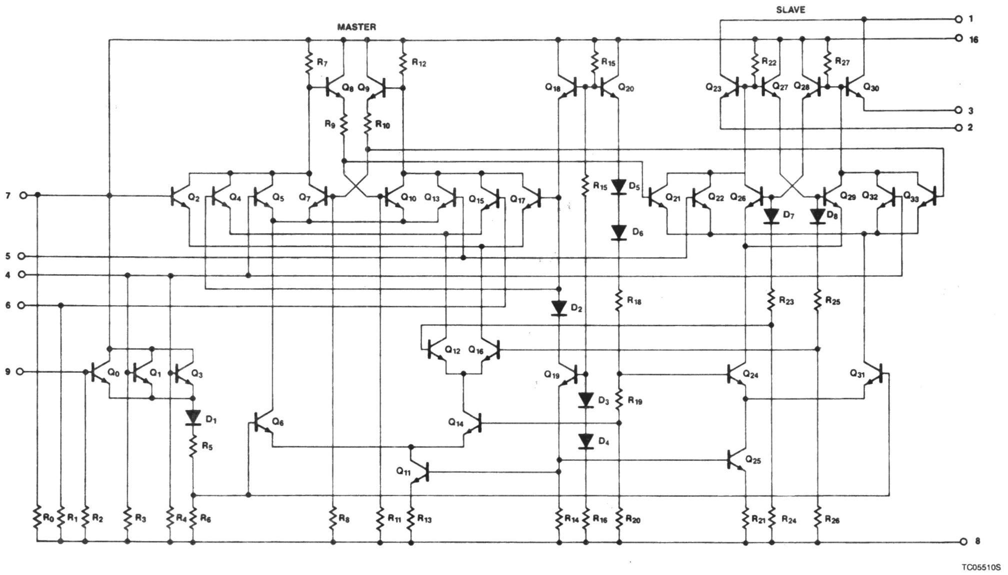

MASTER
SLAVE
1
16
3
2
7
5
4
6
9
8
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
Q16
Q17
Q18
Q19
Q20
Q21
Q22
Q23
Q24
Q25
Q26
Q27
Q28
Q29
Q30
Q31
Q32
Q33
D1
D2
D3
D4
D5
D6
D7
D8
R0
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
R18
R19
R20
R21
R22
R23
R24
R25
R26
R27
TC05510S

**Figure 3. Circuit Diagram (One Flip-flop)**

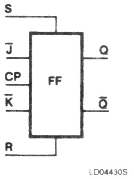

S
J̄
CP
K̄
R
FF
Q
Q̄
LD04430S

**Figure 4. Logic Function**

## FUNCTION TABLES

| R | S | $Q_{n+1}$ |
|---|---|---|
| L | L | $Q_n$ |
| L | H | H |
| H | L | L |
| H | H | * |

*Not allowed.
R and S must be low.

| $\overline{J}$ | $\overline{K}$ | $Q_{n+1}$ |
|---|---|---|
| L | L | $\overline{Q}_n$ |
| H | L | L |
| L | H | H |
| H | H | $Q_n$ |

Positive Logic:
H = HIGH state (the more positive voltage) = 1
L = LOW state (the less positive voltage) = 0
X = Don't Care

# Flip-Flop

# 10135

**ABSOLUTE MAXIMUM RATINGS** (Operation beyond the limits set forth in this table may impair useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | | 10K ECL | UNIT |
|---|---|---|---|---|
| $V_{EE}$ | Supply voltage | | −8.0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | | 0 to $V_{EE}$ | V |
| $I_O$ | Output current | | −50 | mA |
| $T_S$ | Storage temperature | | −55 to +150 | °C |
| $T_J$ | Maximum junction temperature | Ceramic package | +165 | °C |
| | | Plastic package | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | 10K ECL | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | −5.2 | | V |
| $V_{IH}$ | HIGH level input voltage | $T_A$ = −30°C | | | −890 | mV |
| | | $T_A$ = +25°C | | | −810 | mV |
| | | $T_A$ = +85°C | | | −700 | mV |
| $V_{IHT}$ | HIGH level input threshold voltage | $T_A$ = −30°C | −1205 | | | mV |
| | | $T_A$ = +25°C | −1105 | | | mV |
| | | $T_A$ = +85°C | −1035 | | | mV |
| $V_{ILT}$ | LOW level input threshold voltage | $T_A$ = −30°C | | | −1500 | mV |
| | | $T_A$ = +25°C | | | −1475 | mV |
| | | $T_A$ = +85°C | | | −1440 | mV |
| $V_{IL}$ | LOW level input voltage | $T_A$ = −30°C | −1890 | | | mV |
| | | $T_A$ = +25°C | −1850 | | | mV |
| | | $T_A$ = +85°C | −1825 | | | mV |
| $T_A$ | Operating ambient temperature | | −30 | +25 | +85 | °C |

**NOTE:**
When operating at $V_{EE}$ other than specified voltage (−5.2V), the DC and AC Characteristics will vary slightly from specified values. (See table of DC Characteristics)

**DC ELECTRICAL CHARACTERISTICS** $V_{CC1} = V_{CC2}$ = GND, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$, output loading with 50Ω to $-2.0V \pm 0.010V$ unless otherwise specified[1,3]

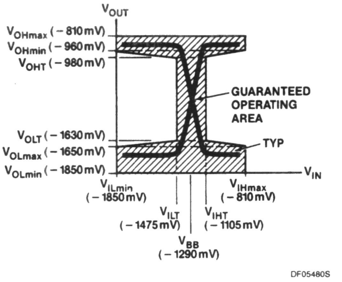
| PARAMETER | | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | | $T_A = -30°C$ | -1060 | | -890 | mV | For Q outputs, apply $V_{IHmax}$ to S input with $V_{ILmin}$ applied to R input and all other inputs. For $\overline{Q}$ outputs, apply $V_{IHmax}$ to R input with $V_{ILmin}$ applied to S input and all other inputs. |
| | | | $T_A = +25°C$ | -960 | | -810 | mV | |
| | | | $T_A = +85°C$ | -890 | | -700 | mV | |
| $V_{OHT}$ | HIGH level output threshold voltage | | $T_A = -30°C$ | -1080 | | | mV | For Q outputs, apply $V_{IHT}$ to S input with $V_{ILmin}$ applied to R input and all other inputs. For $\overline{Q}$ outputs, apply $V_{IHT}$ to R input with $V_{ILmin}$ applied to S input and all other inputs. |
| | | | $T_A = +25°C$ | -980 | | | mV | |
| | | | $T_A = +85°C$ | -910 | | | mV | |
| $V_{OLT}$ | LOW level output threshold voltage | | $T_A = -30°C$ | | | -1655 | mV | For Q outputs, apply $V_{IHT}$ to R input with $V_{ILmin}$ applied to S input and all other inputs. For $\overline{Q}$ outputs, apply $V_{IHT}$ to S input with $V_{ILmin}$ applied to R input and all other inputs. |
| | | | $T_A = +25°C$ | | | -1630 | mV | |
| | | | $T_A = +85°C$ | | | -1595 | mV | |
| $V_{OL}$ | LOW level output voltage | | $T_A = -30°C$ | -1890 | | -1675 | mV | For Q outputs, apply $V_{IHmax}$ to R input with $V_{ILmin}$ applied to S input and all other inputs. For $\overline{Q}$ outputs, apply $V_{IHmax}$ to S input with $V_{ILmin}$ applied to R input and all other inputs. |
| | | | $T_A = +25°C$ | -1850 | | -1650 | mV | |
| | | | $T_A = +85°C$ | -1825 | | -1615 | mV | |
| $I_{IH}$ | HIGH level input current | S, R inputs | $T_A = -30°C$ | | | 620 | µA | Apply $V_{IHmax}$ to each input under test, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | | | 390 | µA | |
| | | | $T_A = +85°C$ | | | 390 | µA | |
| | | J, K, CP inputs | $T_A = -30°C$ | | | 425 | µA | Apply $V_{IHmax}$ to each input under test, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | | | 265 | µA | |
| | | | $T_A = +85°C$ | | | 265 | µA | |
| $I_{IL}$ | LOW level input current | | $T_A = -30°C$ | 0.5 | | | µA | Apply $V_{ILmin}$ to each input under test, one at a time, with $V_{IHmax}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | 0.5 | | | µA | |
| | | | $T_A = +85°C$ | 0.3 | | | µA | |
| $-I_{EE}$ | $V_{EE}$ supply current | | $T_A = -30°C$ | | | 75 | mA | |
| | | | $T_A = +25°C$ | | 54 | 68 | mA | |
| | | | $T_A = +85°C$ | | | 75 | mA | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | | $T_A = +25°C$ | | 0.016 | | V/V | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | | 0.250 | | V/V | |
| $\frac{\Delta V_{BB}}{\Delta V_{EE}}$ | Reference bias voltage compensation | | | | 0.148 | | V/V | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst-case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 5.

## Flip-Flop

## 10135



**NOTES:**

$V_{IHmax}$ – Maximum HIGH level input voltage (the most positive $V_{IH}$).

$V_{IHT}$ – HIGH level input threshold voltage.

$V_{ILT}$ – LOW level input threshold voltage.

$V_{ILmin}$ – Minimum LOW level input voltage (the most negative $V_{IL}$).

$V_{OHmax}$ – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition.

$V_{OHmin}$ – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition.

$V_{OHT}$ – HIGH level output threshold voltage with the inputs set to their respective threshold levels.

$V_{OLT}$ – LOW level output threshold voltage with the inputs set to their respective threshold levels.

$V_{OLmax}$ – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions.

$V_{OLmin}$ – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions.

$V_{BB}$ – Reference bias voltage (the internally generated reference voltage which is used to set the input and output threshold level).

Figure 5. Transfer Characteristics

## AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$

| PARAMETER | $T_A = -30°C$ | | $T_A = +25°C$ | | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Typ | Max | Min | Max | | |
| $f_{MAX}$ Maximum clock frequency | 125 | | 125 | 140 | | 115 | | MHz | |
| $t_{PLH}$ Propagation delay | 1.8 | 5.0 | 1.8 | 3.0 | 4.5 | 1.8 | 4.6 | ns | Figs. 6, 7, 8 |
| $t_{PHL}$ $D_n$, $\overline{J}_n$, $\overline{K}_n$ to $Q_n$, $Q_n$ | 1.8 | 5.0 | 1.8 | 3.0 | 4.5 | 1.8 | 4.6 | ns | |
| $t_{PLH}$ Propagation delay | 1.8 | 5.6 | 1.8 | 3.0 | 5.0 | 1.8 | 5.2 | ns | |
| $t_{PHL}$ $S_n$ to $Q_n$, $\overline{Q}_n$ | 1.8 | 5.6 | 1.8 | 3.0 | 5.0 | 1.8 | 5.2 | ns | |
| $t_{PLH}$ Propagation delay | 1.8 | 5.6 | 1.8 | 3.0 | 5.0 | 1.8 | 5.2 | ns | |
| $t_{PHL}$ $R_n$ to $Q_n$, $\overline{Q}_n$ | 1.8 | 5.6 | 1.8 | 3.0 | 5.0 | 1.8 | 5.2 | ns | |
| $t_s$ Setup time $\overline{J}_n$, $\overline{K}_n$ to CP | 2.5 | | 2.5 | 1.0 | | 2.5 | | ns | |
| $t_h$ Hold time $\overline{J}_n$, $\overline{K}_n$ to CP | 1.5 | | 1.5 | 1.0 | | 1.5 | | ns | |
| $t_{TLH}$ Transition time | 1.1 | 4.8 | 1.1 | 2.0 | 4.5 | 1.1 | 4.7 | ns | |
| $t_{THL}$ 20% to 80%, 80% to 20% | 1.1 | 4.8 | 1.1 | 2.0 | 4.5 | 1.1 | 4.7 | ns | |

## AC WAVEFORMS

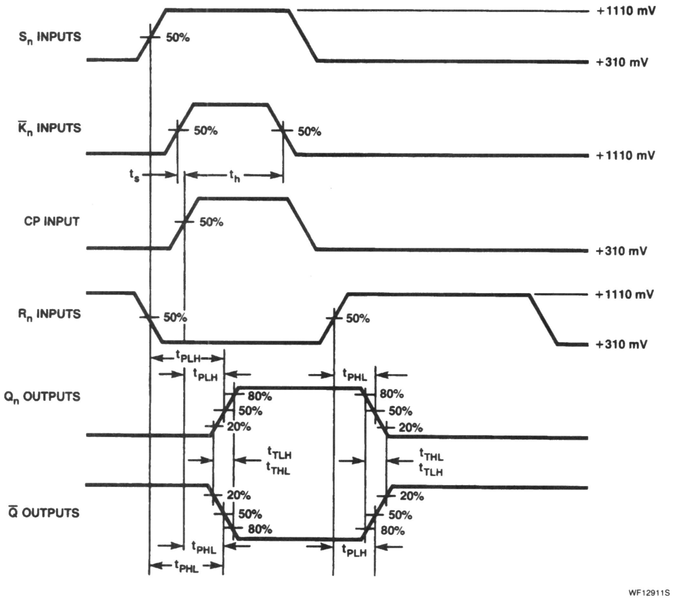
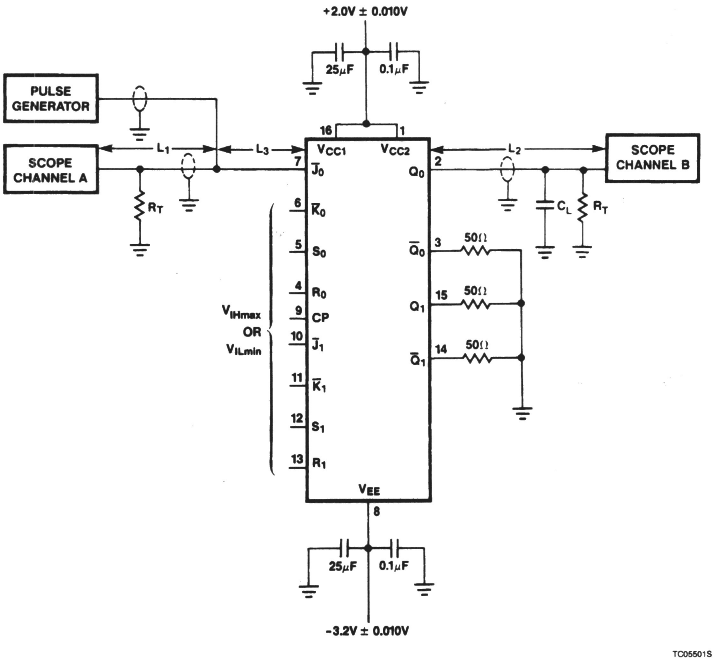

$S_n$ INPUTS
50%
+1110 mV
+310 mV
$\overline{K}_n$ INPUTS
50%
50%
+1110 mV
$t_s$
$t_h$
CP INPUT
50%
+310 mV
$R_n$ INPUTS
50%
50%
+1110 mV
+310 mV
$t_{PLH}$
$t_{PLH}$
$t_{PHL}$
$Q_n$ OUTPUTS
80%
50%
20%
80%
50%
20%
$t_{TLH}$
$t_{THL}$
$t_{THL}$
$t_{TLH}$
$\overline{Q}$ OUTPUTS
20%
50%
80%
20%
50%
80%
$t_{PHL}$
$t_{PHL}$
$t_{PLH}$
WF12911S

Figure 6. Propagation Delays, Setup Times, Hold Times, and Transition Times

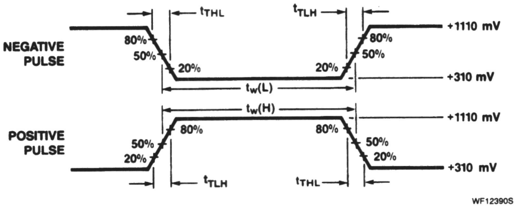
## TEST CIRCUITS AND WAVEFORMS


+2.0V ± 0.010V
25μF
0.1μF
PULSE GENERATOR
SCOPE CHANNEL A
L1
L3
RT
16
1
VCC1
VCC2
7
J0
6
K̄0
5
S0
4
R0
9
CP
10
J1
11
K̄1
12
S1
13
R1
VEE
8
VIHmax OR VILmin
2
Q0
3
Q̄0
15
Q1
14
Q̄1
50Ω
50Ω
50Ω
L2
SCOPE CHANNEL B
CL
RT
25μF
0.1μF
-3.2V ± 0.010V
TC05501S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$
2. Decoupling 0.1μF and 25μF from GND to $V_{CC}$, 0.01μF and 25μF from GND to $V_{EE}$. (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance ⩽ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ±1% or better.

Figure 7. Test Circuit


NEGATIVE PULSE
POSITIVE PULSE
tTHL
tTLH
80%
50%
20%
tw(L)
tw(H)
+1110 mV
+310 mV
WF12390S

| INPUT PULSE REQUIREMENTS<br>$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$, $V_T$ = GND (0V) | | | | | |
|---|---|---|---|---|---|
| **Family** | **Amplitude** | **Rep Rate** | **Pulse Width** | **$t_{TLH}$** | **$t_{THL}$** |
| 10K ECL | 800mVp-p | 1MHz | 500ns | 2.0 ±0.2ns | 2.0 ±0.2ns |

Figure 8. Input Pulse Definition

Signetics

# 10136
# Universal Counter

**Universal Hexadecimal Counter**
***Product Specification***

**ECL Products**

## DESCRIPTION

The 10136 is a high-speed Hexadecimal Synchronous Counter that can count up, count down, preset, or stop count at frequencies exceeding 100MHz. The operation mode of the counter is programmed by three control lines ($S_0$, $S_1$, and CP) as can be seen in the function select table. In the preset mode (loading step), a clock pulse is needed for the information present on the data inputs ($D_0$, $D_1$, $D_2$, and $D_3$) to be entered into the counter. $\overline{C}_{out}$ goes LOW on the terminal count, or when the counter is being preset.

The counter changes state only on the positive-going edge of the clock, so at any other time any other input may change without any result (except for $\overline{C}_{out}$).

This binary counter can be used in many applications, such as in computing for high-speed control processors and peripheral controllers. Unused inputs must be tied LOW to $V_{IL}$ or $V_{EE}$.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 10136 | 3.3ns | 120mA |

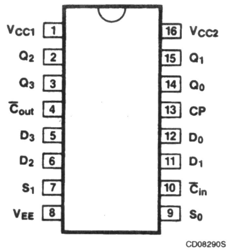
## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} = \text{GND}$; $V_{EE} = -5.2\text{V}$<br>$T_A = -30°\text{C}$ to $+85°\text{C}$ |
|---|---|
| Plastic DIP | 10136N |
| Ceramic DIP | 10136F |

## PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_0 - D_3$ | Data Inputs |
| CP | Clock Input |
| $\overline{C}_{in}$ | Carry-in Input |
| $S_0$, $S_1$ | Select Inputs |
| $\overline{C}_{out}$ | Carry-out Output |
| $Q_0 - Q_3$ | Data Outputs |

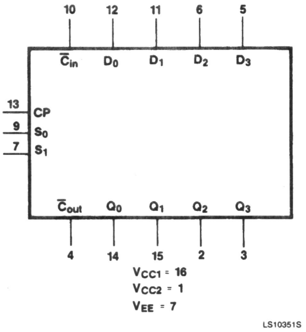
## PIN CONFIGURATION



VCC1 1
Q2 2
Q3 3
C̄out 4
D3 5
D2 6
S1 7
VEE 8
16 VCC2
15 Q1
14 Q0
13 CP
12 D0
11 D1
10 C̄in
9 S0
CD08290S

Figure 1

## LOGIC SYMBOL



10
12
11
6
5
C̄in
D0
D1
D2
D3
13
CP
9
S0
7
S1
C̄out
Q0
Q1
Q2
Q3
4
14
15
2
3
VCC1 = 16
VCC2 = 1
VEE = 7
LS10351S

Figure 2

## Universal Counter

## 10136

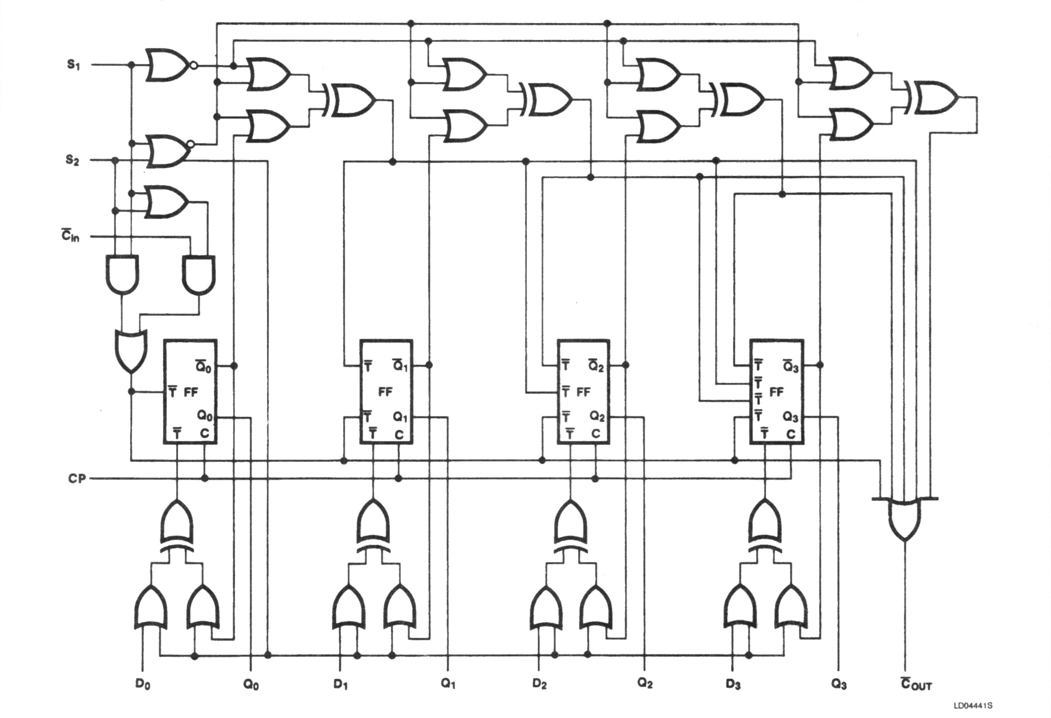

S1
S2
$\overline{C}_{in}$
CP
$\overline{Q}_0$
$\overline{T}$ FF
$Q_0$
$\overline{T}$ C
$\overline{T}$ $\overline{Q}_1$
FF
$\overline{T}$ $Q_1$
$\overline{T}$ C
$\overline{T}$ $\overline{Q}_2$
$\overline{T}$ FF
$\overline{T}$ $Q_2$
$\overline{T}$ C
$\overline{T}$ $\overline{Q}_3$
$\overline{T}$
$\overline{T}$ FF
$\overline{T}$ $Q_3$
$\overline{T}$ C
$D_0$
$Q_0$
$D_1$
$Q_1$
$D_2$
$Q_2$
$D_3$
$Q_3$
$\overline{C}_{OUT}$
LD04441S

Figure 3. Logic Diagram

### FUNCTION SELECT TABLE

| $S_0$ | $S_1$ | OPERATING MODE |
|---|---|---|
| L | L | Preset (program) |
| L | H | Increment (count up) |
| H | L | Decrement (count down) |
| H | H | Hold (stop count) |

Positive Logic:
H = HIGH state (the more positive voltage) = 1
L = LOW state (the less positive voltage) = 0
X = Don't Care

### SEQUENTIAL FUNCTION TABLE

| INPUTS | | | | | | | | OUTPUTS | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $S_0$ | $S_1$ | $D_0$ | $D_1$ | $D_2$ | $D_3$ | $\overline{C}_{IN}$ | CP | $Q_0$ | $Q_1$ | $Q_2$ | $Q_3$ | $\overline{C}_{OUT}$ |
| L | L | L | L | H | H | X | H | L | L | H | H | L |
| L | H | X | X | X | X | L | H | H | L | H | H | H |
| L | H | X | X | X | X | L | H | L | H | H | H | H |
| L | H | X | X | X | X | L | H | H | H | H | H | L |
| L | H | X | X | X | X | H | L | H | H | H | H | H |
| L | H | X | X | X | X | H | H | H | H | H | H | H |
| H | H | X | X | X | X | X | H | H | H | H | H | H |
| L | L | H | H | L | L | X | H | H | H | L | L | L |
| H | L | X | X | X | X | L | H | L | H | L | L | H |
| H | L | X | X | X | X | L | H | H | L | L | L | H |
| H | L | X | X | X | X | L | H | L | L | L | L | L |
| H | L | X | X | X | X | L | H | H | H | H | H | H |

# Universal Counter 10136

## ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | | 10K ECL | UNIT |
|---|---|---|---|---|
| $V_{EE}$ | Supply voltage | | -8.0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | | 0 to $V_{EE}$ | V |
| $I_O$ | Output source current | | -50 | mA |
| $T_S$ | Storage temperature | | -55 to +150 | °C |
| $T_J$ | Maximum junction temperature | Ceramic package | +165 | °C |
| | | Plastic package | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | 10K ECL | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | -5.2 | | V |
| $V_{IH}$ | HIGH level input voltage | $T_A$ = -30°C | | | -890 | mV |
| | | $T_A$ = +25°C | | | -810 | mV |
| | | $T_A$ = +85°C | | | -700 | mV |
| $V_{IHT}$ | HIGH level input threshold voltage | $T_A$ = -30°C | -1205 | | | mV |
| | | $T_A$ = +25°C | -1105 | | | mV |
| | | $T_A$ = +85°C | -1035 | | | mV |
| $V_{ILT}$ | LOW level input threshold voltage | $T_A$ = -30°C | | | -1500 | mV |
| | | $T_A$ = +25°C | | | -1475 | mV |
| | | $T_A$ = +85°C | | | -1440 | mV |
| $V_{IL}$ | LOW level input voltage | $T_A$ = -30°C | -1890 | | | mV |
| | | $T_A$ = +25°C | -1850 | | | mV |
| | | $T_A$ = +85°C | -1825 | | | mV |
| $T_A$ | Operating ambient temperature | | -30 | +25 | +85 | °C |

**NOTE:**
When operating at $V_{EE}$ other than specified voltage (-5.2V), the DC and AC Characteristics will vary slightly from specified values. (See table of DC Characteristics)

**DC ELECTRICAL CHARACTERISTICS** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$, output loading with 50Ω to $-2.0V \pm 0.010V$ unless otherwise specified[1,3]

| PARAMETER | | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | | $T_A = -30°C$ | -1060 | | -890 | mV | Apply $V_{IHmax}$ to all inputs. |
| | | | $T_A = +25°C$ | -960 | | -810 | mV | |
| | | | $T_A = +85°C$ | -890 | | -700 | mV | |
| $V_{OHT}$ | HIGH level output threshold voltage | | $T_A = -30°C$ | -1080 | | | mV | Apply $V_{IHT}$ to each input, one at a time, with $V_{IHmax}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | -980 | | | mV | |
| | | | $T_A = +85°C$ | -910 | | | mV | |
| $V_{OLT}$ | LOW level output threshold voltage | | $T_A = -30°C$ | | | -1655 | mV | Apply $V_{IHT}$ to $S_0$ input with $V_{IHmax}$ applied to CP input and $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | | | -1630 | mV | |
| | | | $T_A = +85°C$ | | | -1595 | mV | |
| $V_{OL}$ | LOW level output voltage | | $T_A = -30°C$ | -1890 | | -1675 | mV | Apply $V_{IHmax}$ to $S_0$ and CP inputs with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | -1850 | | -1650 | mV | |
| | | | $T_A = +85°C$ | -1825 | | -1615 | mV | |
| $I_{IH}$ | HIGH level input current | $D_n$ inputs | $T_A = -30°C$ | | | 350 | μA | Apply $V_{IHmax}$ to each input under test, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | | | 220 | μA | |
| | | | $T_A = +85°C$ | | | 220 | μA | |
| | | $S_1$ input | $T_A = -30°C$ | | | 425 | μA | |
| | | | $T_A = +25°C$ | | | 265 | μA | |
| | | | $T_A = +85°C$ | | | 265 | μA | |
| | | $S_0$, $\overline{C}_{in}$ inputs | $T_A = -30°C$ | | | 390 | μA | |
| | | | $T_A = +25°C$ | | | 245 | μA | |
| | | | $T_A = +85°C$ | | | 245 | μA | |
| | | CP input | $T_A = -30°C$ | | | 460 | μA | Apply $V_{IHmax}$ to CP input with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | | | 290 | μA | |
| | | | $T_A = +85°C$ | | | 290 | μA | |
| $I_{IL}$ | LOW level input current | | $T_A = -30°C$ | 0.5 | | | μA | Apply $V_{ILmin}$ to each input under test, one at a time, with $V_{IHmax}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | 0.5 | | | μA | |
| | | | $T_A = +85°C$ | 0.3 | | | μA | |
| $-I_{EE}$ | $V_{EE}$ supply current | | $T_A = -30°C$ | | | 165 | mA | |
| | | | $T_A = +25°C$ | | 120 | 150 | mA | |
| | | | $T_A = +85°C$ | | | 165 | mA | |

6

# Universal Counter

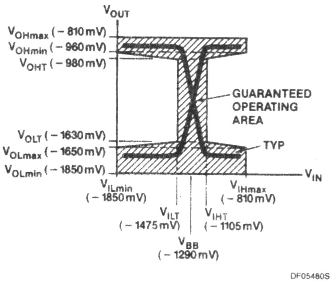
# 10136

## DC ELECTRICAL CHARACTERISTICS (Continued)

| PARAMETER | | MIN | TYP | MAX | UNIT | TEST CONDITIONS$^2$ |
|---|---|---|---|---|---|---|
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ HIGH level output voltage compensation | $T_A = +25°C$ | | 0.016 | | V/V | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ LOW level output voltage compensation | | | 0.250 | | V/V | |
| $\frac{\Delta V_{BB}}{\Delta V_{EE}}$ Reference bias voltage compensation | | | 0.148 | | V/V | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst-case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 4.



**NOTES:**

| | |
|---|---|
| $V_{IHmax}$ | – Maximum HIGH level input voltage (the most positive $V_{IH}$). |
| $V_{IHT}$ | – HIGH level input threshold voltage. |
| $V_{ILT}$ | – LOW level input threshold voltage. |
| $V_{ILmin}$ | – Minimum LOW level input voltage (the most negative $V_{IL}$). |
| $V_{OHmax}$ | – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition. |
| $V_{OHmin}$ | – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition. |
| $V_{OHT}$ | – HIGH level output threshold voltage with the inputs set to their respective threshold levels. |
| $V_{OLT}$ | – LOW level output threshold voltage with the inputs set to their respective threshold levels. |
| $V_{OLmax}$ | – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions. |
| $V_{OLmin}$ | – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions. |
| $V_{BB}$ | – Reference bias voltage (the internally generated reference voltage which is used to set the input and output threshold level). |

Figure 4. Transfer Characteristics

## AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$

| PARAMETER | $T_A = -30°C$ | | $T_A = +25°C$ | | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Typ | Max | Min | Max | | |
| $f_{MAX}$ Maximum clock frequency | 125 | | 125 | 150 | | 125 | | MHz | Figs. 5, 10, 11 |
| $t_{PLH}$ Propagation delay CP to $Q_n$ | 1.7 | 4.8 | 1.7 | 3.3 | 4.5 | 1.7 | 5.0 | ns | Figs. 5, 6, 7, 10, 11 |
| | 1.7 | 4.8 | 1.7 | 3.3 | 4.5 | 1.7 | 5.0 | ns | |
| $t_{PHL}$ Propagation delay CP to $\overline{C}_{OUT}$ | 2.0 | 10.9 | 2.5 | 7.0 | 10.5 | 2.4 | 11.5 | ns | |
| | 2.0 | 10.9 | 2.5 | 7.0 | 10.5 | 2.4 | 11.5 | ns | |
| $t_{PLH}$ Propagation delay | 1.6 | 7.4 | 1.6 | 5.0 | 6.9 | 1.9 | 7.5 | ns | |
| $t_{PHL}$ $\overline{C}_{IN}$ to $\overline{C}_{OUT}$ | 1.6 | 7.4 | 1.6 | 5.0 | 6.9 | 1.9 | 7.5 | ns | |
| $t_s$ Setup time $D_n$ to CP | 3.5 | | 3.5 | | | 3.5 | | ns | Figs. 8, 10, 11 |
| $t_h$ Hold time $D_n$ to CP | 0.0 | | 0.0 | | | 0.0 | | ns | |
| $t_s$ Setup time $S_n$ to CP | 7.5 | | 7.5 | | | 7.5 | | ns | |
| $t_h$ Hold time $S_n$ to CP | −2.5 | | −2.5 | | | −2.5 | | ns | |
| $t_s$ Setup time $\overline{C}_{IN}$ to CP | 4.5 | | 3.7 | | | 4.5 | | ns | Figs. 9, 10, 11 |
| CP to $\overline{C}_{IN}$ | −1.0 | | −1.0 | | | −1.0 | | ns | |
| $t_h$ Hold time CP to $\overline{C}_{IN}$ | −1.6 | | −1.6 | | | −1.6 | | ns | |
| $\overline{C}_{IN}$ to CP | 4.0 | | 3.1 | | | 4.0 | | ns | |
| $t_{TLH}$ Transition time | 0.9 | 3.3 | 1.1 | 2.0 | 3.3 | 1.1 | 3.5 | ns | Figs. 5, 6, 7, 10, 11 |
| $t_{THL}$ 20% to 80%, 80% to 20% | 0.9 | 3.3 | 1.1 | 2.0 | 3.3 | 1.1 | 3.5 | ns | |

## AC WAVEFORMS

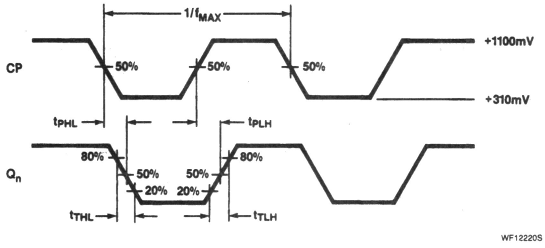

1/fMAX
+1100mV
CP
50%
50%
50%
+310mV
tPHL
tPLH
80%
Qn
50%
50%
20%
20%
80%
tTHL
tTLH
WF12220S

Figure 5. Propagation Delay and Transition Times for Clock Input to Outputs and Maximum Clock Frequency

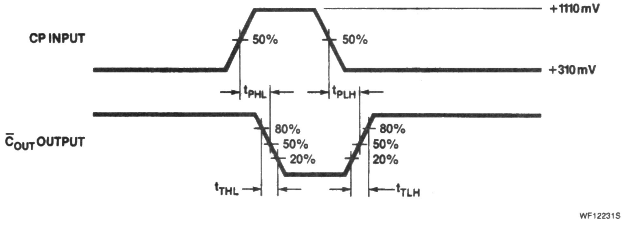
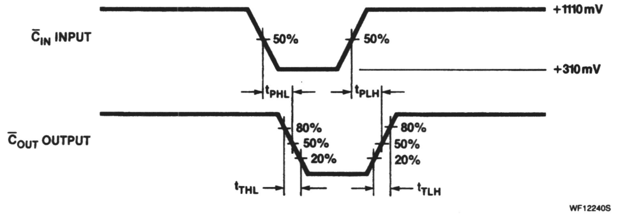

+1110mV
CP INPUT
50%
50%
+310mV
tPHL
tPLH
C̄OUT OUTPUT
80%
50%
20%
80%
50%
20%
tTHL
tTLH
WF12231S

Figure 6. Propagation Delay and Transition Time for Clock Input to Carry-Out Output

# Universal Counter

# 10136


$\overline{C}_{IN}$ INPUT
50%
50%
+1110mV
+310mV
$t_{PHL}$
$t_{PLH}$
$\overline{C}_{OUT}$ OUTPUT
80%
50%
20%
80%
50%
20%
$t_{THL}$
$t_{TLH}$
WF12240S

**NOTE:**
Setup times are the minimum times before the positive transition of the clock pulse (CP) that information must be present at the data input (D) or control input (S).
Hold times are the minimum times after the positive transition of the clock pulse (CP) that information must remain unchanged at the data input (D) or control input (S).

Figure 7. Propogation Delay and Transtion Time for Carry-In Input to Carry-Out Output

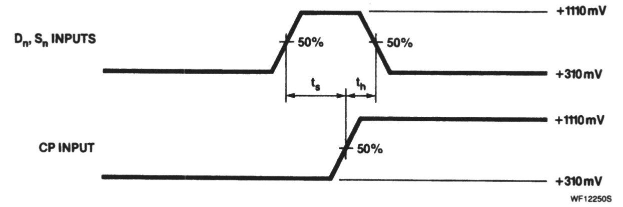
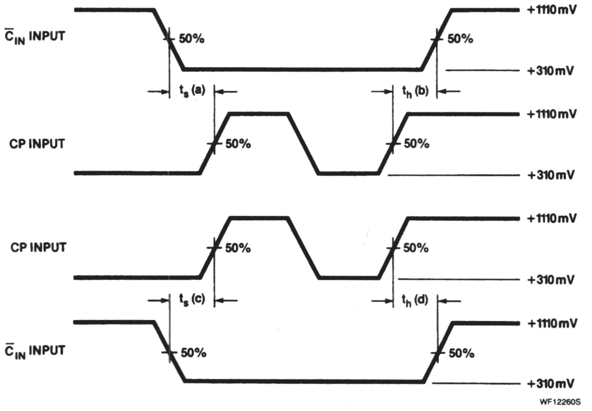

$D_n$, $S_n$ INPUTS
50%
50%
+1110mV
+310mV
$t_s$
$t_h$
CP INPUT
50%
+1110mV
+310mV
WF12250S

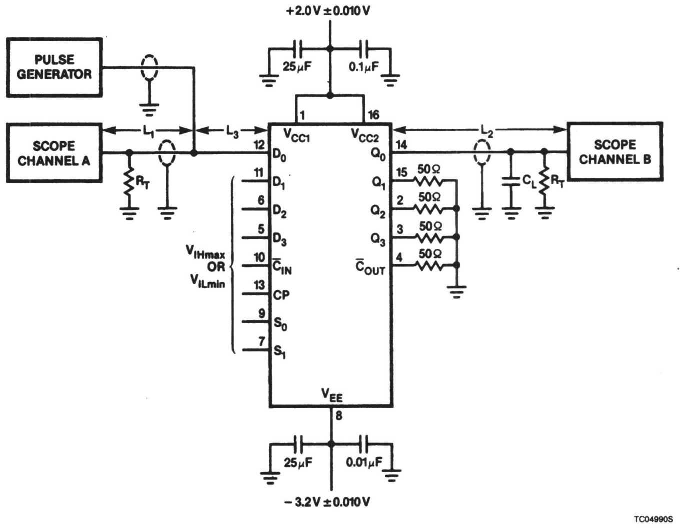
Figure 8. Setup and Hold Times for Data And Select Inputs to Clock Input


$\overline{C}_{IN}$ INPUT
50%
50%
+1110mV
+310mV
$t_s$ (a)
$t_h$ (b)
CP INPUT
50%
50%
+1110mV
+310mV
CP INPUT
50%
50%
+1110mV
+310mV
$t_s$ (c)
$t_h$ (d)
$\overline{C}_{IN}$ INPUT
50%
50%
+1110mV
+310mV
WF12260S

**NOTE:**
(a) is the minimum time to wait to clock the counter after it has been enabled.
(b) is the minimum time that the counter may be clocked before it has been disabled.
(c) is the minimum time that a clock pulse may be applied with no effect on the state of the counter before it is enabled.
(d) is the minimum time to wait before a clock pulse may be applied with no effect on the state of the counter after it is disabled.
(b) and (c) may be negative numbers.

Figure 9. Setup and Hold Times for Carry-In to Clock Input

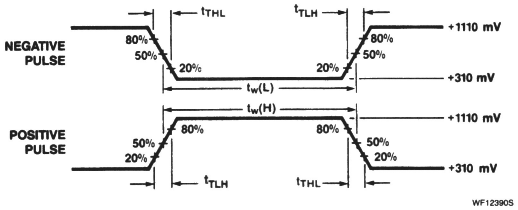
## TEST CIRCUITS AND WAVEFORMS


+2.0V ±0.010V
25µF
0.1µF
PULSE GENERATOR
SCOPE CHANNEL A
L1
L3
L2
RT
1
16
VCC1
VCC2
12
D0
11
D1
6
D2
5
D3
10
C̄IN
13
CP
9
S0
7
S1
14
Q0
15
Q1
2
Q2
3
Q3
4
C̄OUT
50Ω
50Ω
50Ω
50Ω
VIHmax OR VILmin
CL
RT
SCOPE CHANNEL B
VEE
8
25µF
0.01µF
−3.2V ±0.010V
TC04990S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1µF and 25µF from GND to $V_{CC}$, 0.01µF and 25µF from GND to $V_{EE}$. (0.01 and 0.1µF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance ≤ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.

Figure 10. Test Circuit


NEGATIVE PULSE
POSITIVE PULSE
tTHL
tTLH
80%
50%
20%
tw(L)
tw(H)
+1110 mV
+310 mV
WF12390S

| INPUT PULSE REQUIREMENTS<br>$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$, $V_T$ = GND (0V) | | | | | |
|---|---|---|---|---|---|
| **Family** | **Amplitude** | **Rep Rate** | **Pulse Width** | **$t_{TLH}$** | **$t_{THL}$** |
| 10K ECL | 800mVp-p | 1MHz | 500ns | 2.0 ±0.2ns | 2.0 ±0.2ns |

Figure 11. Input Pulse Definition

**Signetics**

# 10137

# Universal Counter

**Universal Decade Counter**
***Product Specification***

**ECL Products**

## DESCRIPTION

The 10137 is a high-speed Synchronous Decade Counter that can count up, count down, preset, or stop count at frequencies exceeding 100MHz.

The operation mode of the counter is programmed by three control lines ($S_0$, $S_1$ and $\overline{C}_{IN}$) as can be seen in the function select table.

In the preset mode (loading step), a clock pulse is needed for the information present on the data inputs ($D_0$, $D_1$, $D_2$, and $D_3$) to be entered into the counter. $\overline{C}_{OUT}$ goes LOW on the terminal count. $\overline{C}_{OUT}$ is partially decoded from $Q_0$ and $Q_1$ directly, so in the preset mode the condition of $\overline{C}_{OUT}$ after the clock's positive excursion will depend on the condition of $Q_0$ and/or $Q_1$.

The counter changes state only on the positive going edge of the clock, so at any other time, any other input may change without any result (except $\overline{C}_{OUT}$). The sequence for counting out of proper states is as shown in the state diagrams. This binary counter can be used in many applications, such as in computing for high speed control processors and peripheral controllers.

Unused inputs must be tied LOW to $V_{IL}$ or $V_{EE}$.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 10137 | 3.3ns | 120mA |

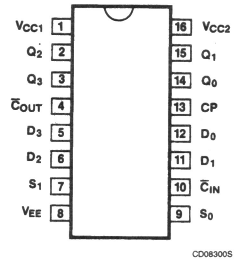
## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} = GND$; $V_{EE} = -5.2V$<br>$T_A = -30°C$ to $+85°C$ |
|---|---|
| Plastic DIP | 10137N |
| Ceramic DIP | 10137F |

## PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_0 - D_3$ | Data Inputs |
| CP | Clock Input |
| $\overline{C}_{IN}$ | Carry-in Input |
| $S_0$, $S_1$ | Select Inputs |
| $\overline{C}_{OUT}$ | Carry-out Output |
| $Q_0 - Q_3$ | Data Outputs |

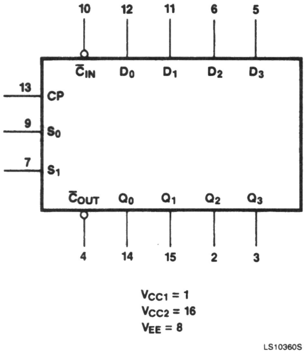
## PIN CONFIGURATION



$V_{CC1}$ 1
$Q_2$ 2
$Q_3$ 3
$\overline{C}_{OUT}$ 4
$D_3$ 5
$D_2$ 6
$S_1$ 7
$V_{EE}$ 8
16 $V_{CC2}$
15 $Q_1$
14 $Q_0$
13 CP
12 $D_0$
11 $D_1$
10 $\overline{C}_{IN}$
9 $S_0$
CD08300S

Figure 1

## LOGIC SYMBOL



10
12
11
6
5
$\overline{C}_{IN}$
$D_0$
$D_1$
$D_2$
$D_3$
13
CP
9
$S_0$
7
$S_1$
$\overline{C}_{OUT}$
$Q_0$
$Q_1$
$Q_2$
$Q_3$
4
14
15
2
3
$V_{CC1}$ = 1
$V_{CC2}$ = 16
$V_{EE}$ = 8
LS10360S

Figure 2

## Universal Counter

## 10137

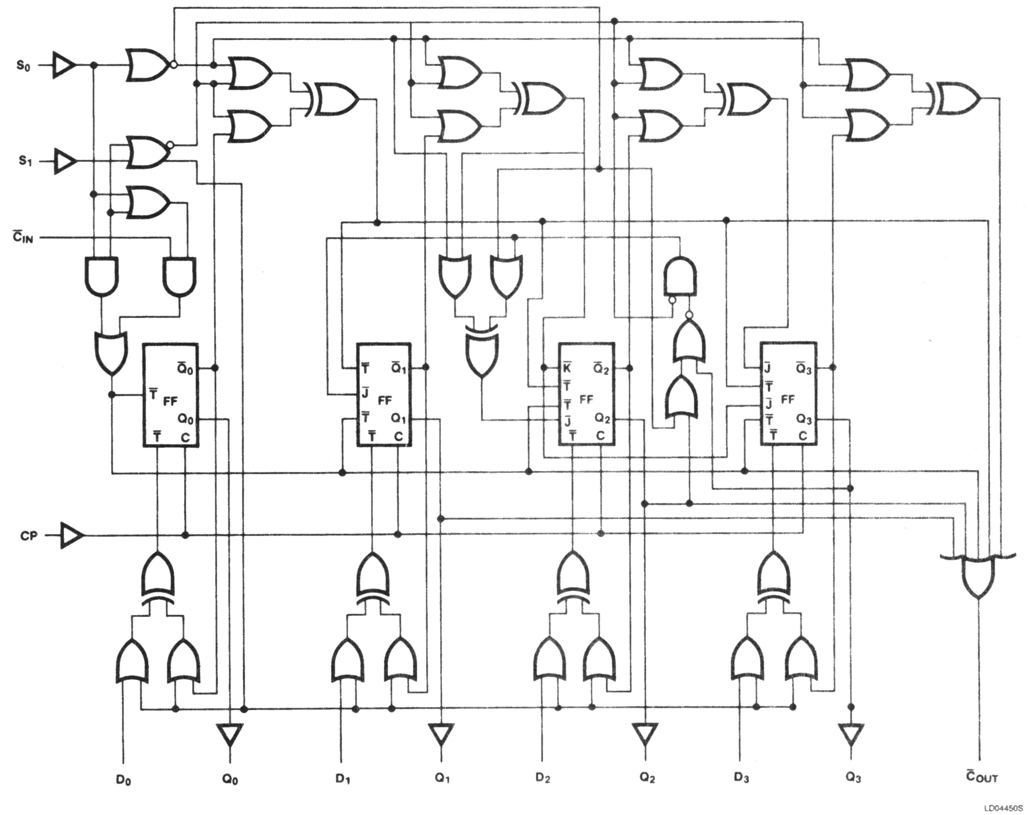

$S_0$
$S_1$
$\overline{C}_{IN}$
CP
$\overline{Q}_0$
$\overline{T}$ FF
$Q_0$
$\overline{T}$ C
$\overline{T}$ $\overline{Q}_1$
$\overline{J}$ FF
$\overline{T}$ $Q_1$
$\overline{T}$ C
$\overline{K}$ $\overline{Q}_2$
$\overline{T}$
$\overline{T}$ FF
$\overline{J}$ $Q_2$
$\overline{T}$ C
$\overline{J}$ $\overline{Q}_3$
$\overline{T}$
$\overline{J}$ FF
$\overline{T}$ $Q_3$
$\overline{T}$ C
$D_0$
$Q_0$
$D_1$
$Q_1$
$D_2$
$Q_2$
$D_3$
$Q_3$
$\overline{C}_{OUT}$
LD04450S

Figure 3. Logic Diagram

### FUNCTION SELECT TABLE

| $S_0$ | $S_1$ | OPERATING MODE |
|---|---|---|
| L | L | Preset |
| L | H | Increment (count up) |
| H | L | Decrement (count down) |
| H | H | Hold (stop count) |

Positive Logic:
H = HIGH state (the more positive voltage) = 1
L = LOW state (the less positive voltage) = 0
X = Don't Care

)

## Universal Counter 10137

### SEQUENTIAL FUNCTION TABLE

| INPUTS | | | | | | | | OUTPUTS | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $S_0$ | $S_1$ | $D_0$ | $D_1$ | $D_2$ | $D_3$ | $\overline{C}_{IN}$ | C | $Q_0$ | $Q_1$ | $Q_2$ | $Q_3$ | $\overline{C}_{OUT}$ |
| L | L | H | H | H | H | X | H | H | H | H | L | H |
| L | H | X | X | X | X | L | H | L | L | L | H | H |
| L | H | X | X | X | X | L | H | H | L | L | H | L |
| L | H | X | X | X | X | L | H | L | L | L | L | H |
| L | H | X | X | X | X | L | H | H | L | L | L | H |
| L | H | X | X | X | X | H | H | H | L | L | L | H |
| L | H | X | X | X | X | H | H | H | L | L | L | H |
| H | H | X | X | X | X | X | H | H | L | L | L | H |
| L | L | H | H | L | L | X | H | H | H | L | L | H |
| H | L | X | X | X | X | L | H | L | H | L | L | H |
| H | L | X | X | X | X | L | H | H | L | L | L | H |
| H | L | X | X | X | X | L | H | L | L | L | L | L |

**ABSOLUTE MAXIMUM RATINGS** (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | | 100K ECL | UNIT |
|---|---|---|---|---|
| $V_{EE}$ | Supply voltage | | −8.0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | | 0 to $V_{EE}$ | V |
| $I_O$ | Output source current | | −50 | mA |
| $T_S$ | Storage temperature | | −55 to +150 | °C |
| $T_J$ | Maximum junction temperature | Ceramic package | +165 | °C |
| | | Plastic package | +150 | °C |

### DC OPERATING CONDITIONS

| PARAMETER | | | 10K ECL | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | −5.2 | | V |
| $V_{IH}$ | HIGH level input voltage | $T_A$ = −30°C | | | −890 | mV |
| | | $T_A$ = +25°C | | | −810 | mV |
| | | $T_A$ = +85°C | | | −700 | mV |
| $V_{IHT}$ | HIGH level input threshold voltage | $T_A$ = −30°C | −1205 | | | mV |
| | | $T_A$ = +25°C | −1105 | | | mV |
| | | $T_A$ = +85°C | −1035 | | | mV |
| $V_{ILT}$ | LOW level input threshold voltage | $T_A$ = −30°C | | | −1500 | mV |
| | | $T_A$ = +25°C | | | −1475 | mV |
| | | $T_A$ = +85°C | | | −1440 | mV |
| $V_{IL}$ | LOW level input voltage | $T_A$ = −30°C | −1890 | | | mV |
| | | $T_A$ = +25°C | −1850 | | | mV |
| | | $T_A$ = +85°C | −1825 | | | mV |
| $T_A$ | Operating ambient temperature | | −30 | +25 | +85 | °C |

**NOTE:**
When operating at $V_{EE}$ other than specified voltage (−5.2V) the DC and AC Characteristics will vary slightly from specified values. (See table of DC Characteristics)

## Universal Counter

## 10137

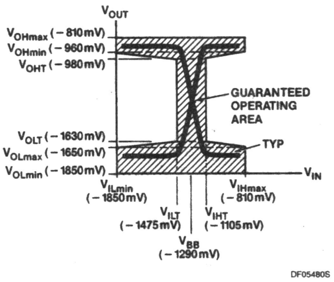
**DC ELECTRICAL CHARACTERISTICS** $V_{CC1} = V_{CC2} =$ GND, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$, output loading with 50Ω to $-2.0V \pm 0.010V$ unless otherwise specified[1,3]

| PARAMETER | | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | | $T_A = -30°C$ | −1060 | | −890 | mV | For $Q_n$ outputs, apply $V_{ILmin}$ to CP, $S_0$, and $S_1$ inputs. After applying $V_{IHmax}$ to all other inputs, change the CP input from $V_{ILmin}$ to $V_{IHmax}$.<br>For $\overline{C}_{OUT}$, apply $V_{ILmin}$ to CP, $\overline{C}_{IN}$, $S_0$, and $S_1$ inputs. After applying $V_{IHmax}$ to $D_n$ inputs, change CP from $V_{ILmin}$ to $V_{IHmax}$ then change $S_0$ and $\overline{C}_{IN}$ from $V_{ILmin}$ to $V_{IHmax}$. |
| | | | $T_A = +25°C$ | −960 | | −810 | mV | |
| | | | $T_A = +85°C$ | −890 | | −700 | mV | |
| $V_{OHT}$ | HIGH level output threshold voltage | | $T_A = -30°C$ | −1080 | | | mV | For $Q_0$ output, apply $V_{IHT}$ to $D_0$ input and $V_{ILmin}$ to CP, $S_0$, $S_1$, and $D_1$, $D_2$, and $D_3$. Raise CP from $V_{ILmin}$ to $V_{IHmax}$ and measure $Q_0$. Repeat this process for $Q_1$, $Q_2$, and $Q_3$ by applying $V_{IHT}$ to $D_1$, $D_2$, and $D_3$, respectively, one at a time.<br>For $\overline{C}_{OUT}$, apply $V_{ILmin}$ to CP, $\overline{C}_{IN}$, $S_0$, and $S_1$ inputs. After applying $V_{IHmax}$ to $D_n$ inputs, change CP from $V_{ILmin}$ to $V_{IHT}$ then change $S_0$ and $\overline{C}_{IN}$ from $V_{ILmin}$ to $V_{IHmax}$. |
| | | | $T_A = +25°C$ | −980 | | | mV | |
| | | | $T_A = +85°C$ | −910 | | | mV | |
| $V_{OLT}$ | LOW level output threshold voltage | | $T_A = -30°C$ | | | −1655 | mV | For $Q_n$ outputs, apply $V_{ILmin}$ to $D_n$ inputs and to CP, $S_0$, and $S_1$ inputs. Raise CP from $V_{ILmin}$ to $V_{IHT}$ and measure $Q_n$ outputs.<br>For $\overline{C}_{OUT}$, apply $V_{ILT}$ to CP, $\overline{C}_{IN}$, $S_0$, and $S_1$ inputs. After applying $V_{IHmax}$ to $D_n$ inputs, change CP from $V_{ILmin}$ to $V_{IHmax}$ and measure $\overline{C}_{OUT}$. |
| | | | $T_A = +25°C$ | | | −1630 | mV | |
| | | | $T_A = +85°C$ | | | −1595 | mV | |
| $V_{OL}$ | LOW level output voltage | | $T_A = -30°C$ | −1890 | | −1675 | mV | For $Q_n$ outputs, apply $V_{ILmin}$ to $D_n$ inputs and to CP, $S_0$, and $S_1$ inputs. Raise CP from $V_{ILmin}$ to $V_{IHmax}$ and measure $Q_n$ outputs.<br>For $\overline{C}_{OUT}$, apply $V_{ILmin}$ to CP, $C_{IN}$, $S_0$ and $S_1$ inputs. After applying $V_{IHmax}$ to $D_n$ inputs, change CP from $V_{ILmin}$ to $V_{IHmax}$ and measure $\overline{C}_{OUT}$. |
| | | | $T_A = +25°C$ | −1850 | | −1650 | mV | |
| | | | $T_A = +85°C$ | −1825 | | −1615 | mV | |
| $I_{IH}$ | HIGH level input current | $D_n$ inputs | $T_A = -30°C$ | | | 350 | μA | Apply $V_{IHmax}$ to each input under test, one at a time, with $V_{IHmax}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | | | 220 | μA | |
| | | | $T_A = +85°C$ | | | 220 | μA | |
| | | $S_0$, $\overline{C}_{IN}$ inputs | $T_A = -30°C$ | | | 390 | μA | |
| | | | $T_A = +25$ | | | 245 | μA | |
| | | | $T_A = +85$ | | | 245 | μA | |
| | | $S_1$ input | $T_A = -30°C$ | | | 425 | μA | |
| | | | $T_A = +25$ | | | 265 | μA | |
| | | | $T_A = +85°C$ | | | 265 | μA | |
| | | CP input | $T_A = -30°C$ | | | 460 | μA | |
| | | | $T_A = +25°C$ | | | 290 | μA | |
| | | | $T_A = +85°C$ | | | 290 | μA | |
| $I_{IL}$ | LOW level input current | | $T_A = -30°C$ | 0.5 | | | μA | Apply $V_{ILmin}$ to each input under test, one at a time, with $V_{IHmax}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | 0.5 | | | μA | |
| | | | $T_A = +85°C$ | 0.3 | | | μA | |
| $I_{EE}$ | $V_{EE}$ supply current | | $T_A = -30°C$ | | | 165 | mA | |
| | | | $T_A = +25°C$ | | 120 | 150 | mA | |
| | | | $T_A = +85°C$ | | | 165 | mA | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst-case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 4.

# Universal Counter 10137



$V_{IHmax}$ – Maximum HIGH level input voltage (the most positive $V_{IH}$).
$V_{IHT}$ – HIGH level input threshold voltage.
$V_{ILT}$ – LOW level input threshold voltage.
$V_{ILmin}$ – Minimum LOW level input voltage (the most negative $V_{IL}$).
$V_{OHmax}$ – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition.
$V_{OHmin}$ – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition.
$V_{OHT}$ – HIGH level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLT}$ – LOW level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLmax}$ – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions.
$V_{OLmin}$ – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions.
$V_{BB}$ – Reference bias voltage. The internally generated reference voltage which is used to set the input and output threshold level.

**Figure 4. Transfer Characteristics**

## AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$

| PARAMETER | $T_A = -30°C$ | | $T_A = +25°C$ | | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Typ | Max | Min | Max | | |
| $f_{MAX}$ Maximum clock frequency | 125 | | 125 | 150 | | 125 | | MHz | Figs. 5, 8, 9 |
| $t_{PLH}$ Propagation delay | 0.8 | 4.8 | 1.0 | 3.3 | 4.5 | 1.1 | 5.0 | ns | |
| $t_{PHL}$ CP to $Q_n$ | 0.8 | 4.8 | 1.0 | 3.3 | 4.5 | 1.1 | 5.0 | ns | |
| $t_{PLH}$ Propagation delay | 2.0 | 10.9 | 2.5 | 7.0 | 10.5 | 2.4 | 11.5 | ns | |
| $t_{PHL}$ CP to $\overline{C}_{OUT}$ | 2.0 | 10.9 | 2.5 | 7.0 | 10.5 | 2.4 | 11.5 | ns | |
| $t_{PLH}$ Propagation delay | 1.6 | 7.4 | 1.6 | 5.0 | 6.9 | 1.9 | 7.5 | ns | |
| $t_{PHL}$ $\overline{C}_{IN}$ to $\overline{C}_{OUT}$ | 1.6 | 7.4 | 1.6 | 5.0 | 6.9 | 1.9 | 7.5 | ns | |
| $t_s$ Setup time $D_n$ to CP | 3.5 | | 3.5 | | | 3.5 | | ns | Figs. 6, 8, 9 |
| $t_h$ Hold time CP to $D_n$ | 0.0 | | 0.0 | | | 0.0 | | ns | |
| $t_s$ Setup time $S_n$ to CP | 7.5 | | 7.5 | | | 7.5 | | ns | |
| $t_h$ Hold time CP to $S_n$ | −2.5 | | −2.5 | | | −2.5 | | ns | |
| $t_s$ Setup time $\overline{C}_{IN}$ to CP | 4.5 | | 3.7 | | | 4.5 | | ns | Figs. 7, 8, 9 |
| $t_h$ Hold time CP to $\overline{C}_{IN}$ | −1.6 | | −1.6 | | | −1.6 | | ns | |
| $t_s$ Setup time CP to $\overline{C}_{IN}$ | −1.0 | | −1.0 | | | −1.0 | | ns | |
| $t_h$ Hold time $\overline{C}_{IN}$ to CP | 4.0 | | 3.1 | | | 4.0 | | ns | |
| $t_{TLH}$ Transition time | 0.9 | 3.3 | 1.1 | 2.0 | 3.3 | 1.1 | 3.5 | ns | Figs. 5, 8, 9 |
| $t_{THL}$ 20% to 80%, 80% to 20% | 0.9 | 3.3 | 1.1 | 2.0 | 3.3 | 1.1 | 3.5 | ns | |

## AC WAVEFORMS

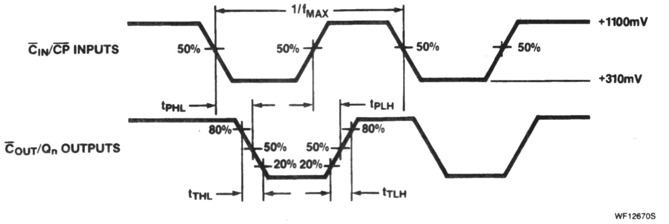

1/fMAX
C̄IN/C̄P INPUTS
50%
50%
50%
50%
+1100mV
+310mV
tPHL
tPLH
C̄OUT/Qn OUTPUTS
80%
50%
50%
20%
20%
80%
tTHL
tTLH
WF12670S

Figure 5. Propagation Delay and Transition Times for CP to $Q_n$ and $\overline{C}_{IN}$ to $\overline{C}_{OUT}$

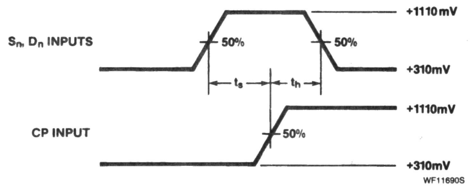
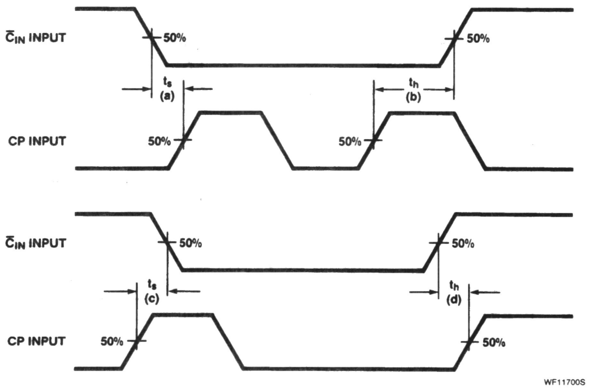

Sn, Dn INPUTS
50%
50%
+1110mV
+310mV
ts
th
CP INPUT
50%
+1110mV
+310mV
WF11690S

Figure 6. Setup and Hold Times for Data and Select to Clock

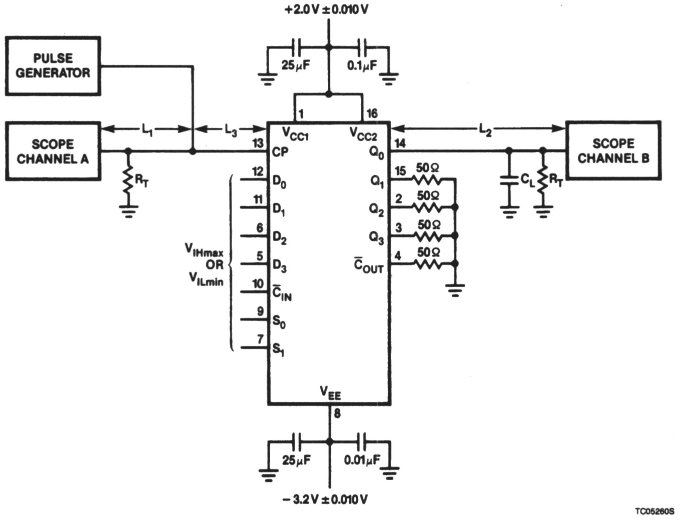

C̄IN INPUT
50%
50%
ts
(a)
th
(b)
CP INPUT
50%
50%
C̄IN INPUT
50%
50%
ts
(c)
th
(d)
CP INPUT
50%
50%
WF11700S

**NOTES:**
(a) is the minimum time to wait to clock the counter after it is enabled.
(b) is the minimum time that the counter may be clocked before it is disabled.
(c) is the minimum time that a clock pulse may be applied with no effect on the state of the counter before it is enabled.
(d) is the minimum time to wait before a clock pulse may be applied with no effect on the state of the counter after it is disabled.
(b) and (c) may be negative numbers.

Figure 7. Setup and Hold Times for $\overline{C}_{IN}$ to CP

# Universal Counter 10137

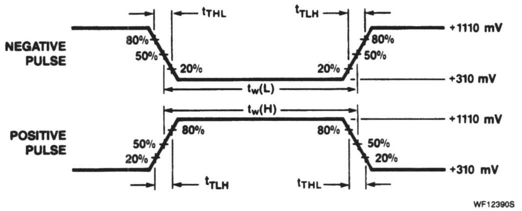
## TEST CIRCUITS AND WAVEFORMS


+2.0V ±0.010V
25μF
0.1μF
1
16
PULSE GENERATOR
SCOPE CHANNEL A
L1
L3
L2
13
CP
VCC1
VCC2
14
Q0
SCOPE CHANNEL B
RT
CL
RT
12
D0
11
D1
6
D2
5
D3
10
C̄IN
9
S0
7
S1
VIHmax OR VILmin
15
Q1
2
Q2
3
Q3
4
C̄OUT
50Ω
50Ω
50Ω
50Ω
VEE
8
25μF
0.01μF
−3.2V ±0.010V
TC05260S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V$ ±0.010V, $V_{EE} = -3.2V$ ±0.010V.
2. Decoupling 0.1μF and 25μF from GND to $V_{CC}$, 0.01μF from GND to $V_{EE}$ (0.01 and 0.1uF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than ¼ inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin and the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed ¼ inch (6mm).
6. $R_T = 50\Omega$ terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than ¼ inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance $\leqslant 3pF$.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed ¼ inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ±1% or better.

Figure 8. AC Test Circuit for 10137


NEGATIVE PULSE
tTHL
tTLH
80%
50%
20%
20%
80%
50%
+1110 mV
+310 mV
tw(L)
tw(H)
POSITIVE PULSE
80%
80%
50%
20%
50%
20%
+1110 mV
+310 mV
tTLH
tTHL
WF12390S

| INPUT PULSE REQUIREMENTS<br>$V_{CC1} = V_{CC2} = +2.0V$ ±0.010V, $V_{EE} = -3.2V$ ±0.010V, $V_T$ = GND (0V) | | | | | |
|---|---|---|---|---|---|
| Family | Amplitude | Rep Rate | Pulse Width | $t_{TLH}$ | $t_{THL}$ |
| 10K ECL | 800mVp-p | 1MHz | 500ns | 2.0 ±0.2ns | 2.0 ±0.2ns |

Figure 9. Input Pulse Definition

# 10141
## Shift Register

**4-Bit Universal Shift Register**
***Product Specification***

**ECL Products**

## DESCRIPTION

The 10141 is a four-bit serial-/parallel-out shift register. Inputs $S_0$ and $S_1$ are used to determine the four possible functions of the register, these being no shift, shift left, and parallel entrance of data with no external gating of the clock. The other inputs $D_R$ and $D_L$ are intended for shifting in from the left and the right, while inputs $D_0$ to $D_3$ are normal data inputs. All four outputs are capable of driving 50Ω lines. When the register is operating for serial output only, the unused outputs may be left open. All unused inputs must be tied LOW to $V_{IL}$ or $V_{EE}$.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 10141 | 2.9ns | 82mA |

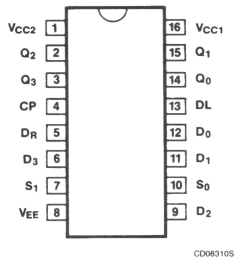
## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} =$ GND; $V_{EE} = -5.2V$<br>$T_A = -30°C$ to $+85°C$ |
|---|---|
| Plastic DIP | 10141N |
| Ceramic DIP | 10141F |

## PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_0 - D_3$ | Data Inputs |
| CP | Clock Input |
| $S_0$, $S_1$ | Select Inputs |
| DR | Serial Shift Right Register |
| DL | Serial Shift Left Register |
| $Q_0 - Q_3$ | Data Outputs |

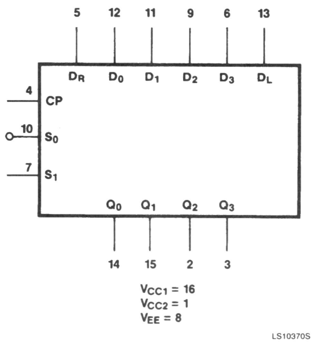
## PIN CONFIGURATION



$V_{CC2}$ 1
$Q_2$ 2
$Q_3$ 3
CP 4
$D_R$ 5
$D_3$ 6
$S_1$ 7
$V_{EE}$ 8
16 $V_{CC1}$
15 $Q_1$
14 $Q_0$
13 DL
12 $D_0$
11 $D_1$
10 $S_0$
9 $D_2$
CD08310S

Figure 1

## LOGIC SYMBOL



5
12
11
9
6
13
$D_R$
$D_0$
$D_1$
$D_2$
$D_3$
$D_L$
4
CP
10
$S_0$
7
$S_1$
$Q_0$
$Q_1$
$Q_2$
$Q_3$
14
15
2
3
$V_{CC1}$ = 16
$V_{CC2}$ = 1
$V_{EE}$ = 8
LS10370S

Figure 2

## Shift Register

## 10141

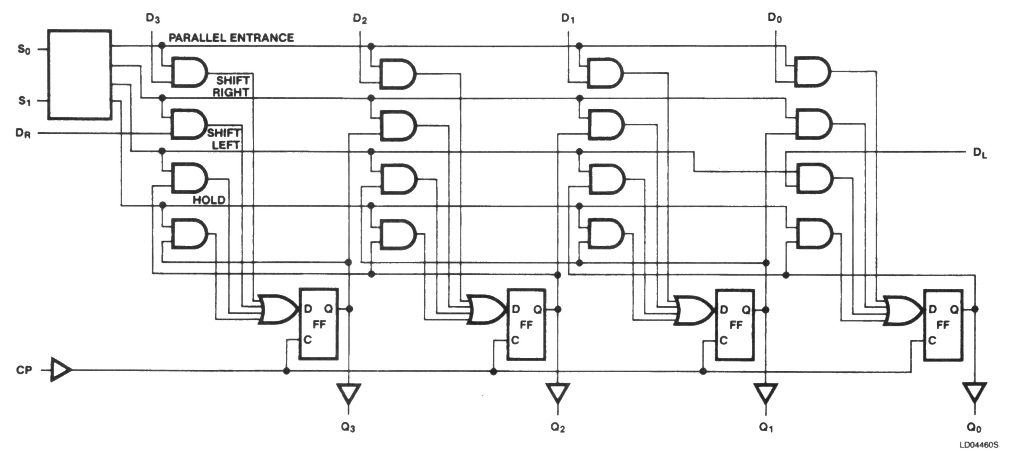

D3
D2
D1
D0
PARALLEL ENTRANCE
SHIFT RIGHT
SHIFT LEFT
HOLD
S0
S1
DR
DL
D Q
FF
C
D Q
FF
C
D Q
FF
C
D Q
FF
C
CP
Q3
Q2
Q1
Q0
LD04460S

Figure 3. Logic Diagram

## FUNCTION TABLE

| SELECT INPUTS | | OPERATION MODE | OUTPUTS | | |
|---|---|---|---|---|---|
| $S_1$ | $S_2$ | | $Q_{0(n+1)}$ | $Q_{1(n+1)}$ | $Q_{3(n+1)}$ |
| L | L | Parallel | $D_0$ | $D_1$ | $D_2$ |
| L | H | Shift right* | $Q_{1n}$ | $Q_{2n}$ | $Q_{3n}$ |
| H | L | Shift left* | DL | $Q_{0n}$ | $Q_{1n}$ |
| H | H | Stop shift | $Q_{0n}$ | $Q_{1n}$ | $Q_{2n}$ |

Positive Logic:
H = HIGH state (the more positive voltage) = 1
L = LOW state (the less positive voltage) = 0
* Outputs as they exist after pulse at "CP" input with conditions as shown.
Pulse is positive transition of clock (CP) input.

**ABSOLUTE MAXIMUM RATINGS** (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | | 10KECL | UNIT |
|---|---|---|---|---|
| $V_{EE}$ | Supply voltage | | −8.0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | | 0 to $V_{EE}$ | V |
| $I_O$ | Output source current | | −50 | mA |
| $T_S$ | Storage temperature | | −55 to +150 | °C |
| $T_J$ | Maximum junction temperature | Ceramic package | +165 | °C |
| | | Plastic package | +150 | °C |

**DC ELECTRICAL CHARACTERISTICS** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30^{\circ}C$ to $+85^{\circ}C$, output loading with 50Ω to $-2.0V \pm 0.010V$ unless otherwise specified[1,3]

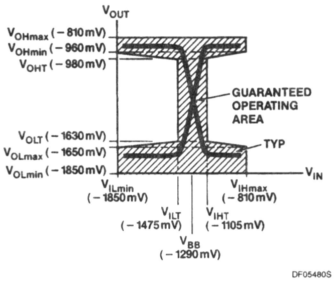
| PARAMETER | | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | | $T_A = -30^{\circ}C$ | -1060 | | -890 | mV | Apply $V_{IHmax}$ to CP input and $D_n$ inputs, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25^{\circ}C$ | -960 | | -810 | mV | |
| | | | $T_A = +85^{\circ}C$ | -890 | | -700 | mV | |
| $V_{OHT}$ | HIGH level output threshold voltage | | $T_A = -30^{\circ}C$ | -1080 | | | mV | Apply $V_{IHT}$ to CP input. Apply $V_{IHmax}$ to $D_n$ inputs, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25^{\circ}C$ | -980 | | | mV | |
| | | | $T_A = +85^{\circ}C$ | -910 | | | mV | |
| $V_{OLT}$ | LOW level output threshold voltage | | $T_A = -30^{\circ}C$ | | | -1655 | mV | Apply $V_{IHT}$ to CP input with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25^{\circ}C$ | | | -1630 | mV | |
| | | | $T_A = +85^{\circ}C$ | | | -1595 | mV | |
| $V_{OLT}$ | LOW level output voltage | | $T_A = -30^{\circ}C$ | -1890 | | -1675 | mV | Apply $V_{IHmax}$ to CP input with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25^{\circ}C$ | -1850 | | -1650 | mV | |
| | | | $T_A = +85^{\circ}C$ | -1825 | | -1515 | mV | |
| $I_{IH}$ | HIGH level input current | $D_n$, $D_R$ $D_L$ inputs | $T_A = -30^{\circ}C$ | | | 350 | μA | Apply $V_{IHmax}$ to each input under test, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25^{\circ}C$ | | | 200 | μA | |
| | | | $T_A = +85^{\circ}C$ | | | 200 | μA | |
| | | $S_0$, $S_1$ input | $T_A = -30^{\circ}C$ | | | 390 | μA | |
| | | | $T_A = +25^{\circ}C$ | | | 245 | μA | |
| | | | $T_A = +85^{\circ}C$ | | | 245 | μA | |
| | | CP input | $T_A = -30^{\circ}C$ | | | 425 | μA | Apply $V_{IHmax}$ to CP input with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25^{\circ}C$ | | | 265 | μA | |
| | | | $T_A = +85^{\circ}C$ | | | 265 | μA | |
| $I_{IL}$ | LOW level input current | | $T_A = -30^{\circ}C$ | 0.5 | | | μA | Apply $V_{ILmin}$ to each input under test one at a time with $V_{IHmax}$ applied to all other inputs. |
| | | | $T_A = +25^{\circ}C$ | 0.5 | | | μA | |
| | | | $T_A = +85^{\circ}C$ | 0.3 | | | μA | |
| $-I_{EE}$ | $V_{EE}$ supply current | | $T_A = -30^{\circ}C$ | | | 112 | mA | |
| | | | $T_A = +25^{\circ}C$ | | 82 | 102 | mA | |
| | | | $T_A = +85^{\circ}C$ | | | 112 | mA | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst-case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 4.

## Shift Register

## 10141



$V_{IHmax}$ – Maximum HIGH level input voltage (the most positive $V_{IH}$).
$V_{IHT}$ – HIGH level input threshold voltage.
$V_{ILT}$ – LOW level input threshold voltage.
$V_{ILmin}$ – Minimum LOW level input voltage (the most negative $V_{IL}$).
$V_{OHmax}$ – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition.
$V_{OHmin}$ – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition.
$V_{OHT}$ – HIGH level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLT}$ – LOW level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLmax}$ – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions.
$V_{OLmin}$ – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions.
$V_{BB}$ – Reference bias voltage. The internally generated reference voltage which is used to set the input and output threshold level.

**Figure 4. Transfer Characteristics**

## AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$

| PARAMETER | | $T_A = -30°C$ | | $T_A = +25°C$ | | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Typ | Max | Min | Max | | |
| $f_{MAX}$ | Maximum clock frequency | 150 | | 150 | 200 | | 150 | | MHz | Figs. 5, 8, 9 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$D_n$ to $Q_n$ | 1.7<br>1.7 | 3.9<br>3.9 | 1.8<br>1.8 | 2.9<br>2.9 | 3.8<br>3.8 | 2.0<br>2.0 | 4.2<br>4.2 | ns<br>ns | Figs. 5, 7, 9 |
| $t_s$ | Setup time $D_n$ to CP | 2.5 | | 2.5 | | | 2.5 | | ns | Figs. 6, 7, 9 |
| $t_h$ | Hold time CP to $D_n$ | 1.5 | | 1.5 | | | 1.5 | | ns | |
| $t_s$ | Setup time $S_n$ to CP | 5.5 | | 5.0 | | 5.5 | | | ns | |
| $t_h$ | Hold time CP to $S_n$ | 1.5 | | 1.5 | | | 1.5 | | ns | |
| $t_{TLH}$<br>$t_{THL}$ | Transition time<br>20% to 80%, 80% to 20% | 1.0<br>1.0 | 3.4<br>3.4 | 1.1<br>1.1 | 2.0<br>2.0 | 3.3<br>3.3 | 1.1<br>1.1 | 3.6<br>3.6 | ns<br>ns | Figs. 5, 7, 9 |

## AC WAVEFORMS

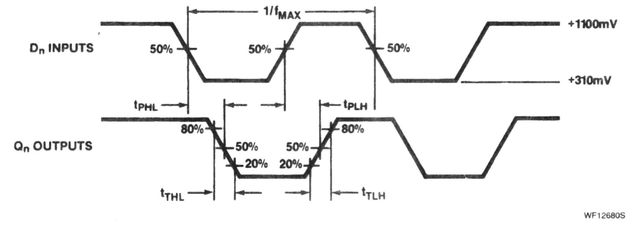

1/$f_{MAX}$
$D_n$ INPUTS
50%
50%
50%
+1100mV
+310mV
$t_{PHL}$
$t_{PLH}$
$Q_n$ OUTPUTS
80%
50%
20%
50%
20%
80%
$t_{THL}$
$t_{TLH}$
WF12680S

Figure 5. Propagation Delay and Transition Times for $D_n$ to $Q_n$ and Maximum Clock Frequency

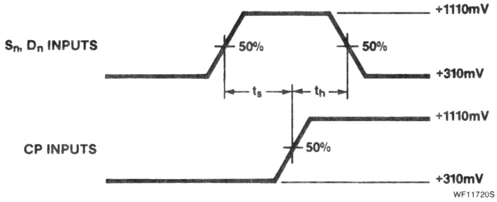
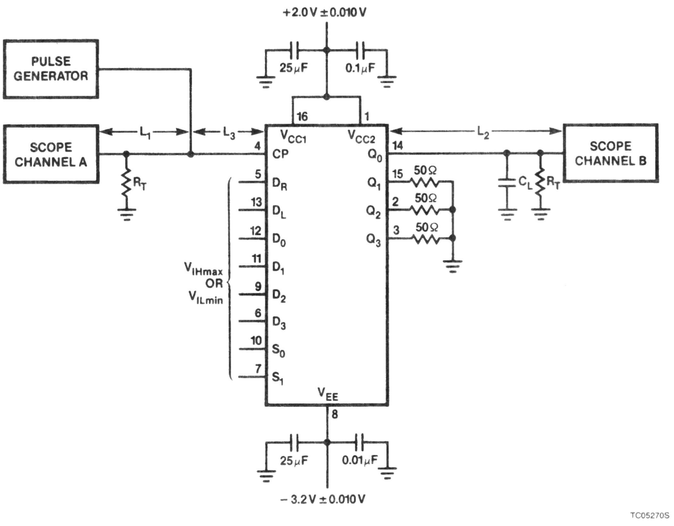

$S_n$, $D_n$ INPUTS
50%
50%
+1110mV
+310mV
$t_s$
$t_h$
CP INPUTS
50%
+1110mV
+310mV
WF11720S

Figure 6. Setup and Hold Times for Data and Select to Clock

## TEST CIRCUITS AND WAVEFORMS


+2.0V ±0.010V
25µF
0.1µF
PULSE GENERATOR
SCOPE CHANNEL A
$L_1$
$L_3$
$R_T$
16
1
$V_{CC1}$
$V_{CC2}$
4 CP
14 $Q_0$
5 $D_R$
13 $D_L$
12 $D_0$
11 $D_1$
9 $D_2$
6 $D_3$
10 $S_0$
7 $S_1$
15 $Q_1$
2 $Q_2$
3 $Q_3$
50Ω
50Ω
50Ω
$L_2$
SCOPE CHANNEL B
$C_L$
$R_T$
$V_{IHmax}$ OR $V_{ILmin}$
$V_{EE}$
8
25µF
0.01µF
−3.2V ±0.010V
TC05270S

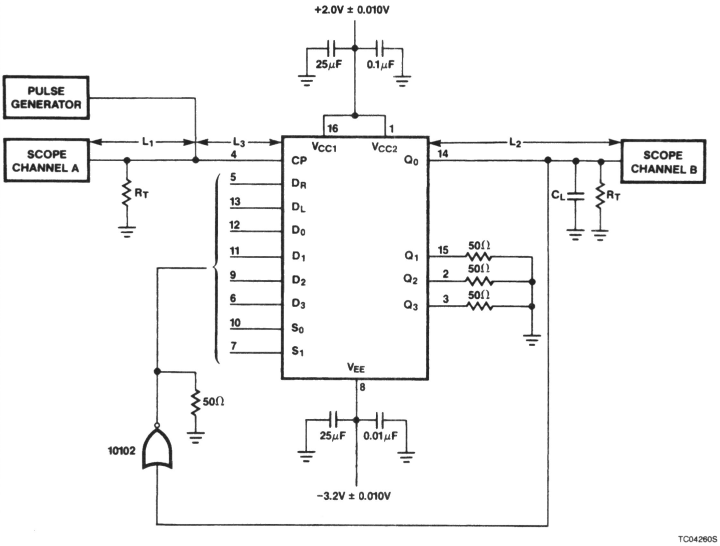
**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1µF and 25µF from GND to $V_{CC}$, 0.01µF from GND to $V_{EE}$ (0.01 and 0.1uF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than ¼ inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin and the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed ¼ inch (6mm).
6. $R_T = 50\Omega$ terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than ¼ inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance $\leqslant 3pF$.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed ¼ inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.

Figure 7. AC Test Circuit for 10141

# Shift Register

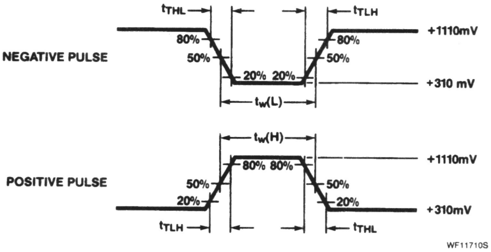
# 10141


+2.0V ± 0.010V
25μF
0.1μF
PULSE GENERATOR
SCOPE CHANNEL A
L1
L3
L2
16
1
4
14
VCC1
VCC2
CP
Q0
SCOPE CHANNEL B
RT
CL
RT
5
DR
13
DL
12
D0
11
D1
9
D2
6
D3
10
S0
7
S1
Q1
Q2
Q3
15
2
3
50Ω
50Ω
50Ω
VEE
8
50Ω
10102
25μF
0.01μF
-3.2V ± 0.010V
TC04260S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1μF and 25μF from GND to $V_{CC}$, 0.01μF from GND to $V_{EE}$ (0.01 and 0.1uF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than ¼ inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin and the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed ¼ inch (6mm).
6. $R_T = 50\Omega$ terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than ¼ inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance $\leqslant 3pF$.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed ¼ inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.

Figure 8. Clock Frequency Test Circuit for 10141


NEGATIVE PULSE
tTHL
tTLH
80%
50%
20%
20%
80%
50%
+1110mV
+310 mV
tw(L)
POSITIVE PULSE
tw(H)
80%
80%
50%
20%
50%
20%
+1110mV
+310mV
tTLH
tTHL
WF11710S

**INPUT PULSE REQUIREMENTS**
$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$, $V_T = GND$ (0V)

| Family | Amplitude | Rep Rate | Pulse Width | $t_{TLH}$ | $t_{THL}$ |
|---|---|---|---|---|---|
| 10K ECL | 800mVp-p | 1MHz | 500ns | 2.0 ±0.2ns | 2.0 ±0.2ns |

Figure 9. Input Pulse Definition

Signetics

# 10158
# Multiplexer

**Quad 2-to-1 Multiplexer, Non-Inverting**
***Product Specification***

**ECL Products**

## DESCRIPTION

The 10158 is a high-speed, low power, Quad 2-to-1 Multiplexer. With respect to a single control signal(s), it transmits to a common output pin the data present on either of two input pins.

As contrasted with the 10159, the 10158 has no enable input and non-inverting outputs. All unused inputs can be left open due to integrated pull-down resistors which avoid the need for a supply voltage.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 10158 | 2.5ns | 38mA |

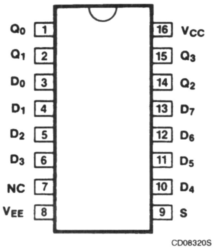
## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} = GND$; $V_{EE} = -5.2V$<br>$T_A = -30°C$ to $+85°C$ |
|---|---|
| Plastic DIP | 10158N |
| Ceramic DIP | 10158F |

## PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_0 - D_7$ | Data Inputs |
| S | Select Input |
| $Q_0 - Q_3$ | Data Outputs |

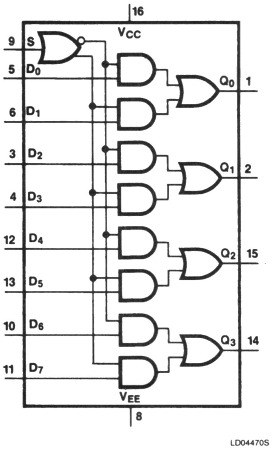
## PIN CONFIGURATION



Q0 1
Q1 2
D0 3
D1 4
D2 5
D3 6
NC 7
VEE 8
16 VCC
15 Q3
14 Q2
13 D7
12 D6
11 D5
10 D4
9 S
CD08320S

Figure 1

## LOGIC SYMBOL



16
VCC
9 S
5 D0
6 D1
3 D2
4 D3
12 D4
13 D5
10 D6
11 D7
Q0 1
Q1 2
Q2 15
Q3 14
VEE
8
LD04470S

Figure 2

# Multiplexer

# 10158

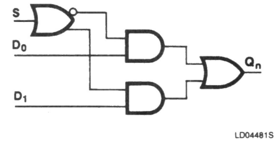


**Figure 3. Logic Function (One Multiplexer)**

## FUNCTION TABLE

| INPUTS | | | OUTPUT |
|---|---|---|---|
| $D_0$ | $D_1$ | S | $Q_0$ |
| L | X | L | L |
| H | X | L | H |
| X | L | H | L |
| X | H | H | H |

Positive Logic:
H = HIGH state (the more positive voltage) = 1
L = LOW state (the less positive voltage) = 0
X = Don't Care

## ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | | 10K ECL | UNIT |
|---|---|---|---|---|
| $V_{EE}$ | Supply voltage | | -8.0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | | 0 to $V_{EE}$ | V |
| $I_O$ | Output current | | -50 | mA |
| $T_S$ | Storage temperature | | -55 to +150 | °C |
| $T_J$ | Maximum junction temperature | Ceramic package | +165 | °C |
| | | Plastic package | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | 10K ECL | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | -5.2 | | V |
| $V_{IH}$ | HIGH level input voltage | $T_A = -30°C$ | | | -890 | mV |
| | | $T_A = +25°C$ | | | -810 | mV |
| | | $T_A = +85°C$ | | | -700 | mV |
| $V_{IHT}$ | HIGH level input threshold voltage | $T_A = -30°C$ | -1205 | | | mV |
| | | $T_A = +25°C$ | -1105 | | | mV |
| | | $T_A = +85°C$ | -1035 | | | mV |
| $V_{ILT}$ | LOW level input threshold voltage | $T_A = -30°C$ | | | -1500 | mV |
| | | $T_A = +25°C$ | | | -1475 | mV |
| | | $T_A = +85°C$ | | | -1440 | mV |
| $V_{IL}$ | LOW level input voltage | $T_A = -30°C$ | -1890 | | | mV |
| | | $T_A = +25°C$ | -1850 | | | mV |
| | | $T_A = +85°C$ | -1825 | | | mV |
| $T_A$ | Operating ambient temperature | | -30 | +25 | +85 | °C |

**NOTE:**
When operating at $V_{EE}$ other than specified voltage (-5.2V), the DC and AC Characteristics will vary slightly from specified values. (See table of DC Characteristics)

# Multiplexer

# 10158

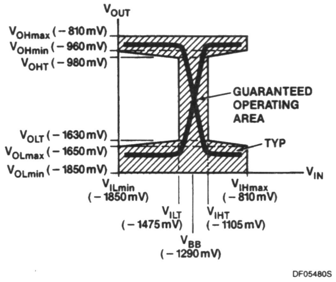
**DC ELECTRICAL CHARACTERISTICS** $V_{CC}$ = GND, $V_{EE}$ = −5.2V ±0.010V, $T_A$ = −30°C to +85°C, output loading with 50Ω to −2.0V ±0.010V unless otherwise specified[1, 3]

| PARAMETER | | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | | $T_A$ = −30°C | −1060 | | −890 | mV | For even inputs, apply $V_{ILmin}$ to S input with $V_{IHmax}$ applied to all other inputs.<br>For odd inputs, apply $V_{IHmax}$ to all inputs. |
| | | | $T_A$ = +25°C | −960 | | −810 | mV | |
| | | | $T_A$ = +85°C | −890 | | −700 | mV | |
| $V_{OHT}$ | HIGH level output threshold voltage | | $T_A$ = −30°C | −1080 | | | mV | Apply $V_{IHT}$ to $D_0$ input with $V_{ILmin}$ applied to S input. Repeat for each even input.<br>Apply $V_{IHT}$ to $D_1$ input with $V_{IHmax}$ applied to S input.Repeat for each odd input. |
| | | | $T_A$ = +25°C | −980 | | | mV | |
| | | | $T_A$ = +85°C | −910 | | | mV | |
| $V_{OLT}$ | LOW level output threshold voltage | | $T_A$ = −30°C | | | −1655 | mV | Apply $V_{ILT}$ to $D_0$ input with $V_{ILmin}$ applied to S input. Repeat for each even input.<br>Apply $V_{ILT}$ to $D_1$ input with $V_{IHmax}$ applied to S input.Repeat for each odd input. |
| | | | $T_A$ = +25°C | | | −1630 | mV | |
| | | | $T_A$ = +85°C | | | −1595 | mV | |
| $V_{OL}$ | LOW level output voltage | | $T_A$ = −30°C | −1890 | | −1675 | mV | For even inputs, apply $V_{ILmin}$ to all inputs.<br>For odd inputs, apply $V_{IHmax}$ to S input and $V_{ILmin}$ to all other inputs. |
| | | | $T_A$ = +25°C | −1850 | | −1650 | mV | |
| | | | $T_A$ = +85°C | −1825 | | −1615 | mV | |
| $I_{IH}$ | HIGH level input current | S input | $T_A$ = −30°C | | | 360 | μA | Apply $V_{IHmax}$ to S input with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A$ = +25°C | | | 225 | μA | |
| | | | $T_A$ = +85°C | | | 225 | μA | |
| | | Other inputs | $T_A$ = −30°C | | | 400 | μA | For even inputs, apply $V_{IHmax}$ to input under test, one at a time, with $V_{ILmin}$ applied to all other inputs.<br>For odd inputs, apply $V_{IHmax}$ to S input and to input under test, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A$ = +25°C | | | 250 | μA | |
| | | | $T_A$ = +85°C | | | 250 | μA | |
| $I_{IL}$ | LOW level input current | | $T_A$ = −30°C | 0.5 | | | μA | Apply $V_{ILmin}$ to each input under test, one at a time, with $V_{IHmax}$ applied to all other inputs. |
| | | | $T_A$ = +25°C | 0.5 | | | μA | |
| | | | $T_A$ = +85°C | 0.3 | | | μA | |
| $-I_{EE}$ | $V_{EE}$ supply current | | $T_A$ = −30°C | | | 53 | mA | |
| | | | $T_A$ = +25°C | | 38 | 46 | mA | |
| | | | $T_A$ = +85°C | | | 53 | mA | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | | $T_A$ = +25°C | | 0.016 | | V/V | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | | 0.250 | | V/V | |
| $\frac{\Delta V_{BB}}{\Delta V_{EE}}$ | Reference bias voltage compensation | | | | 0.148 | | V/V | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst-case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 4.

# Multiplexer 10158



$V_{OUT}$
$V_{OHmax}$ (−810mV)
$V_{OHmin}$ (−960mV)
$V_{OHT}$ (−980mV)
GUARANTEED OPERATING AREA
$V_{OLT}$ (−1630mV)
TYP
$V_{OLmax}$ (−1650mV)
$V_{OLmin}$ (−1850mV)
$V_{IN}$
$V_{ILmin}$ (−1850mV)
$V_{IHmax}$ (−810mV)
$V_{ILT}$ (−1475mV)
$V_{IHT}$ (−1105mV)
$V_{BB}$ (−1290mV)
DF05480S

**NOTES:**

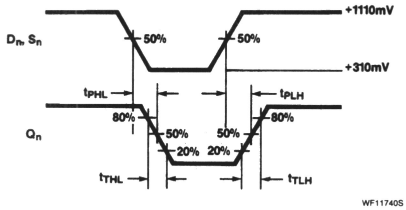
$V_{IHmax}$ – Maximum HIGH level input voltage (the most positive $V_{IH}$).
$V_{IHT}$ – HIGH level input threshold voltage.
$V_{ILT}$ – LOW level input threshold voltage.
$V_{ILmin}$ – Minimum LOW level input voltage (the most negative $V_{IL}$).
$V_{OHmax}$ – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition.
$V_{OHmin}$ – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition.
$V_{OHT}$ – HIGH level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLT}$ – LOW level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLmax}$ – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions.
$V_{OLmin}$ – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions.
$V_{BB}$ – Reference bias voltage. The internally generated reference voltage which is used to set the input and output threshold level.

Figure 4. Transfer Characteristics

## AC ELECTRICAL CHARACTERISTICS $V_{CC} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$

| PARAMETER | $T_A = -30°C$ | | $T_A = +25°C$ | | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Typ | Max | Min | Max | | |
| $t_{PLH}$ Propagation delay<br>$t_{PHL}$ $D_n$ to $Q_n$ | 1.3 | 3.1 | 1.2 | 2.5 | 3.0 | 1.3 | 3.2 | ns | Figs. 5, 6, 7 |
| $t_{PLH}$ Propagation delay<br>$t_{PHL}$ S to $Q_n$ | 2.5 | 4.8 | 2.4 | 3.2 | 4.5 | 2.5 | 4.8 | ns | Figs. 5, 6, 7 |
| $t_{TLH}$ Transition time<br>$t_{THL}$ 20% to 80%, 80% to 20% | 1.6<br>1.6 | 3.4<br>3.4 | 1.5<br>1.5 | 2.5<br>2.5 | 3.3<br>3.3 | 1.6<br>1.6 | 3.4<br>3.4 | ns<br>ns | Figs. 5, 6, 7 |

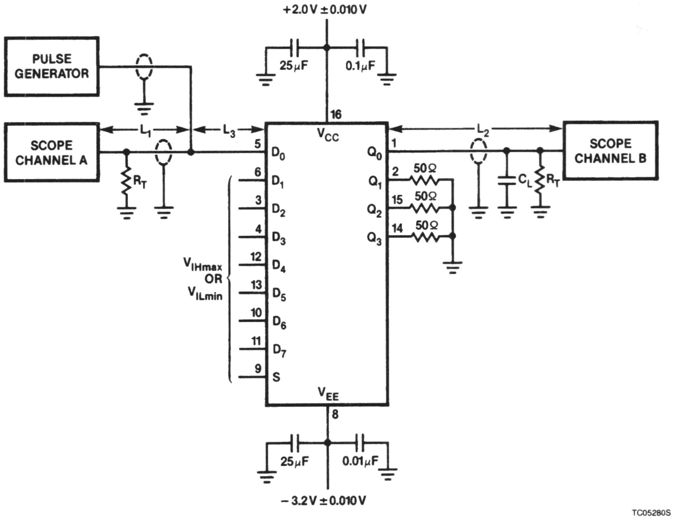
## AC WAVEFORMS



+1110mV
$D_n, S_n$
50%
50%
+310mV
$t_{PHL}$
$t_{PLH}$
80%
80%
$Q_n$
50%
50%
20%
20%
$t_{THL}$
$t_{TLH}$
WF11740S

Figure 5. Propagation Delay and Transition Times

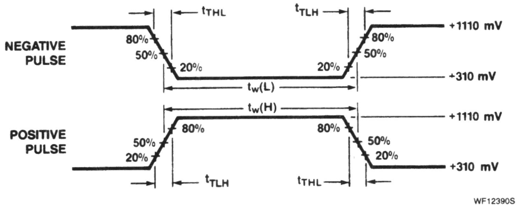
## TEST CIRCUITS AND WAVEFORMS


+2.0 V ± 0.010 V
25μF
0.1μF
PULSE GENERATOR
SCOPE CHANNEL A
L1
L3
R_T
16
V_CC
5 D0
6 D1
3 D2
4 D3
12 D4
13 D5
10 D6
11 D7
9 S
V_IHmax OR V_ILmin
Q0 1
Q1 2
Q2 15
Q3 14
50Ω
50Ω
50Ω
L2
C_L
R_T
SCOPE CHANNEL B
V_EE
8
25μF
0.01μF
−3.2V ± 0.010V
TC05280S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1μF and 25μF from GND to $V_{CC}$, 0.01μF and 25μF from GND to $V_{EE}$ (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than ¼ inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed ¼ inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than ¼ inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance ≤ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed ¼ inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.

Figure 6. AC Test Circuit


NEGATIVE PULSE
POSITIVE PULSE
t_THL
t_TLH
80%
50%
20%
t_w(L)
t_w(H)
+1110 mV
+310 mV
+1110 mV
+310 mV
WF12390S

| INPUT PULSE REQUIREMENTS<br>$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$, $V_T$ = GND (0V) | | | | | |
|---|---|---|---|---|---|
| **Family** | **Amplitude** | **Rep Rate** | **Pulse Width** | **$t_{TLH}$** | **$t_{THL}$** |
| 10K ECL | 800mVp-p | 1MHz | 500ns | 2.0 ± 0.2ns | 2.0 ± 0.2ns |

Figure 7. Input Pulse Definition

**Signetics**

# 10159
## Multiplexer

**Quad 2-to-1 Multiplexer, Inverting**
***Product Specification***

**ECL Products**

## DESCRIPTION

The 10159 is a high-speed, low power, Quad 2-to-1 Multiplexer.

With respect to a single control signal, (S), it transmits to a common output pin the data present on either of two input pins.

As contrasted with the 10158, the 10159 has a common output enable input ($\overline{OE}$) and inverting outputs.

All unused inputs can be left open due to integrated pull-down resistors which avoid the need for a supply voltage.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 10159 | 2.5ns | 42mA |

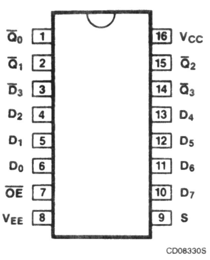
## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} = GND$; $V_{EE} = -5.2V$<br>$T_A = -30°C$ to $+85°C$ |
|---|---|
| Plastic DIP | 10159N |
| Ceramic DIP | 10159F |

## PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_0 - D_7$ | Data Inputs |
| S | Select Input |
| $\overline{OE}$ | Output Enable Input |
| $\overline{Q}_0 - \overline{Q}_3$ | Data Outputs |

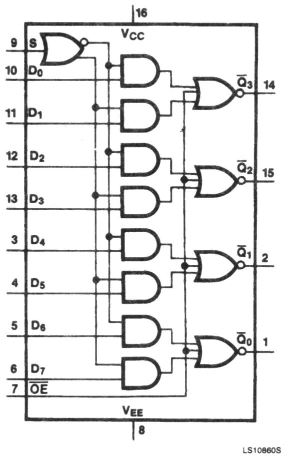
## PIN CONFIGURATION



$\overline{Q}_0$ 1
$\overline{Q}_1$ 2
$\overline{D}_3$ 3
$D_2$ 4
$D_1$ 5
$D_0$ 6
$\overline{OE}$ 7
$V_{EE}$ 8
16 $V_{CC}$
15 $\overline{Q}_2$
14 $\overline{Q}_3$
13 $D_4$
12 $D_5$
11 $D_6$
10 $D_7$
9 S
CD08330S

Figure 1

## LOGIC SYMBOL



16
$V_{CC}$
9 S
10 $D_0$
11 $D_1$
12 $D_2$
13 $D_3$
3 $D_4$
4 $D_5$
5 $D_6$
6 $D_7$
7 $\overline{OE}$
$V_{EE}$
8
$\overline{Q}_3$ 14
$\overline{Q}_2$ 15
$\overline{Q}_1$ 2
$\overline{Q}_0$ 1
LS10860S

Figure 2

## Multiplexer

## 10159

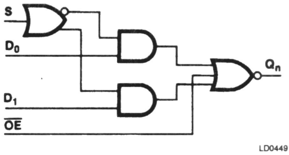


**Figure 3. Logic Diagram (One Multiplexer)**

### FUNCTION TABLE

| INPUTS | | | | OUTPUT |
|---|---|---|---|---|
| $D_0$ | $D_1$ | S | $\overline{OE}$ | $Q_0$ |
| X | X | X | H | L |
| L | X | L | L | H |
| H | X | L | L | L |
| X | L | H | L | H |
| X | H | H | L | L |

Positive Logic:
H = HIGH state (the more positive voltage) = 1
L = LOW state (the less positive voltage) = 0
X = Don't Care
0 means even numbers
1 means odd numbers

**ABSOLUTE MAXIMUM RATINGS** (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating case temperature range.)

| PARAMETER | | | 10K ECL | UNIT |
|---|---|---|---|---|
| $V_{EE}$ | Supply voltage | | -8.0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | | 0 to $V_{EE}$ | V |
| $I_O$ | Output source current | | -50 | mA |
| $T_S$ | Storage temperature | | -55 to +150 | °C |
| $T_J$ | Maximum junction temperature | Ceramic package | +165 | °C |
| | | Plastic package | +150 | °C |

### DC OPERATING CONDITIONS

| PARAMETER | | | 10K ECL | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | -5.2 | | V |
| $V_{IH}$ | HIGH level input voltage | $T_A$ = -30°C | | | -890 | mV |
| | | $T_A$ = +25°C | | | -810 | mV |
| | | $T_A$ = +85°C | | | -700 | mV |
| $V_{IHT}$ | HIGH level input threshold voltage | $T_A$ = -30°C | -1205 | | | mV |
| | | $T_A$ = +25°C | -1105 | | | mV |
| | | $T_A$ = +85°C | -1035 | | | mV |
| $V_{ILT}$ | LOW level input threshold voltage | $T_A$ = -30°C | | | -1500 | mV |
| | | $T_A$ = +25°C | | | -1475 | mV |
| | | $T_A$ = +85°C | | | -1440 | mV |
| $V_{IL}$ | LOW level input voltage | $T_A$ = -30°C | -1890 | | | mV |
| | | $T_A$ = +25°C | -1850 | | | mV |
| | | $T_A$ = +85°C | -1825 | | | mV |
| $T_A$ | Operating ambient temperature | | -30 | +25 | +85 | °C |

**NOTE:**
When operating at $V_{EE}$ other than specified voltage (-5.2V), the DC and AC Characteristics will vary slightly from specified values.
(See table of DC Characteristics)

# Multiplexer 10159

## DC ELECTRICAL CHARACTERISTICS

$V_{CC}$ = GND, $V_{EE}$ = −5.2V ±0.010V, $T_A$ = −30°C to +85°C, output loading with 50Ω to −2.0V ±0.010V unless otherwise specified[1,3]

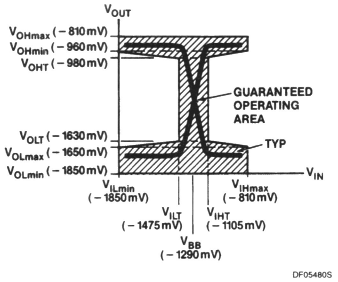
| PARAMETER | | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | | $T_A$ = −30°C | −1060 | | −890 | mV | For even inputs, apply $V_{ILmin}$ to all inputs.<br>For odd inputs, apply $V_{IHmax}$ to S input and $V_{ILmin}$ to all other inputs. |
| | | | $T_A$ = +25°C | −960 | | −810 | mV | |
| | | | $T_A$ = +85°C | −890 | | −700 | mV | |
| $V_{OHT}$ | HIGH level output threshold voltage | | $T_A$ = −30°C | −1080 | | | mV | For even inputs, apply $V_{ILT}$ to S input with $V_{ILmin}$ applied to all other inputs.<br>For odd inputs, apply $V_{IHT}$ to S input with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A$ = −25°C | −980 | | | mV | |
| | | | $T_A$ = −85°C | −910 | | | mV | |
| $V_{OLT}$ | LOW level output threshold voltage | | $T_A$ = −30°C | | | −1655 | mV | Apply $V_{IHT}$ to $\overline{OE}$ input with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A$ = −25°C | | | −1630 | mV | |
| | | | $T_A$ = −85°C | | | −1595 | mV | |
| $V_{OL}$ | LOW level output voltage | | $T_A$ = −30°C | −1890 | | −1675 | mV | Apply $V_{IHmax}$ to $\overline{OE}$ input with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A$ = +25°C | −1850 | | −1650 | mV | |
| | | | $T_A$ = +85°C | −1825 | | −1615 | mV | |
| $I_{IH}$ | HIGH level input current | S input | $T_A$ = −30°C | | | 360 | μA | Apply $V_{IHmax}$ to S input with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A$ = +25°C | | | 225 | μA | |
| | | | $T_A$ = +85°C | | | 225 | μA | |
| | | Other inputs | $T_A$ = −30°C | | | 400 | μA | Apply $V_{IHmax}$ to $\overline{OE}$ or $D_n$ input under test, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A$ = +25°C | | | 250 | μA | |
| | | | $T_A$ = +85°C | | | 250 | μA | |
| $I_{IL}$ | LOW level input current | | $T_A$ = −30°C | 0.5 | | | μA | Apply $V_{ILmin}$ to each input under test, one at a time, with $V_{IHmax}$ applied to all other inputs. |
| | | | $T_A$ = +25°C | 0.5 | | | μA | |
| | | | $T_A$ = +85°C | 0.3 | | | μA | |
| $-I_{EE}$ | $V_{EE}$ supply current | | $T_A$ = −30°C | | | 58 | mA | |
| | | | $T_A$ = +25°C | | 42 | 53 | mA | |
| | | | $T_A$ = +85°C | | | 58 | mA | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | | $T_A$ = +25°C | | 0.016 | | V/V | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | | 0.250 | | V/V | |
| $\frac{\Delta V_{BB}}{\Delta V_{EE}}$ | Reference bias voltage compensation | | | | 0.148 | | V/V | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst-case testing guidelines, refer to Section 3 Testing, DC testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 4.

## Multiplexer

## 10159


$V_{OUT}$
$V_{OHmax}$ (−810mV)
$V_{OHmin}$ (−960mV)
$V_{OHT}$ (−980mV)
GUARANTEED OPERATING AREA
$V_{OLT}$ (−1630mV)
TYP
$V_{OLmax}$ (−1650mV)
$V_{OLmin}$ (−1850mV)
$V_{IN}$
$V_{ILmin}$ (−1850mV)
$V_{IHmax}$ (−810mV)
$V_{ILT}$ (−1475mV)
$V_{IHT}$ (−1105mV)
$V_{BB}$ (−1290mV)
DF05480S

**NOTES:**

$V_{IHmax}$ – Maximum HIGH level input voltage (the most positive $V_{IH}$).

$V_{IHT}$ – HIGH level input threshold voltage.

$V_{ILT}$ – LOW level input threshold voltage.

$V_{ILmin}$ – Minimum LOW level input voltage (the most negative $V_{IL}$).

$V_{OHmax}$ – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition.

$V_{OHmin}$ – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition.

$V_{OHT}$ – HIGH level output threshold voltage with the inputs set to their respective threshold levels.

$V_{OLT}$ – LOW level output threshold voltage with the inputs set to their respective threshold levels.

$V_{OLmax}$ – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions.

$V_{OLmin}$ – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions.

$V_{BB}$ – Reference bias voltage. The internally generated reference voltage which is used to set the input and output threshold level.

**Figure 4. Transfer Characteristics**

## AC ELECTRICAL CHARACTERISTICS $V_{CC}$= +2.0V ±0.010V, $V_{EE}$ = −3.2V ±0.010V

| PARAMETER | | $T_A$ = −30°C | | $T_A$ = +25°C | | | $T_A$ = +85°C | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Typ | Max | Min | Max | | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$D_n$ to $\overline{Q}_n$ | 1.1<br>1.1 | 3.8<br>3.8 | 1.2<br>1.2 | 2.5<br>2.5 | 3.3<br>3.3 | 1.1<br>1.1 | 3.8<br>3.8 | ns<br>ns | Figs. 5, 6, 7 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>S to $\overline{Q}_n$ | 1.5<br>1.5 | 5.3<br>5.3 | 1.5<br>1.5 | 3.2<br>3.2 | 5.0<br>5.0 | 1.5<br>1.5 | 5.3<br>5.3 | ns<br>ns | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$\overline{OE}$ to $\overline{Q}_n$ | 1.4<br>1.4 | 5.3<br>5.3 | 1.5<br>1.5 | 2.5<br>2.5 | 5.0<br>5.0 | 1.4<br>1.4 | 5.3<br>5.3 | ns<br>ns | |
| $t_{TLH}$<br>$t_{THL}$ | Transition time<br>20% to 80%, 80% to 20% | 1.0<br>1.0 | 3.7<br>3.7 | 1.1<br>1.1 | 2.5<br>2.5 | 3.5<br>3.5 | 1.0<br>1.0 | 3.7<br>3.7 | ns<br>ns | Figs. 5, 6, 7 |

## AC WAVEFORMS

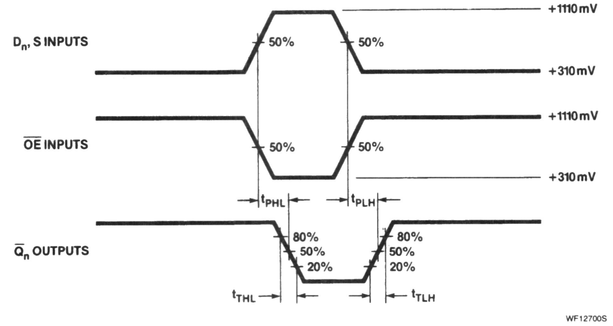
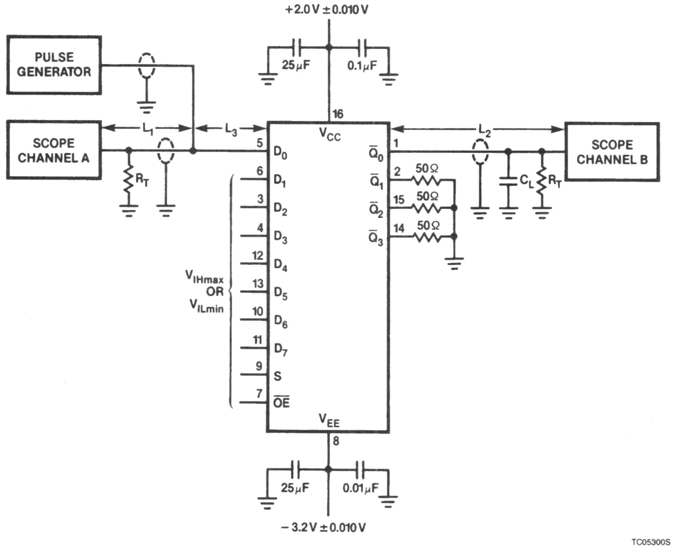

$D_n$, S INPUTS
+1110mV
50%
50%
+310mV
$\overline{OE}$ INPUTS
+1110mV
50%
50%
+310mV
$t_{PHL}$
$t_{PLH}$
$\overline{Q}_n$ OUTPUTS
80%
50%
20%
80%
50%
20%
$t_{THL}$
$t_{TLH}$
WF12700S

**Figure 5. Propagation Delay and Transition Times**

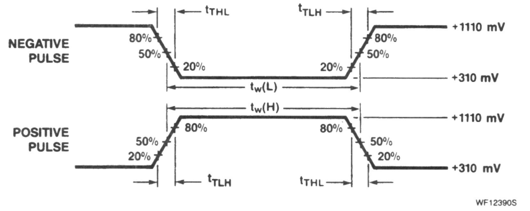
## TEST CIRCUITS AND WAVEFORMS


+2.0V ±0.010V
25μF
0.1μF
16
PULSE GENERATOR
SCOPE CHANNEL A
L1
L3
L2
RT
5 D0
6 D1
3 D2
4 D3
12 D4
13 D5
10 D6
11 D7
9 S
7 OE
VCC
VEE
Q0 1
Q1 2
Q2 15
Q3 14
50Ω
50Ω
50Ω
CL
RT
SCOPE CHANNEL B
VIHmax OR VILmin
8
25μF
0.01μF
−3.2V ±0.010V
TC05300S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1μF and 25μF from GND to $V_{CC}$, 0.01μF and 25μF from GND to $V_{EE}$ (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than ¼ inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed ¼ inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than ¼ inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance ≤ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed ¼ inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1%.

**Figure 6. AC Test Circuit**


NEGATIVE PULSE
POSITIVE PULSE
tTHL
tTLH
80%
50%
20%
tw(L)
tw(H)
+1110 mV
+310 mV
+1110 mV
+310 mV
WF12390S

| INPUT PULSE REQUIREMENTS<br>$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$, $V_T$ = GND (0V) | | | | | |
|---|---|---|---|---|---|
| Family | Amplitude | Rep Rate | Pulse Width | $t_{TLH}$ | $t_{THL}$ |
| 10K ECL | 800mVp-p | 1MHz | 500ns | 2.0 ± 0.2ns | 2.0 ± 0.2ns |

**Figure 7. Input Pulse Definition**

**Signetics**

# 10160

# Parity Checker/Generator

**12-Bit Parity Checker/Generator**
***Product Specification***

**ECL Products**

## DESCRIPTION

The 10160 is a 12-bit Parity Checker or Generator. The output goes HIGH when an odd number on inputs are HIGH. If parity detection or generation is required for less than 12 bits, all unused inputs can be left open due to integrated pull-down resistors which avoid the need for a supply voltage.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 10160 | 5.0ns | 62mA |

## ORDERING CODE

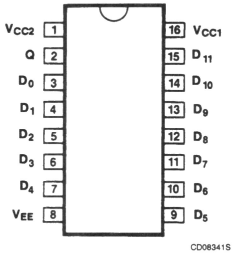
| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} = GND$; $V_{EE} = -5.2V$<br>$T_A = -30°C$ to $+85°C$ |
|---|---|
| Plastic DIP | 10160N |
| Ceramic DIP | 10160F |

## PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_0 - D_{11}$ | Data Inputs |
| Q | Data Output |

6

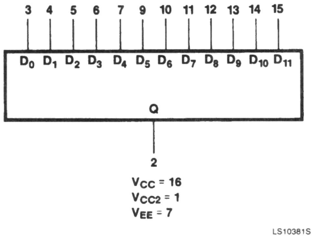
## PIN CONFIGURATION



V_CC2 1
Q 2
D0 3
D1 4
D2 5
D3 6
D4 7
V_EE 8
16 V_CC1
15 D11
14 D10
13 D9
12 D8
11 D7
10 D6
9 D5
CD08341S

**Figure 1**

## LOGIC SYMBOL



3 4 5 6 7 9 10 11 12 13 14 15
D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11
Q
2
V_CC = 16
V_CC2 = 1
V_EE = 7
LS10381S

**Figure 2**

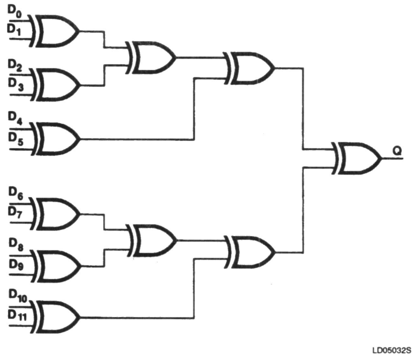

$D_0$
$D_1$
$D_2$
$D_3$
$D_4$
$D_5$
$D_6$
$D_7$
$D_8$
$D_9$
$D_{10}$
$D_{11}$
Q
LD05032S

Figure 3. Logic Diagram

## FUNCTION TABLE

| SUM OF INPUTS AT HIGH STATE | Q |
|---|---|
| Odd | H |
| Even | L |

Positive Logic:
H = HIGH state (the more positive voltage) = 1
L = LOW state (the less positive voltage) = 0

## Parity Checker/Generator 10160

**ABSOLUTE MAXIMUM RATINGS** (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | | 10K ECL | UNIT |
|---|---|---|---|---|
| $V_{EE}$ | Supply voltage | | −8.0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | | 0 to $V_{EE}$ | V |
| $I_O$ | Output source current | | −50 | mA |
| $T_S$ | Storage temperature | | −55 to +150 | °C |
| $T_J$ | Maximum junction temperature | Ceramic package | +165 | °C |
| | | Plastic package | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | 10K ECL | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | −5.2 | | V |
| $V_{IH}$ | HIGH level input voltage | $T_A$ = −30°C | | | −890 | mV |
| | | $T_A$ = +25°C | | | −810 | mV |
| | | $T_A$ = +85°C | | | −700 | mV |
| $V_{IHT}$ | HIGH level input threshold voltage | $T_A$ = −30°C | −1205 | | | mV |
| | | $T_A$ = +25°C | −1105 | | | mV |
| | | $T_A$ = +85°C | −1035 | | | mV |
| $V_{ILT}$ | LOW level input threshold voltage | $T_A$ = −30°C | | | −1500 | mV |
| | | $T_A$ = +25°C | | | −1475 | mV |
| | | $T_A$ = +85°C | | | −1440 | mV |
| $V_{IL}$ | LOW level input voltage | $T_A$ = −30°C | −1890 | | | mV |
| | | $T_A$ = +25°C | −1850 | | | mV |
| | | $T_A$ = +85°C | −1825 | | | mV |
| $T_A$ | Operating ambient temperature | | −30 | +25 | +85 | °C |

**NOTE:**
When operating at $V_{EE}$ other than specified voltage (−5.2V), the DC and AC Characteristics will vary slightly from specified values.
(See table of DC Characteristics)

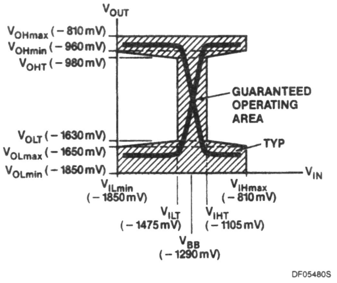
**DC ELECTRICAL CHARACTERISTICS** $V_{CC1} = V_{CC2}$ = GND, $V_{EE}$ = −5.2V ±0.010V, $T_A$ = −30°C to +85°C, output loading with 50Ω to −2.0V ±0.010V unless otherwise specified[1,3]

| PARAMETER | | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | | $T_A$ = −30°C | −1060 | | −890 | mV | Apply $V_{IHmax}$ to each input, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A$ = +25°C | −960 | | −810 | mV | |
| | | | $T_A$ = +85°C | −890 | | −700 | mV | |
| $V_{OHT}$ | HIGH level output threshold voltage | | $T_A$ = −30°C | −1080 | | | mV | Apply $V_{IHT}$ to each input, one at a time with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A$ = −25°C | −980 | | | mV | |
| | | | $T_A$ = −85°C | −910 | | | mV | |
| $V_{OLT}$ | LOW level output threshold voltage | | $T_A$ = −30°C | | | −1655 | mV | Apply $V_{ILT}$ to each input, one at a time with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A$ = −25°C | | | −1630 | mV | |
| | | | $T_A$ = −85°C | | | −1595 | mV | |
| $V_{OL}$ | LOW level output voltage | | $T_A$ = −30°C | −1890 | | −1675 | mV | Apply $V_{IHmax}$ to all inputs or apply $V_{ILmin}$ to all inputs. |
| | | | $T_A$ = +25°C | −1850 | | −1650 | mV | |
| | | | $T_A$ = +85°C | −1825 | | −1615 | mV | |
| $I_{IH}$ | HIGH level input current | Input pins 3, 6, 7, 11, 12, 15 | $T_A$ = −30°C | | | 425 | μA | Apply $V_{IHmax}$ to each input under test, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A$ = +25°C | | | 265 | μA | |
| | | | $T_A$ = +85°C | | | 265 | μA | |
| | | Other inputs | $T_A$ = +30°C | | | 360 | μA | |
| | | | $T_A$ = +25°C | | | 220 | μA | |
| | | | $T_A$ = +85°C | | | 220 | μA | |
| $I_{IL}$ | LOW level input current | | $T_A$ = −30°C | 0.5 | | | μA | Apply $V_{ILmin}$ to each input under test, one at a time, with $V_{IHmax}$ applied to all other inputs. |
| | | | $T_A$ = +25°C | 0.5 | | | μA | |
| | | | $T_A$ = +85°C | 0.3 | | | μA | |
| $-I_{EE}$ | $V_{EE}$ supply current | | $T_A$ = −30°C | | | 86 | mA | Apply $V_{IHmax}$ to input pins 4, 5, 9, 10, 13, 14 and $V_{ILmin}$ to all other pins. |
| | | | $T_A$ = +25°C | | 62 | 78 | mA | |
| | | | $T_A$ = +85°C | | | 86 | mA | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | | $T_A$ = +25°C | | 0.016 | | V/V | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | | 0.250 | | V/V | |
| $\frac{\Delta V_{BB}}{\Delta V_{EE}}$ | Reference bias voltage compensation | | | | 0.148 | | V/V | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst-case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 4.

## Parity Checker/Generator 10160



**NOTES:**

$V_{IHmax}$ – Maximum HIGH level input voltage (the most positive $V_{IH}$).

$V_{IHT}$ – HIGH level input threshold voltage.

$V_{ILT}$ – LOW level input threshold voltage.

$V_{ILmin}$ – Minimum LOW level input voltage (the most negative $V_{IL}$).

$V_{OHmax}$ – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition.

$V_{OHmin}$ – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition.

$V_{OHT}$ – HIGH level output threshold voltage with the inputs set to their respective threshold levels.

$V_{OLT}$ – LOW level output threshold voltage with the inputs set to their respective threshold levels.

$V_{OLmax}$ – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions.

$V_{OLmin}$ – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions.

$V_{BB}$ – Reference bias voltage. The internally generated reference voltage which is used to set the input and output threshold level.

Figure 4. Transfer Characteristics

## AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$

| PARAMETER | $T_A = -30°C$ | | $T_A = +25°C$ | | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Typ | Max | Min | Max | | |
| $t_{PLH}$ Propagation delay | 1.8 | 8.1 | 2.0 | 5.0 | 7.5 | 2.0 | 8.0 | ns | Figs. 5, 6, 7 |
| $t_{PHL}$ $A_0 - A_{11}$ to $Q_n$ | 1.8 | 8.1 | 2.0 | 5.0 | 7.5 | 2.0 | 8.0 | ns | |
| $t_{TLH}$ Transition time | 1.1 | 3.5 | 1.1 | 2.0 | 3.3 | 1.0 | 3.5 | ns | Figs. 5, 6, 7 |
| $t_{THL}$ 20% to 80%, 80% to 20% | 1.1 | 3.5 | 1.1 | 2.0 | 3.3 | 1.0 | 3.5 | ns | |

## AC WAVEFORMS

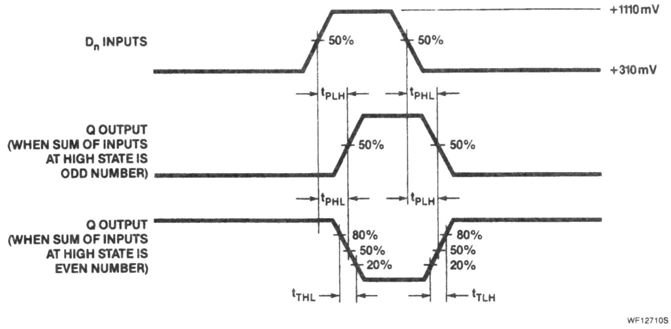
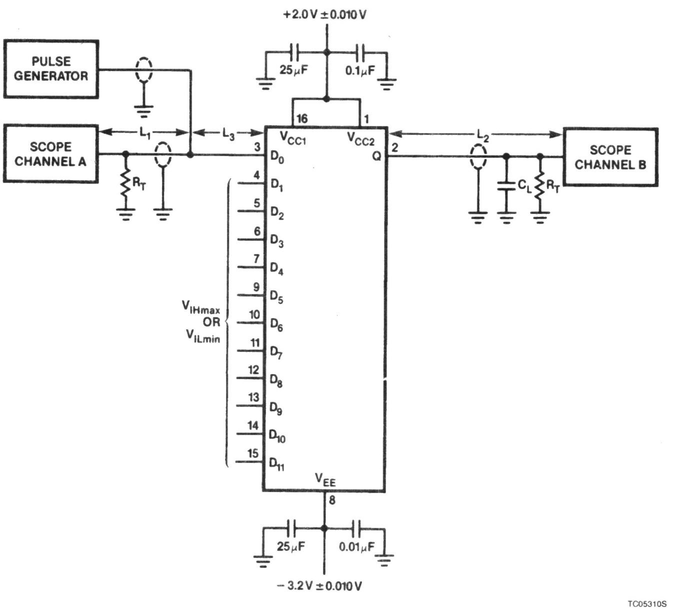

$D_n$ INPUTS
+1110mV
+310mV
50%
50%
$t_{PLH}$
$t_{PHL}$
Q OUTPUT (WHEN SUM OF INPUTS AT HIGH STATE IS ODD NUMBER)
50%
50%
$t_{PHL}$
$t_{PLH}$
Q OUTPUT (WHEN SUM OF INPUTS AT HIGH STATE IS EVEN NUMBER)
80%
50%
20%
80%
50%
20%
$t_{THL}$
$t_{TLH}$
WF12710S

Figure 5. Propagation Delay and Transition Times

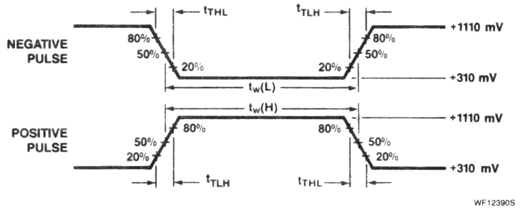
## TEST CIRCUITS AND WAVEFORMS


+2.0V ±0.010V
25µF
0.1µF
PULSE GENERATOR
SCOPE CHANNEL A
L1
L3
L2
RT
16
1
VCC1
VCC2
3
D0
2
Q
SCOPE CHANNEL B
CL
RT
4 D1
5 D2
6 D3
7 D4
9 D5
10 D6
11 D7
12 D8
13 D9
14 D10
15 D11
VIHmax OR VILmin
VEE
8
25µF
0.01µF
−3.2V ±0.010V
TC05310S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1µF and 25µF from GND to $V_{CC}$, 0.01µF and 25µF from GND to $V_{EE}$ (0.01 and 0.1µF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than ¼ inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed ¼ inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than ¼ inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance ≤ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed ¼ inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.

Figure 6. AC Test Circuit


NEGATIVE PULSE
POSITIVE PULSE
tTHL
tTLH
80%
50%
20%
tw(L)
tw(H)
+1110 mV
+310 mV
+1110 mV
+310 mV
WF12390S

| INPUT PULSE REQUIREMENTS<br>$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$, $V_T$ = GND (0V) | | | | | |
|---|---|---|---|---|---|
| **Family** | **Amplitude** | **Rep Rate** | **Pulse Width** | **$t_{TLH}$** | **$t_{THL}$** |
| 10K ECL | 800mVp-p | 1MHz | 500ns | 2.0 ±0.2ns | 2.0 ±0.2ns |

Figure 7. Input Pulse Definition

**Signetics**

# 10161

## Decoder

**1-of-8 Decoder With 2 Enable Inputs (Active LOW Outputs)**
***Product Specification***

**ECL Products**

### DESCRIPTION

The 10161 accepts three binary weighted inputs ($A_0$, $A_1$, $A_2$) and, when enabled, provides eight mutually-exclusive active LOW outputs ($Q_0 - Q_7$). The device features two active LOW enable inputs. All unused inputs can be left open due to integrated pull-down resistors which avoid the need for a supply voltage.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 10161 | 4.0ns | 61mA |

### ORDERING CODE

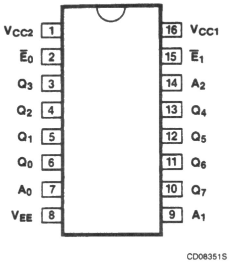
| PACKAGES | COMMERCIAL RANGE $V_{CC1} = V_{CC2} = GND$; $V_{EE} = -5.2V$ $T_A = -30°C$ to $+85°C$ |
|---|---|
| Plastic DIP | 10161N |
| Ceramic DIP | 10161F |

### PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $A_0 - A_2$ | Address Inputs |
| $\overline{E}_0$, $\overline{E}_1$ | Enable Inputs (Active LOW) |
| $Q_0 - Q_7$ | Data Outputs |

6

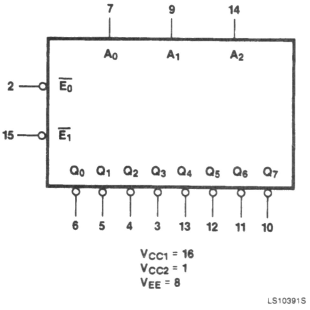
### PIN CONFIGURATION



$V_{CC2}$ 1
$\overline{E}_0$ 2
$Q_3$ 3
$Q_2$ 4
$Q_1$ 5
$Q_0$ 6
$A_0$ 7
$V_{EE}$ 8
16 $V_{CC1}$
15 $\overline{E}_1$
14 $A_2$
13 $Q_4$
12 $Q_5$
11 $Q_6$
10 $Q_7$
9 $A_1$
CD08351S

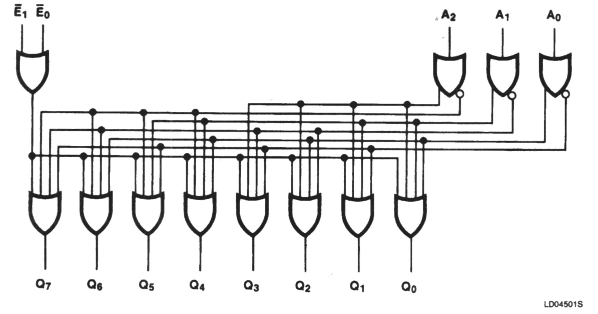
**Figure 1**

### LOGIC SYMBOL



7
9
14
$A_0$
$A_1$
$A_2$
2
$\overline{E}_0$
15
$\overline{E}_1$
$Q_0$ $Q_1$ $Q_2$ $Q_3$ $Q_4$ $Q_5$ $Q_6$ $Q_7$
6 5 4 3 13 12 11 10
$V_{CC1}$ = 16
$V_{CC2}$ = 1
$V_{EE}$ = 8
LS10391S

**Figure 2**



**$A_0$ to $A_2$: Binary Inputs; $\overline{E}_0$ , $\overline{E}_1$: Enable Inputs; $Q_0$ to $Q_7$: Coded Outputs**
**Figure 3. Logic Function**

## FUNCTION TABLE

| ENABLE INPUTS | | BINARY INPUTS | | | DECIMAL OUTPUTS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $\overline{E}_0$ | $\overline{E}_1$ | $A_0$ | $A_1$ | $A_2$ | $Q_0$ | $Q_1$ | $Q_2$ | $Q_3$ | $Q_4$ | $Q_5$ | $Q_6$ | $Q_7$ |
| H | H | X | X | X | H | H | H | H | H | H | H | H |
| L | H | X | X | X | H | H | H | H | H | H | H | H |
| H | L | X | X | X | H | H | H | H | H | H | H | H |
| L | L | L | L | L | L | H | H | H | H | H | H | H |
| L | L | H | L | L | H | L | H | H | H | H | H | H |
| L | L | L | H | L | H | H | L | H | H | H | H | H |
| L | L | H | H | L | H | H | H | L | H | H | H | H |
| L | L | L | L | H | H | H | H | H | L | H | H | H |
| L | L | H | L | H | H | H | H | H | H | L | H | H |
| L | L | L | H | H | H | H | H | H | H | H | L | H |
| L | L | H | H | H | H | H | H | H | H | H | H | L |

Positive Logic:
H = HIGH state (the more positive voltage) = 1
L = LOW state (the less positive voltage) = 0
X = Don't Care

## Decoder 10161

**ABSOLUTE MAXIMUM RATINGS** (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | | 10K ECL | UNIT |
|---|---|---|---|---|
| $V_{EE}$ | Supply voltage | | -8.0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | | 0 to $V_{EE}$ | V |
| $I_O$ | Output source current | | -50 | mA |
| $T_S$ | Storage temperature | | -55 to +150 | °C |
| $T_J$ | Maximum junction temperature | Ceramic package | +165 | °C |
| | | Plastic package | +150 | °C |

### DC OPERATING CONDITIONS

| PARAMETER | | | 10K ECL | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | -5.2 | | V |
| $V_{IH}$ | HIGH level input voltage | $T_A = -30°C$ | | | -890 | mV |
| | | $T_A = +25°C$ | | | -810 | mV |
| | | $T_A = +85°C$ | | | -700 | mV |
| $V_{IHT}$ | HIGH level input threshold voltage | $T_A = -30°C$ | -1205 | | | mV |
| | | $T_A = +25°C$ | -1105 | | | mV |
| | | $T_A = +85°C$ | -1035 | | | mV |
| $V_{ILT}$ | LOW level input threshold voltage | $T_A = -30°C$ | | | -1500 | mV |
| | | $T_A = +25°C$ | | | -1475 | mV |
| | | $T_A = +85°C$ | | | -1440 | mV |
| $V_{IL}$ | LOW level input voltage | $T_A = -30°C$ | -1890 | | | mV |
| | | $T_A = +25°C$ | -1850 | | | mV |
| | | $T_A = +85°C$ | -1825 | | | mV |
| $T_A$ | Operating ambient temperature | | -30 | +25 | +85 | °C |

**NOTE:**
When operating at $V_{EE}$ other than specified voltage (-5.2V), the DC and AC Characteristics will vary slightly from specified values.
(See table of DC Characteristics)

## Decoder

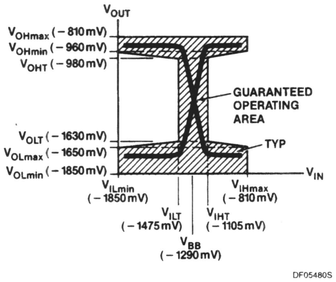
## 10161

**DC ELECTRICAL CHARACTERISTICS** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$, output loading with 50Ω to −2.0V ±0.010V unless otherwise specified[1,3]

| PARAMETER | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | $T_A = -30°C$ | −1060 | | −890 | mV | Apply $V_{IHmax}$ to $\overline{E}_0$ input with $V_{ILmin}$ applied to all other inputs. |
| | | $T_A = +25°C$ | −960 | | −810 | mV | |
| | | $T_A = +85°C$ | −890 | | −700 | mV | |
| $V_{OHT}$ | HIGH level output threshold voltage | $T_A = -30°C$ | −1080 | | | mV | Apply $V_{IHT}$ to $\overline{E}_0$ input with $V_{ILmin}$ applied to all other inputs. |
| | | $T_A = +25°C$ | −980 | | | mV | |
| | | $T_A = +85°C$ | −910 | | | mV | |
| $V_{OLT}$ | LOW level output threshold voltage | $T_A = -30°C$ | | | −1655 | mV | Using $V_{IHmax}$ and $V_{ILmin}$, apply a functional pattern as indicated in the Function Table, Substituting $V_{IHT}$ for $V_{IHmax}$ and $V_{ILT}$ for $V_{ILmin}$ on one input at a time and measure $V_{OLT}$ on the respective output. |
| | | $T_A = +25°C$ | | | −1630 | mV | |
| | | $T_A = +85°C$ | | | −1595 | mV | |
| $V_{OL}$ | LOW level output voltage | $T_A = -30°C$ | −1890 | | −1675 | mV | Using $V_{IHmax}$ and $V_{ILmin}$, apply a functional pattern as indicated in the Function Table and measure $V_{OL}$ on the respective output. |
| | | $T_A = +25°C$ | −1850 | | −1650 | mV | |
| | | $T_A = +85°C$ | −1825 | | −1615 | mV | |
| $I_{IH}$ | HIGH level input current | $T_A = -30°C$ | | | 350 | μA | Apply $V_{IHmax}$ to each input under test, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | $T_A = +25°C$ | | | 220 | μA | |
| | | $T_A = +85°C$ | | | 220 | μA | |
| $I_{IL}$ | LOW level input current | $T_A = -30°C$ | 0.5 | | | μA | Apply $V_{ILmin}$ to each input under test, one at a time, with $V_{IHmax}$ applied to all other inputs. |
| | | $T_A = +25°C$ | 0.5 | | | μA | |
| | | $T_A = +85°C$ | 0.3 | | | μA | |
| $-I_{EE}$ | $V_{EE}$ supply current | $T_A = -30°C$ | | | 84 | mA | Apply $V_{IHmax}$ to pins 2, 7, 9, 14, 15 and $V_{ILmin}$ to all other inputs. |
| | | $T_A = +25°C$ | | 61 | 76 | mA | |
| | | $T_A = +85°C$ | | | 84 | mA | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | $T_A = +25°C$ | | 0.016 | | V/V | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | 0.250 | | V/V | |
| $\frac{\Delta V_{BB}}{\Delta V_{EE}}$ | Reference bias voltage compensation | | | 0.148 | | V/V | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst-case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 4.



**NOTES:**

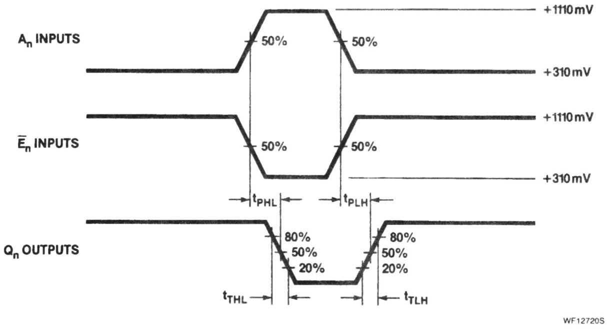
$V_{IHmax}$ – Maximum HIGH level input voltage (the most positive $V_{IH}$).
$V_{IHT}$ – HIGH level input threshold voltage.
$V_{ILT}$ – LOW level input threshold voltage.
$V_{ILmin}$ – Minimum LOW level input voltage (the most negative $V_{IL}$).
$V_{OHmax}$ – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition.
$V_{OHmin}$ – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition.
$V_{OHT}$ – HIGH level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLT}$ – LOW level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLmax}$ – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions.
$V_{OLmin}$ – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions.
$V_{BB}$ – Reference bias voltage. The internally generated reference voltage which is used to set the input and output threshold level.

Figure 4. Transfer Characteristics

## AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$

| PARAMETER | $T_A = -30°C$ | | $T_A = +25°C$ | | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Typ | Max | Min | Max | | |
| $t_{PLH}$ Propagation delay | 1.5 | 6.2 | 1.5 | 4.0 | 6.0 | 1.5 | 6.4 | ns | Figs. 5, 6, 7 |
| $t_{PHL}$ $\overline{E}_n$, $A_n$ to $Q_n$ | 1.5 | 6.2 | 1.5 | 4.0 | 6.0 | 1.5 | 6.4 | ns | |
| $t_{TLH}$ Transition time | 1.0 | 3.3 | 1.1 | 2.0 | 3.3 | 1.1 | 3.5 | ns | Figs. 5, 6, 7 |
| $t_{THL}$ 20% to 80%, 80% to 20% | 1.0 | 3.3 | 1.1 | 2.0 | 3.3 | 1.1 | 3.5 | ns | |

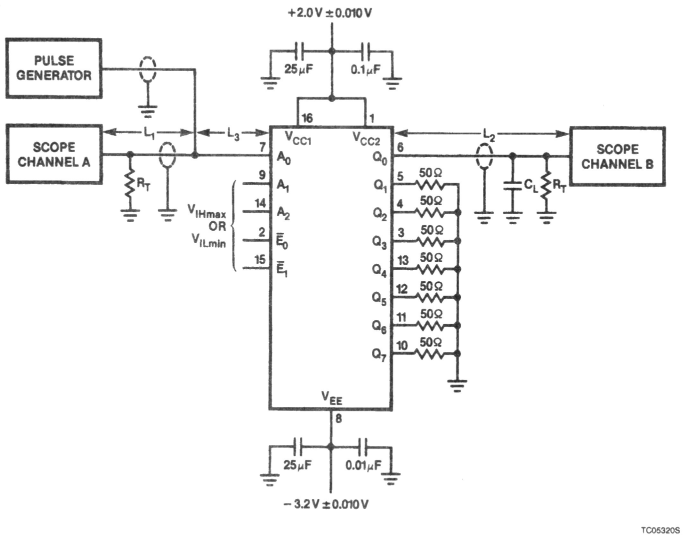
## AC WAVEFORMS



**NOTE:**
Output waveform (a) or (b) depends on particular input and output under test.

Figure 5. Propagation Delay and Transition Times

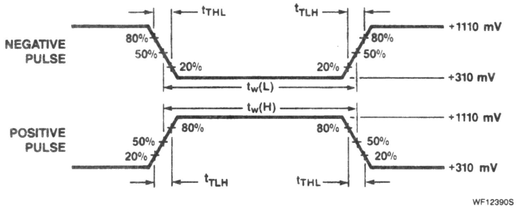
## TEST CIRCUITS AND WAVEFORMS


+2.0V ±0.010V
25μF
0.1μF
PULSE GENERATOR
SCOPE CHANNEL A
L1
L3
L2
RT
16
1
VCC1
VCC2
7
A0
6
Q0
9
A1
Q1
14
A2
Q2
2
Ē0
Q3
15
Ē1
Q4
Q5
Q6
Q7
5
4
3
13
12
11
10
50Ω
VIHmax OR VILmin
SCOPE CHANNEL B
CL
VEE
8
25μF
0.01μF
-3.2V ±0.010V
TC05320S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1μF and 25μF from GND to $V_{CC}$, 0.01μF and 25μF from GND to $V_{EE}$ (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than ¼ inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed ¼ inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than ¼ inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance ≤ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed ¼ inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.

Figure 6. AC Test Circuit


NEGATIVE PULSE
POSITIVE PULSE
tTHL
tTLH
80%
50%
20%
tw(L)
tw(H)
+1110 mV
+310 mV
WF12390S

| INPUT PULSE REQUIREMENTS<br>$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$, $V_T$ = GND (0V) | | | | | |
|---|---|---|---|---|---|
| Family | Amplitude | Rep Rate | Pulse Width | $t_{TLH}$ | $t_{THL}$ |
| 10K ECL | 800mVp-p | 1MHz | 500ns | 2.0 ±0.2ns | 2.0 ±0.2ns |

Figure 7. Input Pulse Definition

**Signetics**

# 10162

# Decoder

**1-of-8 Decoder With 2 Enable Inputs (Active HIGH Outputs)**
***Product Specification***

**ECL Products**

## DESCRIPTION

The 10162 accepts three binary weighted inputs ($A_0$, $A_1$, $A_2$) and when enabled, provides eight mutually-exclusive active HIGH outputs ($Q_0 - Q_7$). The device features two active LOW enable inputs. All unused inputs can be left open due to integrated pull-down resistors which avoid the need for a supply voltage.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 10162 | 4.0ns | 61mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} = GND$; $V_{EE} = -5.2V$<br>$T_A = -30°C$ to $+85°C$ |
|---|---|
| Plastic DIP | 10162N |
| Ceramic DIP | 10162F |

## PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $A_0 - A_2$ | Address Inputs |
| $\overline{E}_0$, $\overline{E}_1$ | Enable Inputs (Active LOW) |
| $Q_0 - Q_7$ | Data Outputs |

## PIN CONFIGURATION

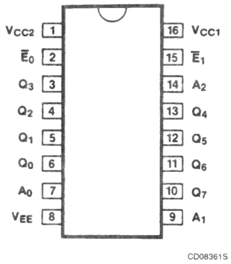

VCC2 1
Ē0 2
Q3 3
Q2 4
Q1 5
Q0 6
A0 7
VEE 8
16 VCC1
15 Ē1
14 A2
13 Q4
12 Q5
11 Q6
10 Q7
9 A1
CD08361S

Figure 1

## LOGIC SYMBOL

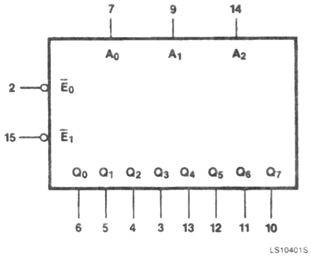
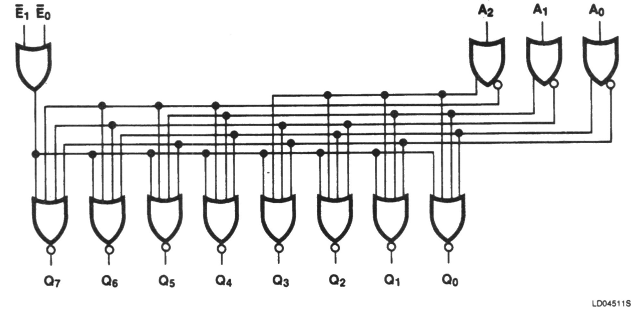

7
9
14
A0
A1
A2
2
Ē0
15
Ē1
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
6 5 4 3 13 12 11 10
LS10401S

Figure 2



**$A_0$ to $A_2$: Binary Inputs; $\overline{E}_1$, $\overline{E}_2$: Enable Inputs; $\overline{Q}_0$ to $\overline{Q}_7$: Decoded Outputs**
**Figure 3. Logic Diagram**

## FUNCTION TABLE

| ENABLE INPUTS | | BINARY INPUTS | | | DECIMAL OUTPUTS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $\overline{E}_0$ | $\overline{E}_1$ | $A_0$ | $A_1$ | $A_3$ | $Q_0$ | $Q_1$ | $Q_2$ | $Q_3$ | $Q_4$ | $Q_5$ | $Q_6$ | $Q_7$ |
| H | H | X | X | X | L | L | L | L | L | L | L | L |
| L | H | X | X | X | L | L | L | L | L | L | L | L |
| H | L | X | X | X | L | L | L | L | L | L | L | L |
| L | L | L | L | L | H | L | L | L | L | L | L | L |
| L | L | H | L | L | L | H | L | L | L | L | L | L |
| L | L | L | H | L | L | L | H | L | L | L | L | L |
| L | L | H | H | L | L | L | L | H | L | L | L | L |
| L | L | L | L | H | L | L | L | L | H | L | L | L |
| L | L | H | L | H | L | L | L | L | L | H | L | L |
| L | L | L | H | H | L | L | L | L | L | L | H | L |
| L | L | H | H | H | L | L | L | L | L | L | L | H |

Positive Logic:
H = HIGH state (the more positive voltage) = 1
L = LOW state (the less positive voltage) = 0
X = Don't Care

## ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | | 10K ECL | UNIT |
|---|---|---|---|---|
| $V_{EE}$ | Supply voltage | | −8.0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | | 0 to $V_{EE}$ | V |
| $I_O$ | Output source current | | −50 | mA |
| $T_S$ | Storage temperature | | −55 to +150 | °C |
| $T_J$ | Maximum junction temperature | Ceramic package | +165 | °C |
| | | Plastic package | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | 10K ECL | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | −5.2 | | V |
| $V_{IH}$ | HIGH level input voltage | $T_A$ = −30°C | | | −890 | mV |
| | | $T_A$ = +25°C | | | −810 | mV |
| | | $T_A$ = +85°C | | | −700 | mV |
| $V_{IHT}$ | HIGH level input threshold voltage | $T_A$ = −30°C | −1205 | | | mV |
| | | $T_A$ = +25°C | −1105 | | | mV |
| | | $T_A$ = +85°C | −1035 | | | mV |
| $V_{ILT}$ | LOW level input threshold voltage | $T_A$ = −30°C | | | −1500 | mV |
| | | $T_A$ = +25°C | | | −1475 | mV |
| | | $T_A$ = +85°C | | | −1440 | mV |
| $V_{IL}$ | LOW level input voltage | $T_A$ = −30°C | −1890 | | | mV |
| | | $T_A$ = +25°C | −1850 | | | mV |
| | | $T_A$ = +85°C | −1825 | | | mV |
| $T_A$ | Operating ambient temperature | | −30 | +25 | +85 | °C |

**NOTE:**

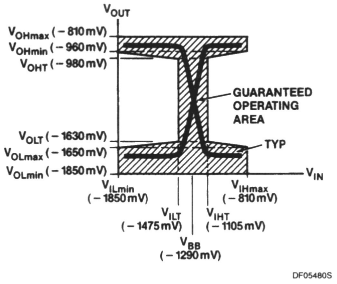
When operating at $V_{EE}$ other than specified voltage (−5.2V), the DC and AC Characteristics will vary slightly from specified values. (See table of DC Characteristics)

**DC ELECTRICAL CHARACTERISTICS** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30^\circ C$ to $+85^\circ C$, output loading with 50Ω to −2.0V ±0.010V unless otherwise specified[1,3]

| PARAMETER | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | $T_A = -30^\circ C$ | −1060 | | −890 | mV | Using $V_{IHmax}$ and $V_{ILmin}$, apply a functional pattern as indicated in the Function Table and measure $V_{OH}$ on the respective outputs. |
| | | $T_A = +25^\circ C$ | −960 | | −810 | mV | |
| | | $T_A = +85^\circ C$ | −890 | | −700 | mV | |
| $V_{OHT}$ | HIGH level output threshold voltage | $T_A = -30^\circ C$ | −1080 | | | mV | Using $V_{IHmax}$ and $V_{ILmin}$, apply a functional pattern as indicated in the Function Table, substituting $V_{IHT}$ for $V_{IHmax}$ and $V_{ILT}$ for $V_{ILmin}$ on one input at a time and measure $V_{OHT}$ on the respective output. |
| | | $T_A = +25^\circ C$ | −980 | | | mV | |
| | | $T_A = +85^\circ C$ | −910 | | | mV | |
| $V_{OLT}$ | LOW level output threshold voltage | $T_A = -30^\circ C$ | | | −1655 | mV | Apply $V_{ILmin}$ to $\overline{E}_0$ input and $V_{IHT}$ to $\overline{E}_1$ input.<br>Apply $V_{ILmin}$ to $\overline{E}_1$ input and $V_{IHT}$ to $\overline{E}_0$ input. |
| | | $T_A = +25^\circ C$ | | | −1630 | mV | |
| | | $T_A = +85^\circ C$ | | | −1595 | mV | |
| $V_{OL}$ | LOW level output voltage | $T_A = -30^\circ C$ | −1890 | | −1675 | mV | Apply $V_{IHmax}$ to $\overline{E}_0$ input and $V_{ILmin}$ to $\overline{E}_1$ input. Apply $V_{IHmax}$ to all inputs. |
| | | $T_A = +25^\circ C$ | −1850 | | −1650 | mV | |
| | | $T_A = +85^\circ C$ | −1825 | | −1615 | mV | |
| $I_{IH}$ | HIGH level input current | $T_A = -30^\circ C$ | | | 350 | μA | Apply $V_{IHmax}$ to each input under test, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | $T_A = +25^\circ C$ | | | 220 | μA | |
| | | $T_A = +85^\circ C$ | | | 220 | μA | |
| $I_{IL}$ | LOW level input current | $T_A = -30^\circ C$ | 0.5 | | | μA | Apply $V_{ILmin}$ to each input under test, one at a time, with $V_{IHmax}$ applied to all other inputs. |
| | | $T_A = +25^\circ C$ | 0.5 | | | μA | |
| | | $T_A = +85^\circ C$ | 0.3 | | | μA | |
| $-I_{EE}$ | $V_{EE}$ supply current | $T_A = -30^\circ C$ | | | 84 | mA | |
| | | $T_A = +25^\circ C$ | | 61 | 76 | mA | |
| | | $T_A = +85^\circ C$ | | | 84 | mA | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | $T_A = +25^\circ C$ | | 0.016 | | V/V | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | 0.250 | | V/V | |
| $\frac{\Delta V_{BB}}{\Delta V_{EE}}$ | Reference bias voltage compensation | | | 0.148 | | V/V | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst-case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 4.



**NOTES:**

$V_{IHmax}$ – Maximum HIGH level input voltage (the most positive $V_{IH}$).

$V_{IHT}$ – HIGH level input threshold voltage.

$V_{ILT}$ – LOW level input threshold voltage.

$V_{ILmin}$ – Minimum LOW level input voltage (the most negative $V_{IL}$).

$V_{OHmax}$ – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition.

$V_{OHmin}$ – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition.

$V_{OHT}$ – HIGH level output threshold voltage with the inputs set to their respective threshold levels.

$V_{OLT}$ – LOW level output threshold voltage with the inputs set to their respective threshold levels.

$V_{OLmax}$ – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions.

$V_{OLmin}$ – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions.

$V_{BB}$ – Reference bias voltage. The internally generated reference voltage which is used to set the input and output threshold level.

**Figure 4. Transfer Characteristics**

## AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$

| PARAMETER | | $T_A = -30°C$ | | $T_A = +25°C$ | | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Typ | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 1.5 | 6.2 | 1.5 | 4.0 | 6.0 | 1.5 | 6.4 | ns | Figs. 5, 6, 7 |
| $t_{PHL}$ | $\overline{E}_n$, $A_n$ to $Q_n$ | 1.5 | 6.2 | 1.5 | 4.0 | 6.0 | 1.5 | 6.4 | ns | |
| $t_{TLH}$ | Transition time | 1.0 | 3.3 | 1.1 | 2.0 | 3.3 | 1.1 | 3.5 | ns | Figs. 5, 6, 7 |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 1.0 | 3.3 | 1.1 | 2.0 | 3.3 | 1.1 | 3.5 | ns | |

## AC WAVEFORMS

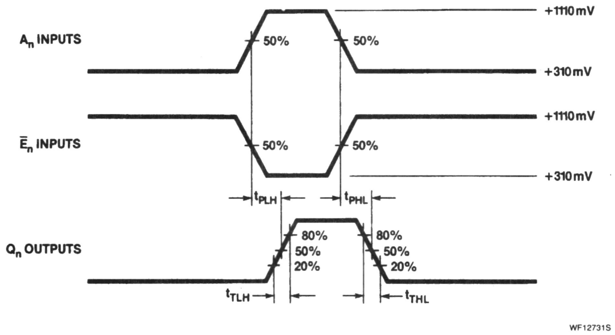
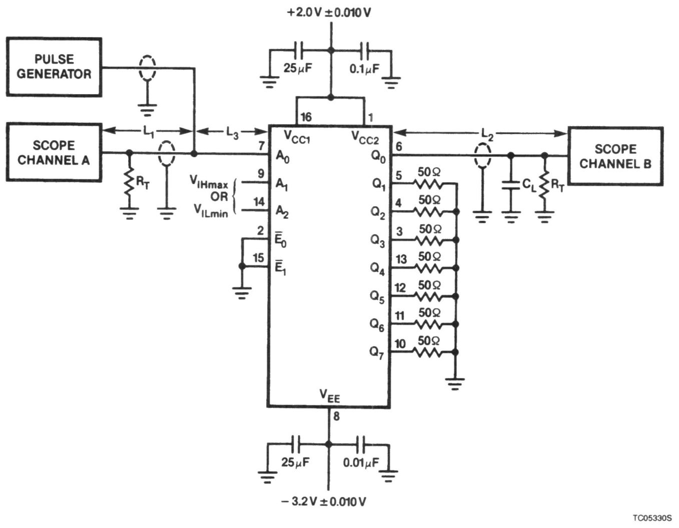


**Figure 5. Propagation Delay and Transition Times for Address to Output**

# Decoder

# 10162

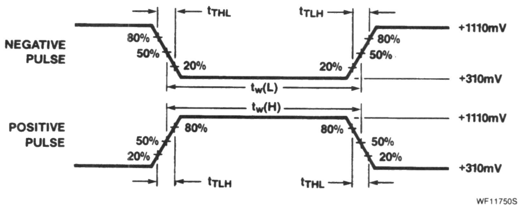
## TEST CIRCUITS AND WAVEFORMS


+2.0V ±0.010V
25μF
0.1μF
PULSE GENERATOR
SCOPE CHANNEL A
L1
L3
L2
16
1
7
6
VCC1
VCC2
A0
Q0
9
A1
14
A2
2
E0
15
E1
Q1
Q2
Q3
Q4
Q5
Q6
Q7
5
4
3
13
12
11
10
50Ω
RT
VIHmax OR VILmin
SCOPE CHANNEL B
CL
RT
VEE
8
25μF
0.01μF
−3.2V ±0.010V
TC05330S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1μF and 25μF from GND to $V_{CC}$, 0.01μF and 25μF from GND to $V_{EE}$ (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than ¼ inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed ¼ inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than ¼ inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance ≤ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed ¼ inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.

Figure 6. AC Test Circuit


NEGATIVE PULSE
POSITIVE PULSE
tTHL
tTLH
80%
50%
20%
tw(L)
tw(H)
+1110mV
+310mV
WF11750S

**INPUT PULSE REQUIREMENTS**

**$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$, $V_T$ = GND (0V)**

| Family | Amplitude | Rep Rate | Pulse Width | $t_{TLH}$ | $t_{THL}$ |
|---|---|---|---|---|---|
| 10K ECL | 800mVp-p | 1MHz | 500ns | 2.0 ±0.2ns | 2.0 ±0.2ns |

Figure 7. Input Pulse Definition

Signetics

# 10164
## Multiplexer

**8-Input Multiplexer With Enable Input**
***Product Specification***

**ECL Products**

### DESCRIPTION

The 10164 performs 8-input multiplexing with enable input. The output goes LOW when not enabled, thus permitting expansion of multiplexers by wire-ORing. All unused inputs can be left open due to integrated pull-down resistors which avoid the need for a supply voltage.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 10164 | 3.0ns | 60mA |

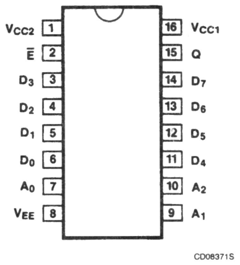
### ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} = \text{GND}$; $V_{EE} = -5.2\text{V}$<br>$T_A = -30°\text{C}$ to $+85°\text{C}$ |
|---|---|
| Plastic DIP | 10164N |
| Ceramic DIP | 10164F |

### PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_0 - D_7$ | Data Inputs |
| $A_0 - A_2$ | Address Inputs |
| $\overline{E}$ | Enable Input |
| Q | Data Output |

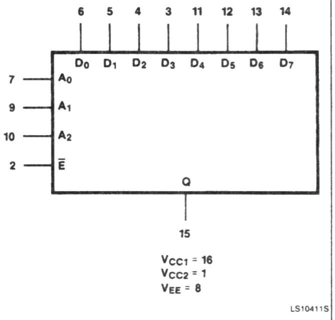
### PIN CONFIGURATION



VCC2 1
Ē 2
D3 3
D2 4
D1 5
D0 6
A0 7
VEE 8
16 VCC1
15 Q
14 D7
13 D6
12 D5
11 D4
10 A2
9 A1
CD08371S

Figure 1

### LOGIC SYMBOL

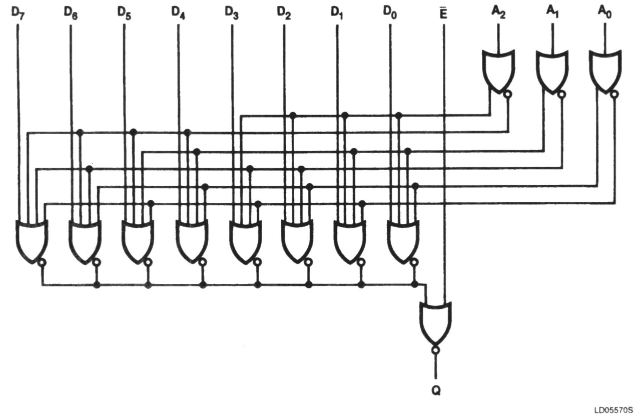


6
5
4
3
11
12
13
14
D0
D1
D2
D3
D4
D5
D6
D7
7
A0
9
A1
10
A2
2
Ē
Q
15
VCC1 = 16
VCC2 = 1
VEE = 8
LS10411S

Figure 2

# Multiplexer

# 10164



$A_0$ to $A_2$ = Address Inputs; $D_0$ to $D_7$ = Data Inputs; Ē = Enable Input

**Figure 3. Logic Diagram**

## FUNCTION TABLE

| INPUTS | | | | | | | | | | | | OUTPUT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $A_0$ | $A_1$ | $A_2$ | Ē | $D_0$ | $D_1$ | $D_2$ | $D_3$ | $D_4$ | $D_5$ | $D_6$ | $D_7$ | Q |
| L | L | L | L | L | X | X | X | X | X | X | X | L |
| L | L | L | L | H | X | X | X | X | X | X | X | H |
| H | L | L | L | X | L | X | X | X | X | X | X | L |
| H | L | L | L | X | H | X | X | X | X | X | X | H |
| L | H | L | L | X | X | L | X | X | X | X | X | L |
| L | H | L | L | X | X | H | X | X | X | X | X | H |
| H | H | L | L | X | X | X | L | X | X | X | X | L |
| H | H | L | L | X | X | X | H | X | X | X | X | H |
| L | L | H | L | X | X | X | X | L | X | X | X | L |
| L | L | H | L | X | X | X | X | H | X | X | X | H |
| H | L | H | L | X | X | X | X | X | L | X | X | L |
| H | L | H | L | X | X | X | X | X | H | X | X | H |
| L | H | H | L | X | X | X | X | X | X | L | X | L |
| L | H | H | L | X | X | X | X | X | X | H | X | H |
| H | H | H | L | X | X | X | X | X | X | X | L | L |
| H | H | H | L | X | X | X | X | X | X | X | H | H |
| X | X | X | H | X | X | X | X | X | X | X | X | L |

Positive Logic:
H = HIGH state (the more positive voltage) = 1
L = LOW state (the less positive voltage) = 0
X = Don't Care

# Multiplexer | 10164

## ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | | 10K ECL | UNIT |
|---|---|---|---|---|
| $V_{EE}$ | Supply voltage | | −8.0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | | 0 to $V_{EE}$ | V |
| $I_O$ | Output source current | | −50 | mA |
| $T_S$ | Storage temperature | | −55 to +150 | °C |
| $T_J$ | Maximum junction temperature | Ceramic package | +165 | °C |
| | | Plastic package | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | 10K ECL | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | −5.2 | | V |
| $V_{IH}$ | HIGH level input voltage | $T_A$ = −30°C | | | −890 | mV |
| | | $T_A$ = +25°C | | | −810 | mV |
| | | $T_A$ = +85°C | | | −700 | mV |
| $V_{IHT}$ | HIGH level input threshold voltage | $T_A$ = −30°C | −1205 | | | mV |
| | | $T_A$ = +25°C | −1105 | | | mV |
| | | $T_A$ = +85°C | −1035 | | | mV |
| $V_{ILT}$ | LOW level input threshold voltage | $T_A$ = −30°C | | | −1500 | mV |
| | | $T_A$ = +25°C | | | −1475 | mV |
| | | $T_A$ = +85°C | | | −1440 | mV |
| $V_{IL}$ | LOW level input voltage | $T_A$ = −30°C | −1890 | | | mV |
| | | $T_A$ = +25°C | −1850 | | | mV |
| | | $T_A$ = +85°C | −1825 | | | mV |
| $T_A$ | Operating ambient temperature | | −30 | +25 | +85 | °C |

**NOTE:**
When operating at $V_{EE}$ other than specified voltage (−5.2V), the DC and AC Characteristics will vary slightly from specified values. (See table of DC Characteristics)

6

**DC ELECTRICAL CHARACTERISTICS** $V_{CC1} = V_{CC2} =$ GND, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$, output loading with 50Ω to −2.0V ±0.010V unless otherwise specified[1,3]

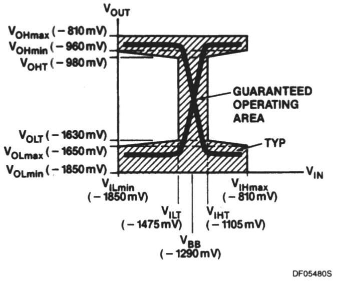
| PARAMETER | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | $T_A = -30°C$ | −1060 | | −890 | mV | Using $V_{IHmax}$ and $V_{ILmin}$, apply a functional pattern as indicated in the Function Table and measure $V_{OH}$ on the output. |
| | | $T_A = +25°C$ | −960 | | −810 | mV | |
| | | $T_A = +85°C$ | −890 | | −700 | mV | |
| $V_{OHT}$ | HIGH level output threshold voltage | $T_A = -30°C$ | −1080 | | | mV | Apply $V_{ILT}$ to $\overline{E}$ input and apply a functional pattern using $V_{IHmax}$ and $V_{ILmin}$ as indicated in the Function Table and measure $V_{OHT}$ on the output. |
| | | $T_A = +25°C$ | −980 | | | mV | |
| | | $T_A = +85°C$ | −910 | | | mV | |
| $V_{OLT}$ | LOW level output threshold voltage | $T_A = -30°C$ | | | −1655 | mV | Apply $V_{IHT}$ to $\overline{E}$ input with $V_{IHmax}$ applied to all other inputs. |
| | | $T_A = +25°C$ | | | −1630 | mV | |
| | | $T_A = +85°C$ | | | −1595 | mV | |
| $V_{OL}$ | LOW level output voltage | $T_A = -30°C$ | −1890 | | −1675 | mV | Apply $V_{IHmax}$ to all inputs.<br>Apply $V_{IHmax}$ to $\overline{E}$ input with $V_{ILmin}$ applied to all other inputs. |
| | | $T_A = +25°C$ | −1850 | | −1650 | mV | |
| | | $T_A = +85°C$ | −1825 | | −1615 | mV | |
| $I_{IH}$ | HIGH level input current | $T_A = -30°C$ | | | 425 | μA | Apply $V_{IHmax}$ to each input under test, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | $T_A = +25°C$ | | | 265 | μA | |
| | | $T_A = +85°C$ | | | 265 | μA | |
| $I_{IL}$ | LOW level input current | $T_A = -30°C$ | 0.5 | | | μA | Apply $V_{ILmin}$ to each input under test, one at a time, with $V_{IHmax}$ applied to all other inputs. |
| | | $T_A = +25°C$ | 0.5 | | | μA | |
| | | $T_A = +85°C$ | 0.3 | | | μA | |
| $-I_{EE}$ | $V_{EE}$ supply current | $T_A = -30°C$ | | | 83 | mA | |
| | | $T_A = +25°C$ | | 60 | 75 | mA | |
| | | $T_A = +85°C$ | | | 83 | mA | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | $T_A = +25°C$ | | 0.016 | | V/V | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | 0.250 | | V/V | |
| $\frac{\Delta V_{BB}}{\Delta V_{EE}}$ | Reference bias voltage compensation | | | 0.148 | | V/V | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst-case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 4.

# Multiplexer

# 10164



**NOTES:**

$V_{IHmax}$ – Maximum HIGH level input voltage (the most positive $V_{IH}$).

$V_{IHT}$ – HIGH level input threshold voltage.

$V_{ILT}$ – LOW level input threshold voltage.

$V_{ILmin}$ – Minimum LOW level input voltage (the most negative $V_{IL}$).

$V_{OHmax}$ – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition.

$V_{OHmin}$ – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition.

$V_{OHT}$ – HIGH level output threshold voltage with the inputs set to their respective threshold levels.

$V_{OLT}$ – LOW level output threshold voltage with the inputs set to their respective threshold levels.

$V_{OLmax}$ – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions.

$V_{OLmin}$ – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions.

$V_{BB}$ – Reference bias voltage. The internally generated reference voltage which is used to set the input and output threshold level.

Figure 4. Transfer Characteristics

## AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$

| PARAMETER | | $T_A = -30°C$ | | $T_A = +25°C$ | | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Typ | Max | Min | Max | | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$D_n$ to Q | 1.5<br>1.5 | 4.7<br>4.7 | 1.5<br>1.5 | 3.0<br>3.0 | 4.5<br>4.5 | 1.6<br>1.6 | 4.8<br>4.8 | ns<br>ns | Figs. 5, 6, 7 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$A_n$ to Q | 1.9<br>1.9 | 6.3<br>6.3 | 2.0<br>2.0 | 4.0<br>4.0 | 6.0<br>6.0 | 2.2<br>2.2 | 6.5<br>6.5 | ns<br>ns | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$\bar{E}$ to Q | 0.9<br>0.9 | 3.3<br>3.3 | 1.0<br>1.0 | 2.0<br>2.0 | 2.9<br>2.9 | 1.0<br>1.0 | 3.1<br>3.1 | ns<br>ns | Figs. 5, 6, 7 |
| $t_{TLH}$<br>$t_{THL}$ | Transition time<br>20% to 80%, 80% to 20% | 0.9<br>0.9 | 3.3<br>3.3 | 1.1<br>1.1 | 2.0<br>2.0 | 3.3<br>3.3 | 1.2<br>1.2 | 3.6<br>3.6 | ns<br>ns | Figs. 5, 6, 7 |

## AC WAVEFORMS

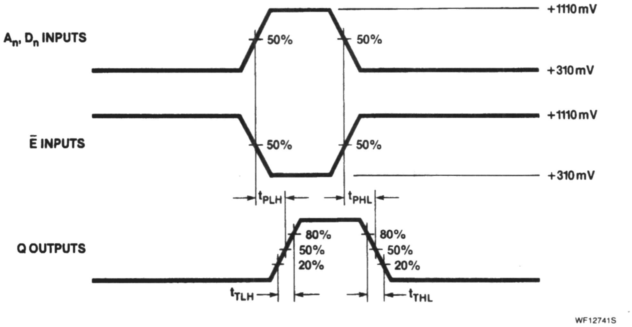
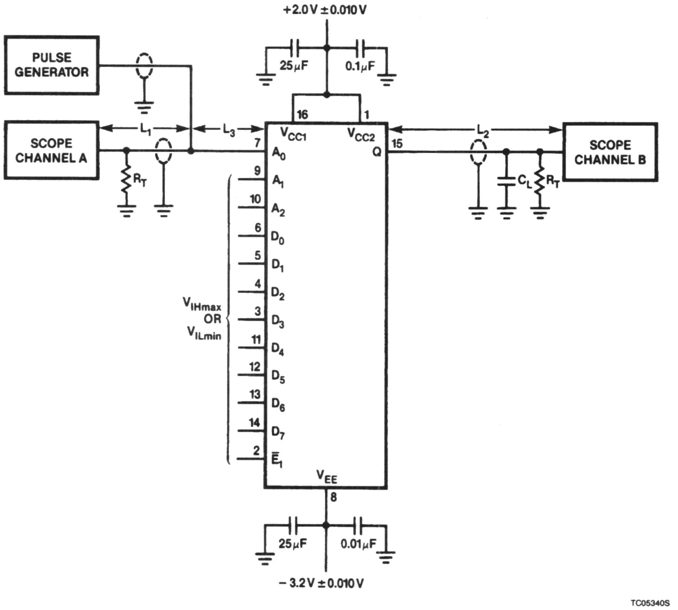


Figure 5. Propagation Delay and Transition Times for Address and Data Input to Outputs

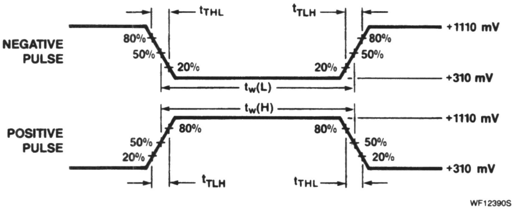
## TEST CIRCUITS AND WAVEFORMS


+2.0V ±0.010V
25μF
0.1μF
PULSE GENERATOR
SCOPE CHANNEL A
L1
L3
L2
RT
16
1
VCC1
VCC2
7
A0
15
Q
SCOPE CHANNEL B
CL
RT
9
A1
10
A2
6
D0
5
D1
4
D2
3
D3
11
D4
12
D5
13
D6
14
D7
2
Ē1
VIHmax OR VILmin
VEE
8
25μF
0.01μF
−3.2V ±0.010V
TC05340S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1μF and 25μF from GND to $V_{CC}$, 0.01μF and 25μF from GND to $V_{EE}$ (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than ¼ inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed ¼ inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than ¼ inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance ≤ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed ¼ inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ±1% or better.

Figure 6. AC Test Circuit


NEGATIVE PULSE
POSITIVE PULSE
tTHL
tTLH
80%
50%
20%
tw(L)
tw(H)
+1110 mV
+310 mV
+1110 mV
+310 mV
WF12390S

| INPUT PULSE REQUIREMENTS<br>$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$, $V_T$ = GND (0V) | | | | | |
|---|---|---|---|---|---|
| Family | Amplitude | Rep Rate | Pulse Width | $t_{TLH}$ | $t_{THL}$ |
| 10K ECL | 800mVp-p | 1MHz | 500ns | 2.0 ±0.2ns | 2.0 ±0.2ns |

Figure 7. Input Pulse Definition

**Signetics**

**ECL Products**

# 10165
# Priority Encoder/Latch

**8-Input Priority Encoder**
***Product Specification***

## DESCRIPTION

The 10165 is able to encode eight inputs to binary coded outputs. Each output is stored in a D-type latch which allows synchronous operation. When the clock input is LOW the outputs follow the inputs and latch when the clock goes HIGH. The output code is that of the highest order input so that any input of lower priority is ignored.

The input is active when HIGH (e.g. the three binary outputs are LOW when input $D_0$ is HIGH). Output $Q_3$ is HIGH when any input is HIGH, which allows direct extension into another priority encoder when more than 8 inputs are used.

The device can be used in many applications, such as testing systems and checking system status in control processors and peripheral controllers. It can also be used to generate binary codes from random logic inputs, for addressing ROMs, RAMs, or for multiplexing data.

All unused inputs must be tied LOW to $V_{IL}$ or $V_{EE}$.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 10165 | 4.5ns | 105mA |

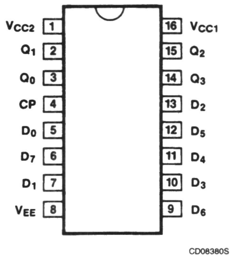
## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} = $ GND; $V_{EE} = -5.2V$<br>$T_A = -30°C$ to $+85°C$ |
|---|---|
| Plastic DIP | 10165N |
| Ceramic DIP | 10165F |

## PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_0 - D_7$ | Data Inputs |
| CP | Clock Input |
| $Q_0 - Q_3$ | Data Outputs |

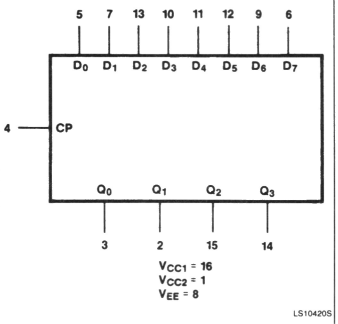
## PIN CONFIGURATION



$V_{CC2}$ 1
$Q_1$ 2
$Q_0$ 3
CP 4
$D_0$ 5
$D_7$ 6
$D_1$ 7
$V_{EE}$ 8
16 $V_{CC1}$
15 $Q_2$
14 $Q_3$
13 $D_2$
12 $D_5$
11 $D_4$
10 $D_3$
9 $D_6$
CD08380S

Figure 1

## LOGIC SYMBOL



5 7 13 10 11 12 9 6
$D_0$ $D_1$ $D_2$ $D_3$ $D_4$ $D_5$ $D_6$ $D_7$
4 CP
$Q_0$ $Q_1$ $Q_2$ $Q_3$
3 2 15 14
$V_{CC1}$ = 16
$V_{CC2}$ = 1
$V_{EE}$ = 8
LS10420S

Figure 2

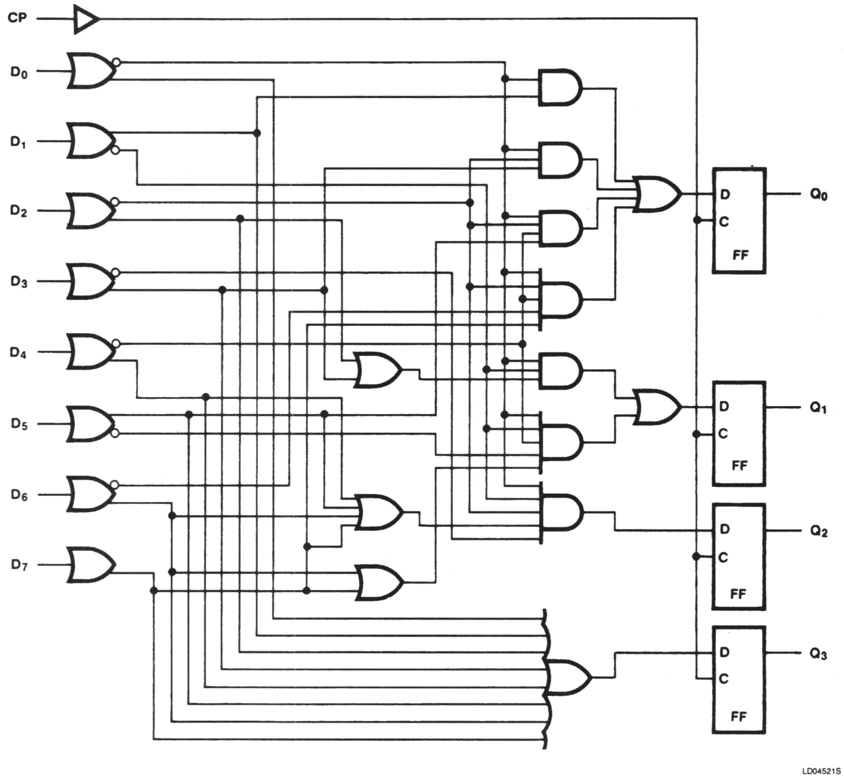


Figure 3. Logic Diagram

## FUNCTION TABLE

| INPUTS | | | | | | | | OUTPUTS | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $D_0$ | $D_1$ | $D_2$ | $D_3$ | $D_4$ | $D_5$ | $D_6$ | $D_7$ | $Q_3$ | $Q_2$ | $Q_1$ | $Q_0$ |
| H | X | X | X | X | X | X | X | H | L | L | L |
| L | H | X | X | X | X | X | X | H | L | L | H |
| L | L | H | X | X | X | X | X | H | L | H | L |
| L | L | L | H | X | X | X | X | H | L | H | H |
| L | L | L | L | H | X | X | X | H | H | L | L |
| L | L | L | L | L | H | X | X | H | H | L | H |
| L | L | L | L | L | L | H | X | H | H | H | L |
| L | L | L | L | L | L | L | H | H | H | H | H |
| L | L | L | L | L | L | L | L | L | L | L | L |

Positive Logic:
H = HIGH state (the more positive voltage) = 1
L = LOW state (the less positive voltage) = 0
X = Don't Care

## Priority Encoder/Latch 10165

**ABSOLUTE MAXIMUM RATINGS** (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | | 10K ECL | UNIT |
|---|---|---|---|---|
| $V_{EE}$ | Supply voltage | | -8.0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | | 0 to $V_{EE}$ | V |
| $I_O$ | Output current | | -50 | mA |
| $T_S$ | Storage temperature | | -55 to +150 | °C |
| $T_J$ | Maximum junction temperature | Ceramic package | +165 | °C |
| | | Plastic package | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | 10K ECL | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | -5.2 | | V |
| $V_{IH}$ | HIGH level input voltage | $T_A = -30°C$ | | | -890 | mV |
| | | $T_A = +25°C$ | | | -810 | mV |
| | | $T_A = +85°C$ | | | -700 | mV |
| $V_{IHT}$ | HIGH level input threshold voltage | $T_A = -30°C$ | -1205 | | | mV |
| | | $T_A = +25°C$ | -1105 | | | mV |
| | | $T_A = +85°C$ | -1035 | | | mV |
| $V_{ILT}$ | LOW level input threshold voltage | $T_A = -30°C$ | | | -1500 | mV |
| | | $T_A = +25°C$ | | | -1475 | mV |
| | | $T_A = +85°C$ | | | -1440 | mV |
| $V_{IL}$ | LOW level input voltage | $T_A = -30°C$ | -1890 | | | mV |
| | | $T_A = +25°C$ | -1850 | | | mV |
| | | $T_A = +85°C$ | -1825 | | | mV |
| $T_A$ | Operating ambient temperature | | -30 | +25 | +85 | °C |

**NOTE:**
When operating at $V_{EE}$ other than specified voltage (-5.2V), the DC and AC Characteristics will vary slightly from specified values. (See table of DC Characteristics)

6

## DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2} = \text{GND}$, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$, output loading with 50Ω to −2.0V ±0.010V unless otherwise specified[1,3]

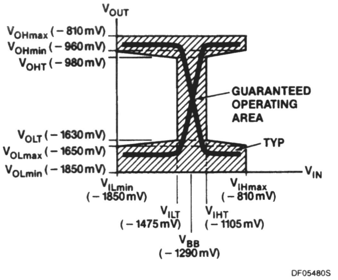
| PARAMETER | | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | | $T_A = -30°C$ | −1060 | | −890 | mV | Apply $V_{IHmax}$ to $D_7$ input with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | −960 | | −810 | mV | |
| | | | $T_A = +85°C$ | −890 | | −700 | mV | |
| $V_{OHT}$ | HIGH level output threshold voltage | | $T_A = -30°C$ | −1080 | | | mV | Apply $V_{IHT}$ to $D_7$ input with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | −980 | | | mV | |
| | | | $T_A = +85°C$ | −910 | | | mV | |
| $V_{OLT}$ | LOW level output threshold voltage | | $T_A = -30°C$ | | | −1655 | mV | Apply $V_{ILT}$ to CP input with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | | | −1630 | mV | |
| | | | $T_A = +85°C$ | | | −1595 | mV | |
| $V_{OL}$ | LOW level output voltage | | $T_A = -30°C$ | −1890 | | −1675 | mV | Apply $V_{ILmin}$ to all inputs. |
| | | | $T_A = +25°C$ | −1850 | | −1650 | mV | |
| | | | $T_A = +85°C$ | −1825 | | −1615 | mV | |
| $I_{IH}$ | HIGH level input current | CP input | $T_A = -30°C$ | | | 390 | μA | Apply $V_{IHmax}$ to CP input with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | | | 245 | μA | |
| | | | $T_A = +85°C$ | | | 245 | μA | |
| | | other inputs | $T_A = -30°C$ | | | 350 | μA | Apply $V_{IHmax}$ to each input under test, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | | | 220 | μA | |
| | | | $T_A = +85°C$ | | | 220 | μA | |
| $I_{IL}$ | LOW level input current | | $T_A = -30°C$ | 0.5 | | | μA | Apply $V_{ILmin}$ to each input under test, one at a time, with $V_{IHmax}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | 0.5 | | | μA | |
| | | | $T_A = +85°C$ | 0.3 | | | μA | |
| $-I_{EE}$ | $V_{EE}$ supply current | | $T_A = -30°C$ | | | 144 | mA | |
| | | | $T_A = +25°C$ | | 105 | 131 | mA | |
| | | | $T_A = +85°C$ | | | 144 | mA | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | | $T_A = +25°C$ | | 0.016 | | V/V | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | | 0.250 | | V/V | |
| $\frac{\Delta V_{BB}}{\Delta V_{EE}}$ | Reference bias voltage compensation | | | | 0.148 | | V/V | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst-case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 4.

## Priority Encoder/Latch

## 10165



**NOTES:**

$V_{IHmax}$ – Maximum HIGH level input voltage (the most positive $V_{IH}$).

$V_{IHT}$ – HIGH level input threshold voltage.

$V_{ILT}$ – LOW level input threshold voltage.

$V_{ILmin}$ – Minimum LOW level input voltage (the most negative $V_{IL}$).

$V_{OHmax}$ – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition.

$V_{OHmin}$ – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition.

$V_{OHT}$ – HIGH level output threshold voltage with the inputs set to their respective threshold levels.

$V_{OLT}$ – LOW level output threshold voltage with the inputs set to their respective threshold levels.

$V_{OLmax}$ – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions.

$V_{OLmin}$ – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions.

$V_{BB}$ – Reference bias voltage. The internally generated reference voltage which is used to set the input and output threshold level.

**Figure 4. Transfer Characteristics**

## AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$

| PARAMETER | $T_A = -30°C$ | | $T_A = +25°C$ | | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Typ | Max | Min | Max | | |
| $t_{PLH}$ Propagation delay | 2.0 | 7.0 | 2.0 | 4.5 | 7.0 | 2.0 | 8.0 | ns | Figs. 5, 7, 8 |
| $t_{PHL}$ $D_n$ to $Q_n$ | 2.0 | 7.0 | 2.0 | 4.5 | 7.0 | 2.0 | 8.0 | ns | |
| $t_{PLH}$ Propagation delay | 1.5 | 4.5 | 1.5 | 4.5 | 4.0 | 1.5 | 4.5 | ns | |
| $t_{PHL}$ CP to $Q_n$ | 1.5 | 4.5 | 1.5 | 4.5 | 4.0 | 1.5 | 4.5 | ns | |
| $t_s(H)$ Setup time | 6.0 | | 6.0 | 3.4 | | 6.0 | | ns | Figs. 6, 7, 8 |
| $t_s(L)$ $D_n$ to CP | 6.0 | | 6.0 | 3.0 | | 6.0 | | ns | |
| $t_h(H)$ Hold time | 1.0 | | 1.0 | −2.3 | | 1.0 | | ns | |
| $t_h(L)$ $D_n$ to CP | 1.0 | | 1.0 | −2.7 | | 1.0 | | ns | |
| $t_{TLH}$ Transition time | 1.1 | 3.5 | 1.1 | 2.0 | 3.3 | 1.1 | 3.5 | ns | Figs. 5, 7, 8 |
| $t_{THL}$ 20% to 80%, 80% to 20% | 1.1 | 3.5 | 1.1 | 2.0 | 3.3 | 1.1 | 3.5 | ns | |

## AC WAVEFORMS

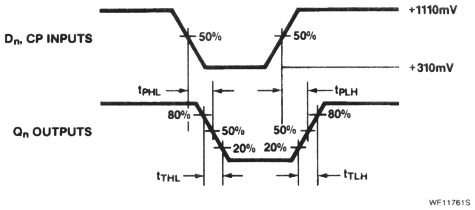


**Figure 5. Propagation Delay and Transition Times for Data to Output**

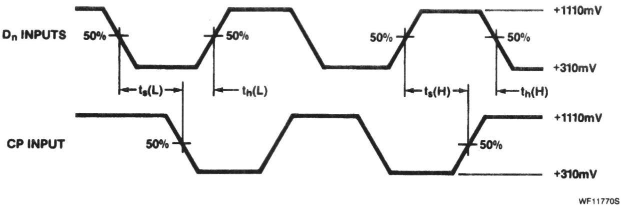
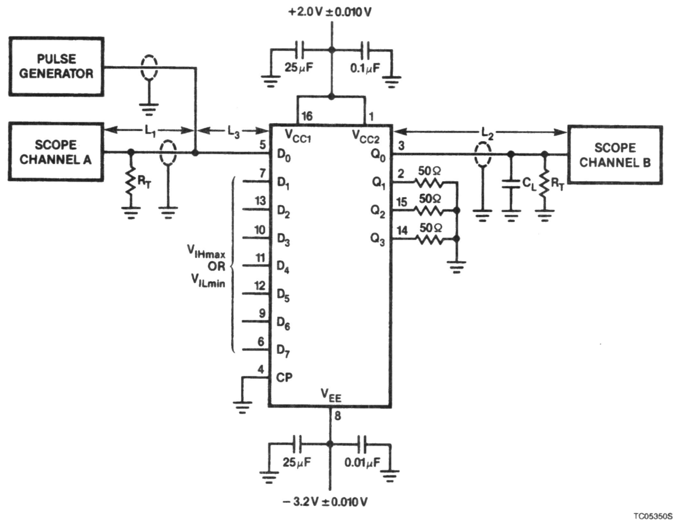


**Figure 6. Setup and Hold Times for Data to Clock**

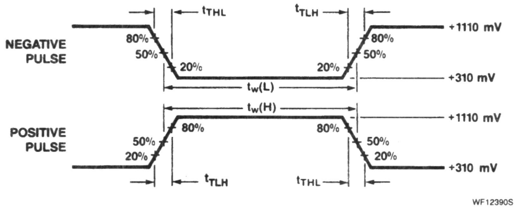
## TEST CIRCUITS AND WAVEFORMS


+2.0V ±0.010V
25µF
0.1µF
PULSE GENERATOR
SCOPE CHANNEL A
L1
L3
16
1
VCC1
VCC2
5
D0
3
Q0
L2
SCOPE CHANNEL B
RT
7
D1
2
50Ω
Q1
CL
RT
13
D2
15
50Ω
Q2
10
D3
14
50Ω
Q3
VIHmax
OR
VILmin
11
D4
12
D5
9
D6
6
D7
4
CP
VEE
8
25µF
0.01µF
−3.2V ±0.010V
TC05350S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1µF and 25µF from GND to $V_{CC}$, 0.01µF and 25µF from GND to $V_{EE}$ (0.01 and 0.1µF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than ¼ inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed ¼ inch (6mm).
6. $R_T = 50\Omega$ terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than ¼ inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance $\leq 3pF$.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed ¼ inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.

Figure 7. AC Test Circuit


tTHL
tTLH
NEGATIVE PULSE
80%
50%
20%
20%
80%
50%
+1110 mV
+310 mV
tw(L)
tw(H)
+1110 mV
POSITIVE PULSE
80%
80%
50%
20%
50%
20%
+310 mV
tTLH
tTHL
WF12390S

| INPUT PULSE REQUIREMENTS<br>$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$, $V_T = GND (0V)$ | | | | | |
|---|---|---|---|---|---|
| Family | Amplitude | Rep Rate | Pulse Width | $t_{TLH}$ | $t_{THL}$ |
| 10K ECL | 800mVp-p | 1MHz | 500ns | 2.0 ± 0.2ns | 2.0 ± 0.2ns |

Figure 8. Input Pulse Definition

# 10171
## Decoder

**Dual 1-of-4 Decoder With One Common and Two Individual Inputs (Active-LOW Outputs)**
***Product Specification***

**ECL Products**

## DESCRIPTION

The 10171 is a Dual 1-of-4 Decoder with common address inputs, one common ($\overline{E}$) and two individual enable ($\overline{E}_0$, $\overline{E}_1$) inputs.

The common enable (E), when HIGH, forces all outputs HIGH. All unused inputs can be left open due to integrated pull-down resistors which avoid the need for a supply voltage.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 10171 | 4.0ns | 65mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} = GND$; $V_{EE} = -5.2V$<br>$T_A = -30°C$ to $+85°C$ |
|---|---|
| Plastic DIP | 10171N |
| Ceramic DIP | 10171F |

## PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $A_0$, $A_1$ | Address Inputs |
| $\overline{E}$, $\overline{E}_0$, $\overline{E}_1$ | Enable Inputs |
| $Q_0 - Q_7$ | Data Outputs |

## PIN CONFIGURATION

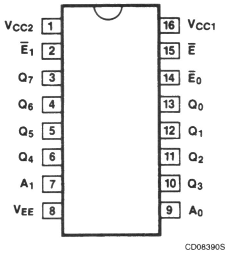

VCC2 1
Ē1 2
Q7 3
Q6 4
Q5 5
Q4 6
A1 7
VEE 8
16 VCC1
15 Ē
14 Ē0
13 Q0
12 Q1
11 Q2
10 Q3
9 A0
CD08390S

Figure 1

## LOGIC SYMBOL

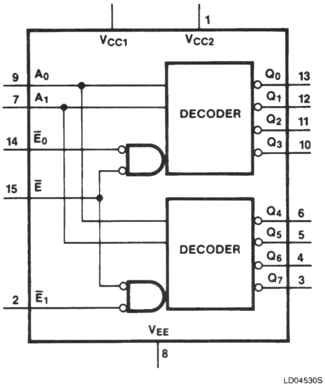

1
VCC1
VCC2
9 A0
7 A1
14 Ē0
15 Ē
2 Ē1
DECODER
DECODER
Q0 13
Q1 12
Q2 11
Q3 10
Q4 6
Q5 5
Q6 4
Q7 3
VEE
8
LD04530S

Figure 2

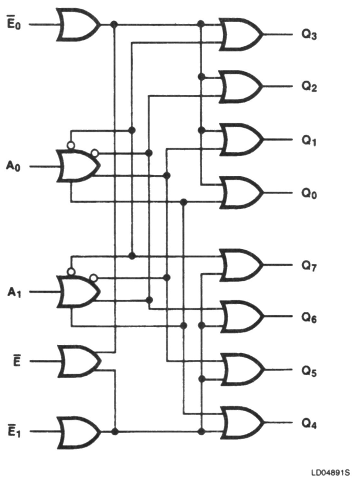

$\overline{E}_0$
$A_0$
$A_1$
$\overline{E}$
$\overline{E}_1$
$Q_3$
$Q_2$
$Q_1$
$Q_0$
$Q_7$
$Q_6$
$Q_5$
$Q_4$
LD04891S

Figure 3. Logic Diagram

## FUNCTION TABLE

| ENABLE INPUTS | | | INPUTS | | OUTPUTS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $\overline{E}$ | $\overline{E}_0$ | $\overline{E}_1$ | $A_0$ | $A_1$ | $Q_4$ | $Q_5$ | $Q_6$ | $Q_7$ | $Q_0$ | $Q_1$ | $Q_2$ | $Q_3$ |
| L | L | L | L | L | L | H | H | H | L | H | H | H |
| L | L | L | L | H | H | L | H | H | H | L | H | H |
| L | L | L | H | L | H | H | L | H | H | H | L | H |
| L | L | L | H | H | H | H | H | L | H | H | H | L |
| L | L | H | L | L | H | H | H | H | L | H | H | H |
| L | H | L | L | L | L | H | H | H | H | H | H | H |
| H | X | X | X | X | H | H | H | H | H | H | H | H |

Positive Logic:
H = HIGH state (the more positive voltage) = 1
L = LOW state (the less positive voltage) = 0
X = Don't Care

# Decoder 10171

**ABSOLUTE MAXIMUM RATINGS** (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | | 10K ECL | UNIT |
|---|---|---|---|---|
| $V_{EE}$ | Supply voltage | | −8.0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | | 0 to $V_{EE}$ | V |
| $I_O$ | Output source current | | −50 | mA |
| $T_S$ | Storage temperature | | −55 to +150 | °C |
| $T_J$ | Maximum junction temperature | Ceramic package | +165 | °C |
| | | Plastic package | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | 10K ECL | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | −5.2 | | V |
| $V_{IH}$ | HIGH level input voltage | $T_A = -30°C$ | | | −890 | mV |
| | | $T_A = +25°C$ | | | −810 | mV |
| | | $T_A = +85°C$ | | | −700 | mV |
| $V_{IHT}$ | HIGH level input threshold voltage | $T_A = -30°C$ | −1205 | | | mV |
| | | $T_A = +25°C$ | −1105 | | | mV |
| | | $T_A = +85°C$ | −1035 | | | mV |
| $V_{ILT}$ | LOW level input threshold voltage | $T_A = -30°C$ | | | −1500 | mV |
| | | $T_A = +25°C$ | | | −1475 | mV |
| | | $T_A = +85°C$ | | | −1440 | mV |
| $V_{IL}$ | LOW level input voltage | $T_A = -30°C$ | −1890 | | | mV |
| | | $T_A = +25°C$ | −1850 | | | mV |
| | | $T_A = +85°C$ | −1825 | | | mV |
| $T_A$ | Operating ambient temperature | | −30 | +25 | +85 | °C |

**NOTE:**

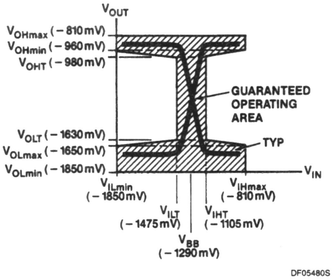
When operating at $V_{EE}$ other than specified voltage (−5.2V), the DC and AC Characteristics will vary slightly from specified values. (See table of DC Characteristics)

**DC ELECTRICAL CHARACTERISTICS** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$, output loading with 50Ω to −2.0V ±0.010V unless otherwise specified[1,3]

| PARAMETER | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | $T_A = -30°C$ | −1060 | | −890 | mV | Apply $V_{IHmax}$ to $\overline{E}$ input with $V_{ILmin}$ applied to all other inputs. |
| | | $T_A = +25°C$ | −960 | | −810 | mV | |
| | | $T_A = +85°C$ | −890 | | −700 | mV | |
| $V_{OHT}$ | HIGH level output threshold voltage | $T_A = -30°C$ | −1080 | | | mV | Apply $V_{IHT}$ to $\overline{E}$ input with $V_{ILmin}$ applied to all other inputs. |
| | | $T_A = +25°C$ | −980 | | | mV | |
| | | $T_A = +85°C$ | −910 | | | mV | |
| $V_{OLT}$ | LOW level output threshold voltage | $T_A = -30°C$ | | | −1655 | mV | For $Q_0$ and $Q_4$ outputs, apply $V_{ILT}$ to $\overline{E}$ input with $V_{ILmin}$ applied to all other inputs. Apply functional pattern to $A_0$ and $A_1$ for other output combinations. |
| | | $T_A = +25°C$ | | | −1630 | mV | |
| | | $T_A = +85°C$ | | | −1595 | mV | |
| $V_{OL}$ | LOW level output voltage | $T_A = -30°C$ | −1890 | | −1675 | mV | For $Q_0$ and $Q_4$ outputs, apply $V_{ILmin}$ to all inputs.<br>Apply functional pattern to $A_0$ and $A_1$ for other output combinations. |
| | | $T_A = +25°C$ | −1850 | | −1675 | mV | |
| | | $T_A = +85°C$ | 1825 | | −1615 | mV | |
| $I_{IH}$ | HIGH level input current | $T_A = -30°C$ | | | 350 | μA | Apply $V_{IHmax}$ to each input under test, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | $T_A = +25°C$ | | | 220 | μA | |
| | | $T_A = +85°C$ | | | 220 | μA | |
| $I_{IL}$ | LOW level input current | $T_A = -30°C$ | 0.5 | | | μA | Apply $V_{ILmin}$ to each input under test, one at a time, with $V_{IHmax}$ applied to all other inputs. |
| | | $T_A = +25°C$ | 0.5 | | | μA | |
| | | $T_A = +85°C$ | 0.3 | | | μA | |
| $-I_{EE}$ | $V_{EE}$ supply current | $T_A = -30°C$ | | | 85 | mA | Apply $V_{IHmax}$ to inputs. |
| | | $T_A = +25°C$ | | 65 | 77 | mA | |
| | | $T_A = +85°C$ | | | 85 | mA | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | $T_A = +25°C$ | | 0.016 | | V/V | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | 0.250 | | V/V | |
| $\frac{\Delta V_{BB}}{\Delta V_{EE}}$ | Reference bias voltage compensation | | | 0.148 | | V/V | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 4.


VOUT
VOHmax (−810mV)
VOHmin (−960mV)
VOHT (−980mV)
GUARANTEED OPERATING AREA
VOLT (−1630mV)
VOLmax (−1650mV)
VOLmin (−1850mV)
TYP
VIN
VILmin (−1850mV)
VIHmax (−810mV)
VILT (−1475mV)
VIHT (−1105mV)
VBB (−1290mV)
DF05480S

**NOTES:**

$V_{IHmax}$ – Maximum HIGH level input voltage (the most positive $V_{IH}$).
$V_{IHT}$ – HIGH level input threshold voltage.
$V_{ILT}$ – LOW level input threshold voltage.
$V_{ILmin}$ – Minimum LOW level input voltage (the most negative $V_{IL}$).
$V_{OHmax}$ – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition.
$V_{OHmin}$ – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition.
$V_{OHT}$ – HIGH level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLT}$ – LOW level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLmax}$ – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions.
$V_{OLmin}$ – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions.
$V_{BB}$ – Reference bias voltage. The internally generated reference voltage which is used to set the input and output threshold level.

**Figure 4. Transfer Characteristics**

## AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$

| PARAMETER | | $T_A = -30°C$ | | $T_A = +25°C$ | | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Typ | Max | Min | Max | | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$A_0$, $A_1$ to $Q_n$ | 1.5<br>1.5 | 6.2<br>6.2 | 1.5<br>1.5 | 4.0<br>4.0 | 6.0<br>6.0 | 1.5<br>1.5 | 6.4<br>6.4 | ns<br>ns | Figs. 5, 6, 7 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$\overline{E}$, $\overline{E}_0$, $\overline{E}_1$ to $Q_n$ | 1.5<br>1.5 | 6.2<br>6.2 | 1.5<br>1.5 | 4.0<br>4.0 | 6.0<br>6.0 | 1.5<br>1.5 | 6.4<br>6.4 | ns<br>ns | Figs. 5, 6, 7 |
| $t_{TLH}$<br>$t_{THL}$ | Transition time<br>20% to 80%, 80% to 20% | 1.0<br>1.0 | 3.3<br>3.3 | 1.1<br>1.1 | 2.0<br>2.0 | 3.3<br>3.3 | 1.1<br>1.1 | 3.4<br>3.4 | ns<br>ns | Figs. 5, 6, 7 |

## AC WAVEFORMS

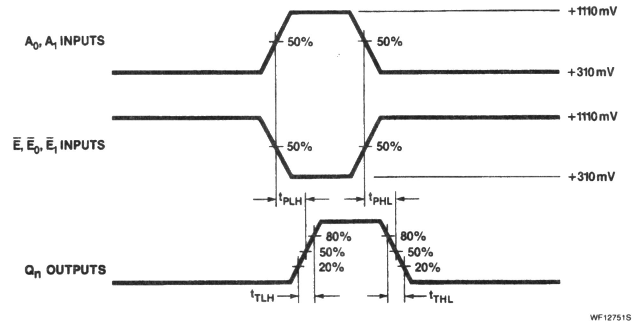
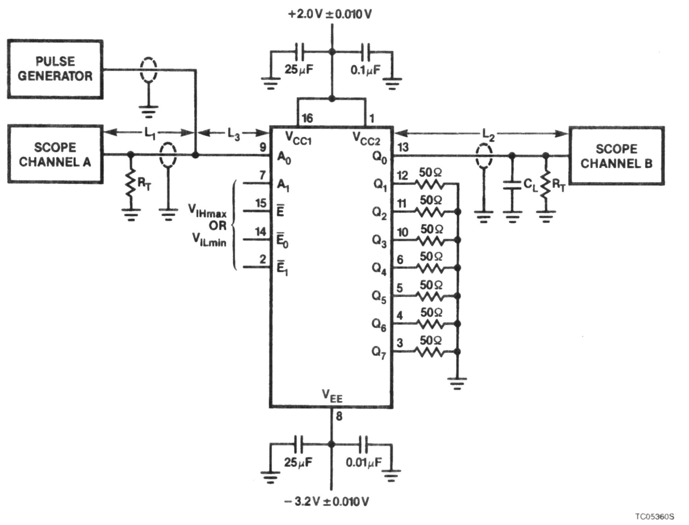

A0, A1 INPUTS
50%
50%
+1110mV
+310mV
Ē, Ē0, Ē1 INPUTS
50%
50%
+1110mV
+310mV
tPLH
tPHL
Qn OUTPUTS
80%
50%
20%
80%
50%
20%
tTLH
tTHL
WF12751S

**Figure 5. Propagation Delay and Transition Times for Address to Output**

# Decoder 10171

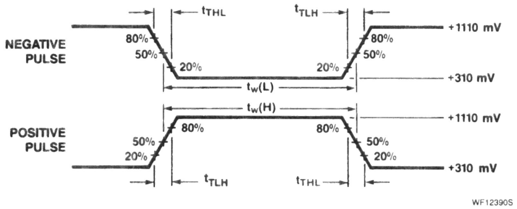
## TEST CIRCUITS AND WAVEFORMS


+2.0 V ±0.010 V
25μF
0.1μF
PULSE GENERATOR
SCOPE CHANNEL A
L1
L3
L2
$R_T$
16
1
$V_{CC1}$
$V_{CC2}$
9
$A_0$
7
$A_1$
15
$\bar{E}$
14
$\bar{E}_0$
2
$\bar{E}_1$
$V_{IHmax}$ OR $V_{ILmin}$
13
$Q_0$
12
$Q_1$
11
$Q_2$
10
$Q_3$
6
$Q_4$
5
$Q_5$
4
$Q_6$
3
$Q_7$
50Ω
$C_L$
SCOPE CHANNEL B
$V_{EE}$
8
25μF
0.01μF
−3.2V ±0.010V
TC05360S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1μF and 25μF from GND to $V_{CC}$, 0.01μF and 25μF from GND to $V_{EE}$ (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than ¼ inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed ¼ inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than ¼ inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance ⩽ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed ¼ inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.

Figure 6. AC Test Circuit


NEGATIVE PULSE
POSITIVE PULSE
$t_{THL}$
$t_{TLH}$
80%
50%
20%
$t_w(L)$
$t_w(H)$
+1110 mV
+310 mV
WF12390S

| INPUT PULSE REQUIREMENTS<br>$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$, $V_T$ = GND (0V) | | | | | |
|---|---|---|---|---|---|
| Family | Amplitude | Rep Rate | Pulse Width | $t_{TLH}$ | $t_{THL}$ |
| 10K ECL | 800mVp-p | 1MHz | 500ns | 2.0 ±0.2ns | 2.0 ±0.2ns |

Figure 7. Input Pulse Definition

Signetics

**ECL Products**

# 10172
## Decoder

**Dual 1-of-4 Decoder With One Common and Two Individual Inputs (Active-HIGH Outputs)**
***Product Specification***

## DESCRIPTION

The 10172 is a Dual 1-of-4 Decoder with common address inputs, one common and two individual enable ($E_0$, $E_1$) inputs. The common Enable ($\overline{E}$), when HIGH, forces all outputs LOW. All unused inputs can be left open due to integrated pull-down resistors which avoid the need for a supply voltage.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 10172 | 4.0ns | 62mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} = GND$; $V_{EE} = -5.2V$<br>$T_A = -30°C$ to $+85°C$ |
|---|---|
| Plastic DIP | 10172N |
| Ceramic DIP | 10172F |

## PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $A_0$, $A_1$ | Address Inputs |
| $\overline{E}$, $E_0$, $E_1$ | Enable Inputs |
| $Q_0 - Q_7$ | Data Outputs |

## PIN CONFIGURATION

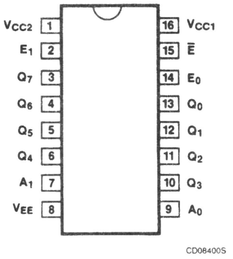

VCC2 1
E1 2
Q7 3
Q6 4
Q5 5
Q4 6
A1 7
VEE 8
16 VCC1
15 Ē
14 E0
13 Q0
12 Q1
11 Q2
10 Q3
9 A0
CD08400S

Figure 1

## LOGIC SYMBOL

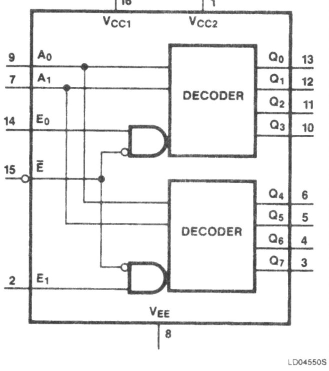

16
1
VCC1
VCC2
9 A0
7 A1
14 E0
15 Ē
2 E1
DECODER
DECODER
Q0 13
Q1 12
Q2 11
Q3 10
Q4 6
Q5 5
Q6 4
Q7 3
VEE
8
LD04550S

Figure 2

## Decoder

## 10172

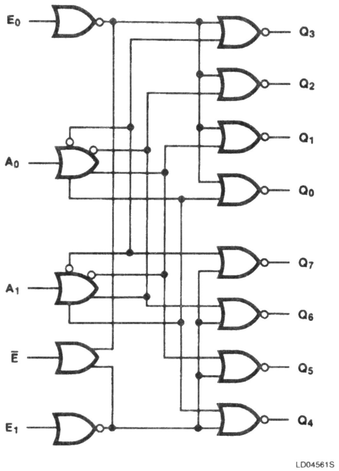

$E_0$
$A_0$
$A_1$
$\overline{E}$
$E_1$
$Q_3$
$Q_2$
$Q_1$
$Q_0$
$Q_7$
$Q_6$
$Q_5$
$Q_4$
LD04561S

**Figure 3. Logic Diagram**

## FUNCTION TABLE

| ENABLE INPUTS | | | INPUTS | | OUTPUTS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $\overline{E}$ | $E_1$ | $E_0$ | $A_0$ | $A_1$ | $Q_4$ | $Q_5$ | $Q_6$ | $Q_7$ | $Q_0$ | $Q_1$ | $Q_2$ | $Q_3$ |
| L | H | H | L | L | H | L | L | L | H | L | L | L |
| L | H | H | L | H | L | H | L | L | L | H | L | L |
| L | H | H | H | L | L | L | H | L | L | L | H | L |
| L | H | H | H | H | L | L | L | H | L | L | L | H |
| L | L | H | L | L | H | L | L | L | L | L | L | L |
| L | H | L | L | L | L | L | L | L | H | L | L | L |
| H | X | X | X | X | L | L | L | L | L | L | L | L |

Positive Logic:
H = HIGH state (the more positive voltage) = 1
L = LOW state (the less positive voltage) = 0
X = Don't Care

## ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | | 10K ECL | UNIT |
|---|---|---|---|---|
| $V_{EE}$ | Supply voltage | | −8.0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | | 0 to $V_{EE}$ | V |
| $I_O$ | Output source current | | −50 | mA |
| $T_S$ | Storage temperature | | −55 to +150 | °C |
| $T_J$ | Maximum junction temperature | Ceramic package | +165 | °C |
| | | Plastic package | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | 10K ECL | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | −5.2 | | V |
| $V_{IH}$ | HIGH level input voltage | $T_A = -30°C$ | | | −890 | mV |
| | | $T_A = +25°C$ | | | −810 | mV |
| | | $T_A = +85°C$ | | | −700 | mV |
| $V_{IHT}$ | HIGH level input threshold voltage | $T_A = -30°C$ | −1205 | | | mV |
| | | $T_A = +25°C$ | −1105 | | | mV |
| | | $T_A = +85°C$ | −1035 | | | mV |
| $V_{ILT}$ | LOW level input threshold voltage | $T_A = -30°C$ | | | −1500 | mV |
| | | $T_A = +25°C$ | | | −1475 | mV |
| | | $T_A = +85°C$ | | | −1440 | mV |
| $V_{IL}$ | LOW level input voltage | $T_A = -30°C$ | −1890 | | | mV |
| | | $T_A = +25°C$ | −1850 | | | mV |
| | | $T_A = +85°C$ | −1825 | | | mV |
| $T_A$ | Operating ambient temperature | | −30 | +25 | +85 | °C |

**NOTE:**

When operating at $V_{EE}$ other than specified voltage (−5.2V), the DC and AC Characteristics will vary slightly from specified values.
(See table of DC Characteristics)

**DC ELECTRICAL CHARACTERISTICS** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$, output loading with 50Ω to −2.0V ±0.010V unless otherwise specified[1,3]

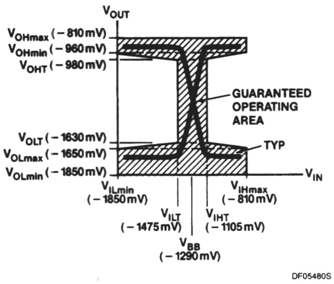
| PARAMETER | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | $T_A = -30°C$ | −1060 | | −890 | mV | For $Q_0$ and $Q_4$ outputs, apply $V_{IHmax}$ to $E_0$ and $E_1$ inputs with $V_{ILmin}$ applied to all other inputs. |
| | | $T_A = +25°C$ | −960 | | −810 | mV | |
| | | $T_A = +85°C$ | −890 | | −700 | mV | |
| $V_{OHT}$ | HIGH level output threshold voltage | $T_A = -30°C$ | −1080 | | | mV | For $Q_0$ output, apply $V_{IHT}$ to $E_1$ input with $V_{ILmin}$ applied to all other inputs. |
| | | $T_A = +25°C$ | −980 | | | mV | |
| | | $T_A = +85°C$ | −910 | | | mV | |
| $V_{OLT}$ | LOW level output threshold voltage | $T_A = -30°C$ | | | −1655 | mV | Apply $V_{IHT}$ to $\overline{E}$ input with $V_{ILmin}$ applied to all other inputs. |
| | | $T_A = +25°C$ | | | −1630 | mV | |
| | | $T_A = +85°C$ | | | −1595 | mV | |
| $V_{OL}$ | LOW level output voltage | $T_A = -30°C$ | −1890 | | −1675 | mV | Apply $V_{IHmax}$ to $\overline{E}$ input with $V_{ILmin}$ applied to all other inputs. |
| | | $T_A = +25°C$ | −1850 | | −1650 | mV | |
| | | $T_A = +85°C$ | −1825 | | −1615 | mV | |
| $I_{IH}$ | HIGH level input current | $T_A = -30°C$ | | | 350 | μA | Apply $V_{IHmax}$ to each input under test, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | $T_A = +25°C$ | | | 220 | μA | |
| | | $T_A = +85°C$ | | | 220 | μA | |
| $I_{IL}$ | LOW level input current | $T_A = -30°C$ | 0.5 | | | μA | Apply $V_{ILmin}$ to each input under test, one at a time, with $V_{IHmax}$ applied to all other inputs. |
| | | $T_A = +25°C$ | 0.5 | | | μA | |
| | | $T_A = +85°C$ | 0.3 | | | μA | |
| $-I_{EE}$ | $V_{EE}$ supply current | $T_A = -30°C$ | | | 85 | mA | |
| | | $T_A = +25°C$ | | 62 | 77 | mA | |
| | | $T_A = +85°C$ | | | 85 | mA | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | $T_A = +25°C$ | | 0.016 | | V/V | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | 0.250 | | V/V | |
| $\frac{\Delta V_{BB}}{\Delta V_{EE}}$ | Reference bias voltage compensation | | | 0.148 | | V/V | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst-case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has beeb established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 4.

## Decoder

## 10172


V_OUT
V_OHmax (−810mV)
V_OHmin (−960mV)
V_OHT (−980mV)
GUARANTEED OPERATING AREA
V_OLT (−1630mV)
V_OLmax (−1650mV)
V_OLmin (−1850mV)
TYP
V_IN
V_ILmin (−1850mV)
V_IHmax (−810mV)
V_ILT (−1475mV)
V_IHT (−1105mV)
V_BB (−1290mV)
DF05480S

**NOTES:**

$V_{IHmax}$ – Maximum HIGH level input voltage (the most positive $V_{IH}$).
$V_{IHT}$ – HIGH level input threshold voltage.
$V_{ILT}$ – LOW level input threshold voltage.
$V_{ILmin}$ – Minimum LOW level input voltage (the most negative $V_{IL}$).
$V_{OHmax}$ – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition.
$V_{OHmin}$ – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition.
$V_{OHT}$ – HIGH level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLT}$ – LOW level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLmax}$ – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions.
$V_{OLmin}$ – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions.
$V_{BB}$ – Reference bias voltage. The internally generated reference voltage which is used to set the input and output threshold level.

**Figure 4. Transfer Characteristics**

## AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$

| PARAMETER | | $T_A = -30°C$ | | $T_A = +25°C$ | | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Typ | Max | Min | Max | | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$A_n$, $E_n$ to $Q_n$ | 1.5<br>1.5 | 6.2<br>6.2 | 1.5<br>1.5 | 4.0<br>4.0 | 6.0<br>6.0 | 1.5<br>1.5 | 6.4<br>6.4 | ns<br>ns | Figs. 5, 6, 7 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$\bar{E}$ to $Q_n$ | 1.5<br>1.5 | 6.2<br>6.2 | 1.5<br>1.5 | 4.0<br>4.0 | 6.0<br>6.0 | 1.5<br>1.5 | 6.4<br>6.4 | ns<br>ns | Figs. 5, 6, 7 |
| $t_{TLH}$<br>$t_{THL}$ | Transition time<br>20% to 80%, 80% to 20% | 1.0<br>1.0 | 3.3<br>3.3 | 1.1<br>1.1 | 2.0<br>2.0 | 3.3<br>3.3 | 1.1<br>1.1 | 3.4<br>3.4 | ns<br>ns | Figs. 5, 6, 7 |

## AC WAVEFORMS

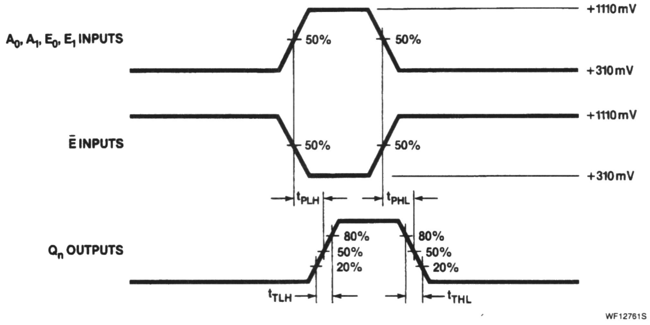
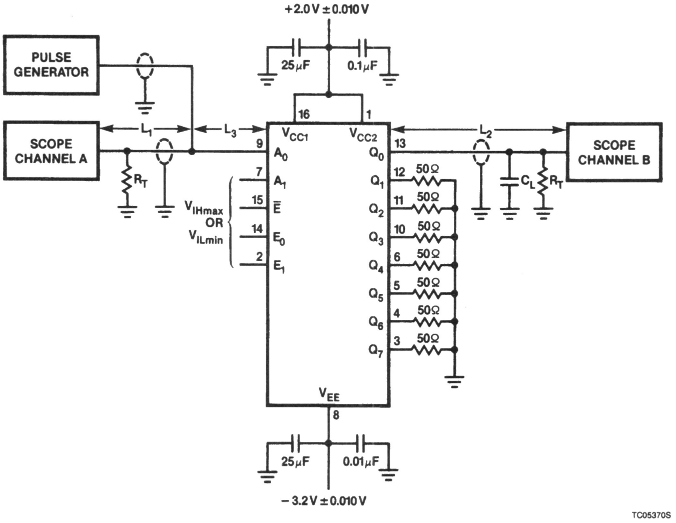

A_0, A_1, E_0, E_1 INPUTS
+1110mV
50%
50%
+310mV
Ē INPUTS
+1110mV
50%
50%
+310mV
t_PLH
t_PHL
Q_n OUTPUTS
80%
50%
20%
80%
50%
20%
t_TLH
t_THL
WF12761S

**Figure 5. Propagation Delay and Transition Times for Address and Enable Inputs to Outputs**

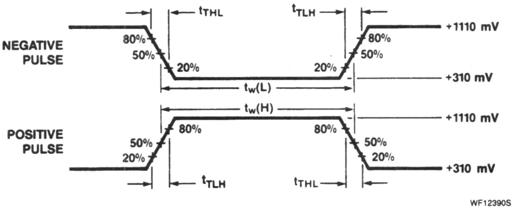
## TEST CIRCUITS AND WAVEFORMS


+2.0V ± 0.010V
25μF
0.1μF
PULSE GENERATOR
SCOPE CHANNEL A
SCOPE CHANNEL B
L1
L3
L2
16
1
9
13
$V_{CC1}$
$V_{CC2}$
$A_0$
$Q_0$
7
$A_1$
$Q_1$
15
$\overline{E}$
$Q_2$
14
$E_0$
$Q_3$
2
$E_1$
$Q_4$
$Q_5$
$Q_6$
$Q_7$
12
11
10
6
5
4
3
50Ω
$R_T$
$C_L$
$V_{IHmax}$ OR $V_{ILmin}$
$V_{EE}$
8
25μF
0.01μF
−3.2V ± 0.010V
TC05370S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1μF and 25μF from GND to $V_{CC}$, 0.01μF and 25μF from GND to $V_{EE}$ (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than ¼ inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed ¼ inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than ¼ inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance ≤ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed ¼ inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.

**Figure 6. AC Test Circuit**


NEGATIVE PULSE
POSITIVE PULSE
$t_{THL}$
$t_{TLH}$
80%
50%
20%
$t_w(L)$
$t_w(H)$
+1110 mV
+310 mV
WF12390S

| INPUT PULSE REQUIREMENTS<br>$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$, $V_T$ = GND (0V) | | | | | |
|---|---|---|---|---|---|
| **Family** | **Amplitude** | **Rep Rate** | **Pulse Width** | $t_{TLH}$ | $t_{THL}$ |
| 10K ECL | 800mVp-p | 1MHz | 500ns | 2.0 ± 0.2ns | 2.0 ± 0.2ns |

**Figure 7. Input Pulse Definition**

**Signetics**

# 10173

## Multiplexer/Latch

**Quad 2-Input Multiplexer With Latched Outputs**
***Product Specification***

**ECL Products**

## DESCRIPTION

The 10173 is a quad 2-input multiplexer with latched outputs. Each multiplexer has two inputs, selected by the common Select (S) input. Outputs are latched when the clock is HIGH. All unused inputs must be tied LOW to $V_{IL}$ or $V_{EE}$.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 10173 | 2.5ns | 53mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} = \text{GND}$; $V_{EE} = -5.2V$<br>$T_A = -30°C$ to $+85°C$ |
|---|---|
| Plastic DIP | 10173N |
| Ceramic DIP | 10173F |

## PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_0 - D_7$ | Data Inputs |
| S | Select Input |
| CP | Clock Input |
| $Q_0 - Q_3$ | Data Outputs |

## PIN CONFIGURATION

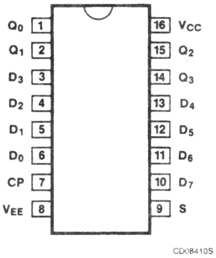

Q0 1
Q1 2
D3 3
D2 4
D1 5
D0 6
CP 7
VEE 8
16 VCC
15 Q2
14 Q3
13 D4
12 D5
11 D6
10 D7
9 S
CD08410S

Figure 1

## LOGIC SYMBOL

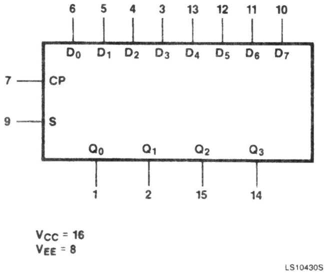

6
5
4
3
13
12
11
10
D0
D1
D2
D3
D4
D5
D6
D7
7
CP
9
S
Q0
Q1
Q2
Q3
1
2
15
14
VCC = 16
VEE = 8
LS10430S

Figure 2

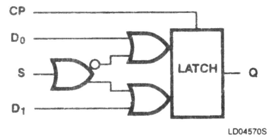


Figure 3. Logic Diagram

## FUNCTION TABLE

| S | CP | $Q_{n+1}$ |
|---|---|---|
| H | L | $D_0$ |
| L | L | $D_1$ |
| X | H | $Q_n$ |

Positive Logic:
H = HIGH state (the more positive voltage) = 1
L = LOW state (the less positive voltage) = 0
X = Don't Care

## ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | | 10K ECL | UNIT |
|---|---|---|---|---|
| $V_{EE}$ | Supply voltage | | -8.0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | | 0 to $V_{EE}$ | V |
| $I_O$ | Output source current | | -50 | mA |
| $T_S$ | Storage temperature | | -55 to +150 | °C |
| $T_J$ | Maximum junction temperature | Ceramic package | +165 | °C |
| | | Plastic package | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | 10K ECL | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | -5.2 | | V |
| $V_{IH}$ | HIGH level input voltage | $T_A$ = -30°C | | | -890 | mV |
| | | $T_A$ = +25°C | | | -810 | mV |
| | | $T_A$ = +85°C | | | -700 | mV |
| $V_{IHT}$ | HIGH level input threshold voltage | $T_A$ = -30°C | -1205 | | | mV |
| | | $T_A$ = +25°C | -1105 | | | mV |
| | | $T_A$ = +85°C | -1035 | | | mV |
| $V_{ILT}$ | LOW level input threshold voltage | $T_A$ = -30°C | | | -1500 | mV |
| | | $T_A$ = +25°C | | | -1475 | mV |
| | | $T_A$ = +85°C | | | -1440 | mV |
| $V_{IL}$ | LOW level input voltage | $T_A$ = -30°C | -1890 | | | mV |
| | | $T_A$ = +25°C | -1850 | | | mV |
| | | $T_A$ = +85°C | -1825 | | | mV |
| $T_A$ | Operating ambient temperature | | -30 | +25 | +85 | °C |

**NOTE:**
When operating at $V_{EE}$ other than specified voltage (-5.2V), the DC and AC Characteristics will vary slightly from specified values. (See table of DC Characteristics)

## DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$, output loading with 50Ω to $-2.0V \pm 0.010V$ unless otherwise specified[1,3]

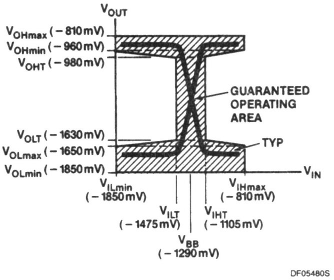
| PARAMETER | | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | | $T_A = -30°C$ | -1060 | | -890 | mV | Apply $V_{IHmax}$ to $D_1$ input, with $V_{ILmin}$ applied to $D_0$, CP and S inputs. |
| | | | $T_A = +25°C$ | -960 | | -810 | mV | |
| | | | $T_A = +85°C$ | -890 | | -700 | mV | |
| $V_{OHT}$ | HIGH level output threshold voltage | | $T_A = -30°C$ | -1080 | | | mV | Apply $V_{IHT}$ to $D_1$ input, with $V_{ILmin}$ applied to $D_0$, CP and S inputs. |
| | | | $T_A = -25°C$ | -980 | | | mV | |
| | | | $T_A = -85°C$ | -910 | | | mV | |
| $V_{OLT}$ | LOW level output threshold voltage | | $T_A = -30°C$ | | =10 | -1655 | mV | Apply $V_{ILT}$ to $D_1$ input with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = -25°C$ | | | -1630 | mV | |
| | | | $T_A = -85°C$ | | | -1595 | mV | |
| $V_{OL}$ | LOW level output voltage | | $T_A = -30°C$ | -1890 | | -1675 | mV | Apply $V_{ILmin}$ to all inputs. |
| | | | $T_A = +25°C$ | -1850 | | -1650 | mV | |
| | | | $T_A = +85°C$ | -1825 | | -1615 | mV | |
| $I_{IH}$ | HIGH level input current | $D_n$ inputs | $T_A = -30°C$ | | | 470 | µA | Apply $V_{IHmax}$ to each input under test, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | | | 295 | µA | |
| | | | $T_A = +85°C$ | | | 295 | µA | |
| | | S, CP inputs | $T_A = -30°C$ | | | 400 | µA | Apply $V_{IHmax}$ to S and CP inputs under test, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | | | 250 | µA | |
| | | | $T_A = +85°C$ | | | 250 | µA | |
| $I_{IL}$ | LOW level input current | | $T_A = -30°C$ | 0.5 | | | µA | Apply $V_{ILmin}$ to each input, one at a time, with $V_{IHmax}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | 0.5 | | | µA | |
| | | | $T_A = +85°C$ | 0.3 | | | µA | |
| $-I_{EE}$ | $V_{EE}$ supply current | | $T_A = -30°C$ | | | 73 | mA | |
| | | | $T_A = +25°C$ | | 53 | 66 | mA | |
| | | | $T_A = +85°C$ | | | 73 | mA | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | | $T_A = +25°C$ | | 0.016 | | V/V | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | | 0.250 | | V/V | |
| $\frac{\Delta V_{BB}}{\Delta V_{EE}}$ | Reference bias voltage compensation | | | | 0.148 | | V/V | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst-case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 4.

# Multiplexer/Latch

# 10173



**NOTES:**

$V_{IHmax}$ – Maximum HIGH level input voltage (the most positive $V_{IH}$).
$V_{IHT}$ – HIGH level input threshold voltage.
$V_{ILT}$ – LOW level input threshold voltage.
$V_{ILmin}$ – Minimum LOW level input voltage (the most negative $V_{IL}$).
$V_{OHmax}$ – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition.
$V_{OHmin}$ – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition.
$V_{OHT}$ – HIGH level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLT}$ – LOW level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLmax}$ – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions.
$V_{OLmin}$ – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions.
$V_{BB}$ – Reference bias voltage. The internally generated reference voltage which is used to set the input and output threshold level.

**Figure 4. Transfer Characteristics**

## AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$

| PARAMETER | | $T_A = -30°C$ | | $T_A = +25°C$ | | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Typ | Max | Min | Max | | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$D_n$ to $Q_n$ | 0.8<br>0.8 | 3.7<br>3.7 | 1.0<br>1.0 | 2.5<br>2.5 | 3.5<br>3.5 | 1.1<br>1.1 | 5.3<br>5.3 | ns<br>ns | Figs. 5, 7, 8 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>CP to $Q_n$ | 1.6<br>1.6 | 7.2<br>7.2 | 1.6<br>1.6 | 4.5<br>4.5 | 6.8<br>6.8 | 1.4<br>1.4 | 6.8<br>6.8 | ns<br>ns | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>S to $Q_n$ | 1.1<br>1.1 | 6.2<br>6.2 | 1.3<br>1.3 | 3.5<br>3.5 | 5.7<br>5.7 | 1.2<br>1.2 | 6.7<br>6.7 | ns<br>ns | |
| $t_s$ | Setup time $D_n$ to CP | 2.0 | | 2.0 | 1.5 | | 2.0 | | ns | Figs. 6, 7, 8 |
| $t_h$ | Hold time $D_n$ to CP | 2.5 | | 2.5 | 0 | | 2.5 | | ns | |
| $t_s$ | Setup time S to CP | 3.0 | | 3.0 | 2.5 | | 3.0 | | ns | |
| $t_h$ | Hold time S to CP | 1.5 | | 1.5 | 0.5 | | 1.5 | | ns | |
| $t_{TLH}$<br>$t_{THL}$ | Transition time<br>20% to 80%, 80% to 20% | 1.2<br>1.2 | 4.0<br>4.0 | 1.5<br>1.5 | 2.0<br>2.0 | 3.5<br>3.5 | 1.4<br>1.4 | 4.0<br>4.0 | ns<br>ns | Figs. 5, 7, 8 |

## AC WAVEFORMS

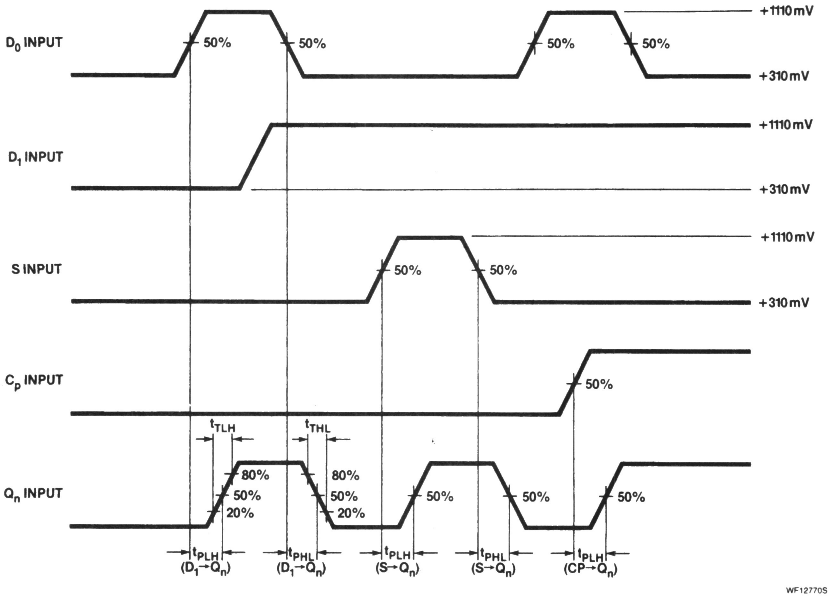

$D_0$ INPUT
$D_1$ INPUT
S INPUT
$C_p$ INPUT
$Q_n$ INPUT
50%
50%
50%
50%
+1110mV
+310mV
+1110mV
+310mV
+1110mV
+310mV
50%
50%
50%
$t_{TLH}$
$t_{THL}$
80%
50%
20%
80%
50%
20%
50%
50%
50%
$t_{PLH}$ ($D_1 \rightarrow Q_n$)
$t_{PHL}$ ($D_1 \rightarrow Q_n$)
$t_{PLH}$ ($S \rightarrow Q_n$)
$t_{PHL}$ ($S \rightarrow Q_n$)
$t_{PLH}$ ($CP \rightarrow Q_n$)
WF12770S

Figure 5. Propagation Delay and Transition Times for Data to Output

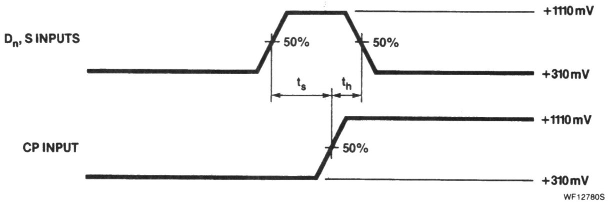
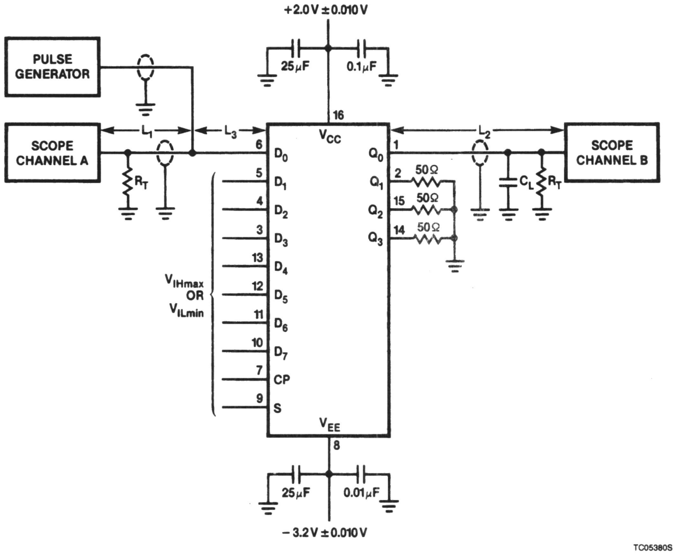

$D_n$, S INPUTS
CP INPUT
50%
50%
+1110mV
+310mV
$t_s$
$t_h$
+1110mV
50%
+310mV
WF12780S

Figure 6. Setup and Hold Times for Data and Select to Clock

## Multiplexer/Latch

## 10173

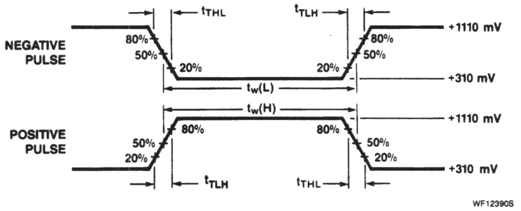
### TEST CIRCUITS AND WAVEFORMS


+2.0V ±0.010V
25μF
0.1μF
PULSE GENERATOR
SCOPE CHANNEL A
$L_1$
$L_3$
$R_T$
16
$V_{CC}$
6 $D_0$
5 $D_1$
4 $D_2$
3 $D_3$
13 $D_4$
12 $D_5$
11 $D_6$
10 $D_7$
7 CP
9 S
$V_{IHmax}$ OR $V_{ILmin}$
$V_{EE}$
8
$Q_0$ 1
$Q_1$ 2
$Q_2$ 15
$Q_3$ 14
50Ω
50Ω
50Ω
$L_2$
$C_L$
$R_T$
SCOPE CHANNEL B
25μF
0.01μF
−3.2V ±0.010V
TC05380S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1μF and 25μF from GND to $V_{CC}$, 0.01μF and 25μF from GND to $V_{EE}$ (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than ¼ inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed ¼ inch (6mm).
6. $R_T = 50\Omega$ terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than ¼ inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance $\leqslant 3pF$.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed ¼ inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.

Figure 7. AC Test Circuit


NEGATIVE PULSE
POSITIVE PULSE
$t_{THL}$
$t_{TLH}$
80%
50%
20%
$t_w(L)$
$t_w(H)$
+1110 mV
+310 mV
WF12390S

| INPUT PULSE REQUIREMENTS<br>$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$, $V_T = GND\ (0V)$ | | | | | |
|---|---|---|---|---|---|
| **Family** | **Amplitude** | **Rep Rate** | **Pulse Width** | **$t_{TLH}$** | **$t_{THL}$** |
| 10K ECL | 800mVp-p | 1MHz | 500ns | 2.0 ±0.2ns | 2.0 ±0.2ns |

Figure 8. Input Pulse Definition

# 10174
## Multiplexer

**Dual 4-to-1 Multiplexer (With Output Enable)**
***Product Specification***

**ECL Products**

## DESCRIPTION

The 10174 is a Dual 4-to-1 Multiplexer with output enable input. The 10174 performs two 4-input multiplexer functions. The output of each multiplexer reflects one of the 4 data inputs determined by the states on the two select inputs. An enable input is provided for easy bit expansion by wire-ORing several multiplexers. Each output will go LOW with the enable input in the HIGH state. All unused inputs can be left open due to integrated pull-down resistors which avoid the need for a supply voltage.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 10174 | 3.5ns | 58mA |

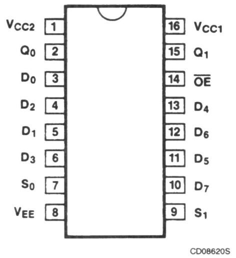
## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} = GND$; $V_{EE} = -5.2V$<br>$T_A = -30°C$ to $+85°C$ |
|---|---|
| Plastic DIP | 10174N |
| Ceramic DIP | 10174F |

## PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_0 - D_7$ | Data Inputs |
| $S_0$, $S_1$ | Select Inputs |
| $\overline{OE}$ | Output Enable Input |
| $Q_0$, $Q_1$ | Data Outputs |

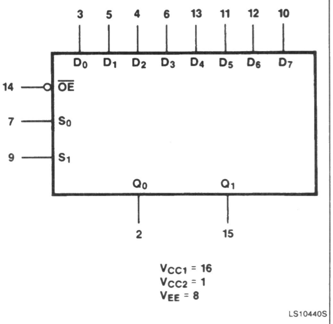
## PIN CONFIGURATION



VCC2 1
Q0 2
D0 3
D2 4
D1 5
D3 6
S0 7
VEE 8
16 VCC1
15 Q1
14 OE
13 D4
12 D6
11 D5
10 D7
9 S1
CD08620S

Figure 1

## LOGIC SYMBOL



3
5
4
6
13
11
12
10
D0
D1
D2
D3
D4
D5
D6
D7
14
OE
7
S0
9
S1
Q0
Q1
2
15
VCC1 = 16
VCC2 = 1
VEE = 8
LS10440S

Figure 2

# Multiplexer

# 10174

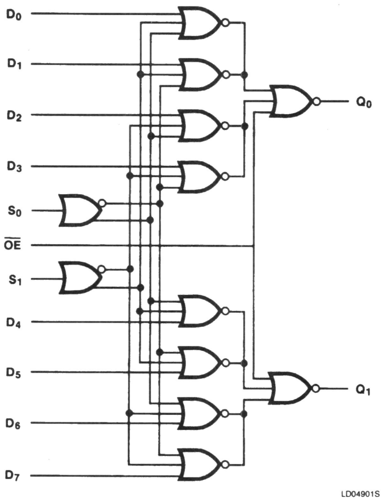

D0
D1
D2
D3
S0
OE
S1
D4
D5
D6
D7
Q0
Q1
LD04901S

Figure 3. Logic Diagram

## FUNCTION TABLE

| INPUTS | | | OUTPUTS | |
|---|---|---|---|---|
| $S_0$ | $S_1$ | $\overline{OE}$ | $Q_0$ | $Q_1$ |
| L | L | L | $D_0$ | $D_4$ |
| H | L | L | $D_1$ | $D_5$ |
| L | H | L | $D_2$ | $D_6$ |
| H | H | L | $D_3$ | $D_7$ |
| X | X | H | L | L |

Positive Logic:
H = HIGH state (the more positive voltage) = 1
L = LOW state (the less positive voltage) = 0
X = Don't Care

## Multiplexer 10174

### ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | | 10K ECL | UNIT |
|---|---|---|---|---|
| $V_{EE}$ | Supply voltage | | -8.0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | | 0 to $V_{EE}$ | V |
| $I_O$ | Output source current | | -50 | mA |
| $T_S$ | Storage temperature | | -55 to +150 | °C |
| $T_J$ | Maximum junction temperature | Ceramic package | +165 | °C |
| | | Plastic package | +150 | °C |

### DC OPERATING CONDITIONS

| PARAMETER | | | 10K ECL | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | -5.2 | | V |
| $V_{IH}$ | HIGH level input voltage | $T_A$ = -30°C | | | -890 | mV |
| | | $T_A$ = +25°C | | | -810 | mV |
| | | $T_A$ = +85°C | | | -700 | mV |
| $V_{IHT}$ | HIGH level input threshold voltage | $T_A$ = -30°C | -1205 | | | mV |
| | | $T_A$ = +25°C | -1105 | | | mV |
| | | $T_A$ = +85°C | -1035 | | | mV |
| $V_{ILT}$ | LOW level input threshold voltage | $T_A$ = -30°C | | | -1500 | mV |
| | | $T_A$ = +25°C | | | -1475 | mV |
| | | $T_A$ = +85°C | | | -1440 | mV |
| $V_{IL}$ | LOW level input voltage | $T_A$ = -30°C | -1890 | | | mV |
| | | $T_A$ = +25°C | -1850 | | | mV |
| | | $T_A$ = +85°C | -1825 | | | mV |
| $T_A$ | Operating ambient temperature | | -30 | +25 | +85 | °C |

**NOTE:**
When operating at $V_{EE}$ other than specified voltage (-5.2V), the DC and AC Characteristics will vary slightly from specified values.
(See table of DC Characteristics)

# Multiplexer 10174

## DC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$, output loading with 50Ω to −2.0V ±0.010V unless otherwise specified[1,3]

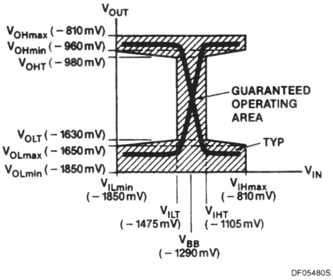
| PARAMETER | | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | | $T_A = -30°C$ | −1060 | | −890 | mV | Apply $V_{IHmax}$ to $D_0$ and $D_4$ inputs, with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | −960 | | −810 | mV | |
| | | | $T_A = +85°C$ | −890 | | −700 | mV | |
| $V_{OHT}$ | HIGH level output threshold voltage | | $T_A = -30°C$ | −1080 | | | mV | Apply $V_{IHT}$ to $D_0$ input, with $V_{ILmin}$ applied to all other inputs. Measure $Q_0$.<br>Apply $V_{IHT}$ to $D_4$ input, with $V_{ILmin}$ applied to all other inputs. Measure $Q_1$. |
| | | | $T_A = -25°C$ | −980 | | | mV | |
| | | | $T_A = -85°C$ | −910 | | | mV | |
| $V_{OLT}$ | LOW level output threshold voltage | | $T_A = -30°C$ | | | −1655 | mV | Apply $V_{IHT}$ to $\overline{OE}$ input with $V_{ILmin}$ applied to all other inputs |
| | | | $T_A = -25°C$ | | | −1630 | mV | |
| | | | $T_A = -85°C$ | | | −1595 | mV | |
| $V_{OL}$ | LOW level output voltage | | $T_A = -30°C$ | −1890 | | −1675 | mV | Apply $V_{IHmax}$ to $\overline{OE}$ input with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | −1850 | | −1650 | mV | |
| | | | $T_A = +85°C$ | −1825 | | −1615 | mV | |
| $I_{IH}$ | HIGH level input current | Other inputs | $T_A = -30°C$ | | | 350 | μA | Apply $V_{IHmax}$ to each input under test, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | | | 220 | μA | |
| | | | $T_A = +85°C$ | | | 220 | μA | |
| | | $\overline{OE}$ input | $T_A = -30°C$ | | | 525 | μA | Apply $V_{IHmax}$ to $\overline{OE}$ input with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | | | 310 | μA | |
| | | | $T_A = +85°C$ | | | 330 | μA | |
| $I_{IL}$ | LOW level input current | | $T_A = -30°C$ | 0.5 | | | μA | Apply $V_{ILmin}$ to each input under test, one at a time, with $V_{IHmax}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | 0.5 | | | μA | |
| | | | $T_A = +85°C$ | 0.3 | | | μA | |
| $-I_{EE}$ | $V_{EE}$ supply current | | $T_A = -30°C$ | | | 80 | mA | |
| | | | $T_A = +25°C$ | | 58 | 73 | mA | |
| | | | $T_A = +85°C$ | | | 80 | mA | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | | $T_A = +25°C$ | | 0.016 | | V/V | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | | 0.250 | | V/V | |
| $\frac{\Delta V_{BB}}{\Delta V_{EE}}$ | Reference bias voltage compensation | | | | 0.148 | | V/V | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst-case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 4.

# Multiplexer

# 10174


$V_{OUT}$
$V_{OHmax}$ (−810mV)
$V_{OHmin}$ (−960mV)
$V_{OHT}$ (−980mV)
GUARANTEED OPERATING AREA
$V_{OLT}$ (−1630mV)
$V_{OLmax}$ (−1650mV)
$V_{OLmin}$ (−1850mV)
TYP
$V_{IN}$
$V_{ILmin}$ (−1850mV)
$V_{IHmax}$ (−810mV)
$V_{ILT}$ (−1475mV)
$V_{IHT}$ (−1105mV)
$V_{BB}$ (−1290mV)
DF05480S

**NOTES:**

| | |
|---|---|
| $V_{IHmax}$ | – Maximum HIGH level input voltage (the most positive $V_{IH}$). |
| $V_{IHT}$ | – HIGH level input threshold voltage. |
| $V_{ILT}$ | – LOW level input threshold voltage. |
| $V_{ILmin}$ | – Minimum LOW level input voltage (the most negative $V_{IL}$). |
| $V_{OHmax}$ | – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition. |
| $V_{OHmin}$ | – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition. |
| $V_{OHT}$ | – HIGH level output threshold voltage with the inputs set to their respective threshold levels. |
| $V_{OLT}$ | – LOW level output threshold voltage with the inputs set to their respective threshold levels. |
| $V_{OLmax}$ | – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions. |
| $V_{OLmin}$ | – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions. |
| $V_{BB}$ | – Reference bias voltage. The internally generated reference voltage which is used to set the input and output threshold level. |

**Figure 4. Transfer Characteristics**

## AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$

| PARAMETER | $T_A = -30°C$ | | $T_A = +25°C$ | | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Typ | Max | Min | Max | | |
| $t_{PLH}$ Propagation delay | 1.4 | 4.8 | 1.5 | 3.5 | 4.5 | 1.4 | 4.8 | ns | Figs. 5, 6, 7 |
| $t_{PHL}$ $D_n$ to $Q_n$ | 1.4 | 4.8 | 1.5 | 3.5 | 4.5 | 1.4 | 4.8 | ns | |
| $t_{PLH}$ Propagation delay | 1.9 | 6.4 | 2.0 | 5.0 | 6.0 | 2.1 | 6.4 | ns | |
| $t_{PHL}$ $S_n$ to $Q_n$ | 1.9 | 6.4 | 2.0 | 5.0 | 6.0 | 2.1 | 6.4 | ns | |
| $t_{PLH}$ Propagation delay | 1.0 | 3.1 | 1.0 | 2.0 | 2.9 | 0.9 | 3.2 | ns | Figs. 5, 6, 7 |
| $t_{PHL}$ $\overline{E}$ to $Q_n$ | 1.0 | 3.1 | 1.0 | 2.0 | 2.9 | 0.9 | 3.2 | ns | |
| $t_{TLH}$ Transition time | 1.0 | 3.4 | 1.1 | 2.0 | 3.3 | 1.1 | 3.6 | ns | Figs. 5, 6, 7 |
| $t_{THL}$ 20% to 80%, 80% to 20% | 1.0 | 3.4 | 1.1 | 2.0 | 3.3 | 1.1 | 3.6 | ns | |

## AC WAVEFORMS

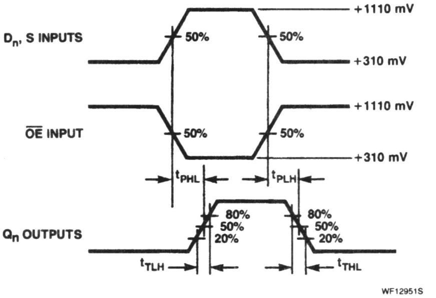
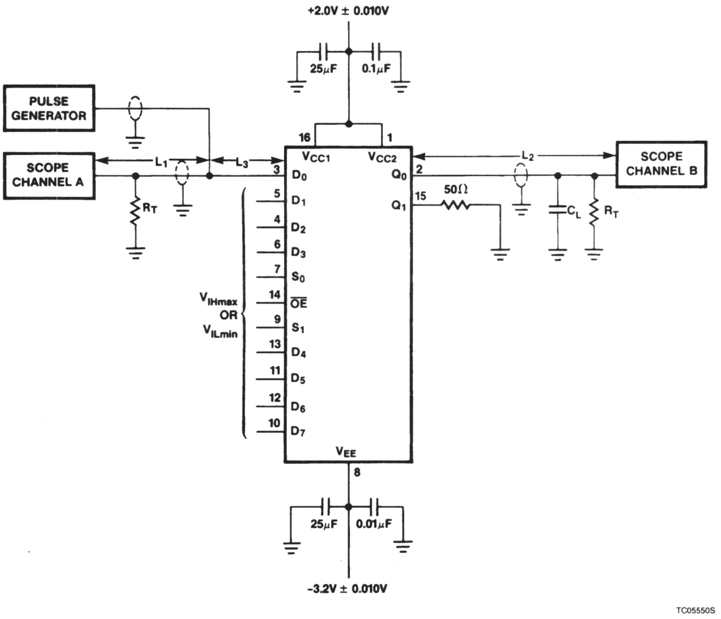

$D_n$, S INPUTS
$\overline{OE}$ INPUT
$Q_n$ OUTPUTS
50%
50%
50%
50%
+1110 mV
+310 mV
+1110 mV
+310 mV
$t_{PHL}$
$t_{PLH}$
80%
50%
20%
80%
50%
20%
$t_{TLH}$
$t_{THL}$
WF12951S

Figure 5. Propagation Delay and Transition Times

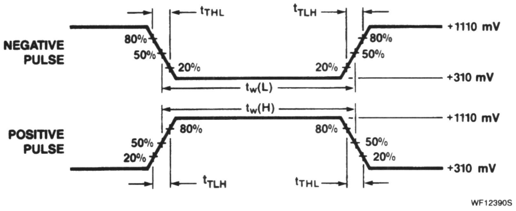
## TEST CIRCUITS AND WAVEFORMS


+2.0V ± 0.010V
25µF
0.1µF
PULSE GENERATOR
SCOPE CHANNEL A
$L_1$
$L_3$
$R_T$
16
1
$V_{CC1}$
$V_{CC2}$
3
$D_0$
$Q_0$
2
$L_2$
SCOPE CHANNEL B
5
$D_1$
$Q_1$
15
50Ω
$C_L$
$R_T$
4
$D_2$
6
$D_3$
7
$S_0$
14
$\overline{OE}$
$V_{IHmax}$
OR
$V_{ILmin}$
9
$S_1$
13
$D_4$
11
$D_5$
12
$D_6$
10
$D_7$
$V_{EE}$
8
25µF
0.01µF
-3.2V ± 0.010V
TC05550S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1µF and 25µF from GND to $V_{CC}$, 0.01µF and 25µF from GND to $V_{EE}$ (0.01 and 0.1µF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than ¼ inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed ¼ inch (6mm).
6. $R_T = 50\Omega$ terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than ¼ inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance $\leqslant 3pF$.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed ¼ inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.

Figure 6. AC Test Circuit


NEGATIVE PULSE
$t_{THL}$
$t_{TLH}$
80%
50%
20%
20%
80%
50%
+1110 mV
+310 mV
$t_w(L)$
$t_w(H)$
POSITIVE PULSE
80%
80%
50%
20%
50%
20%
+1110 mV
+310 mV
$t_{TLH}$
$t_{THL}$
WF12390S

**INPUT PULSE REQUIREMENTS**
**$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$, $V_T = GND$ (0V)**

| Family | Amplitude | Rep Rate | Pulse Width | $t_{TLH}$ | $t_{THL}$ |
|---|---|---|---|---|---|
| 10K ECL | 800mVp-p | 1MHz | 500ns | 2.0 ±0.2ns | 2.0 ±0.2ns |

Figure 7. Input Pulse Definition

# Signetics

# 10175
## Latch

**Quint D-Latch With Common Reset and 2 Wired-OR Common Clock Inputs**
***Product Specification***

**ECL Products**

## DESCRIPTION

The 10175 includes five D-latches with common reset and two wired-OR common clock inputs. When the clock is in the HIGH state, any change of the data input does not affect the output state. When the clock is in the LOW state, any change of the data input is transferred at the output. The outputs are latched on the positive transition of the clock. The reset input is enabled only when the Clock is HIGH. All unused inputs must be tied LOW to $V_{IL}$ or $V_{EE}$.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (−$I_{EE}$) |
|---|---|---|
| 10175 | 2.5ns | 78mA |

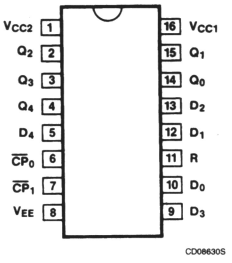
## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} = GND$; $V_{EE} = -5.2V$<br>$T_A = -30°C$ to $+85°C$ |
|---|---|
| Plastic DIP | 10175N |
| Ceramic DIP | 10175F |

## PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_0 - D_4$ | Data Input |
| $\overline{CP}_0$, $\overline{CP}_1$ | Clock Inputs |
| R | Reset Input |
| $Q_0 - Q_4$ | Data Outputs |

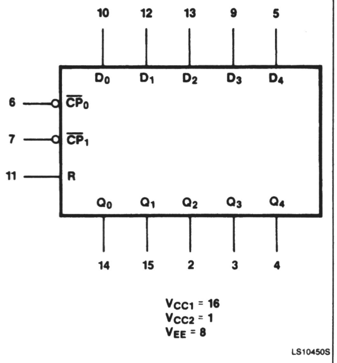
## PIN CONFIGURATION



VCC2 1
Q2 2
Q3 3
Q4 4
D4 5
CP0 6
CP1 7
VEE 8
16 VCC1
15 Q1
14 Q0
13 D2
12 D1
11 R
10 D0
9 D3
CD08630S

Figure 1

## LOGIC SYMBOL



10
12
13
9
5
D0
D1
D2
D3
D4
6
CP0
7
CP1
11
R
Q0
Q1
Q2
Q3
Q4
14
15
2
3
4
VCC1 = 16
VCC2 = 1
VEE = 8
LS10450S

Figure 2

# Latch 10175

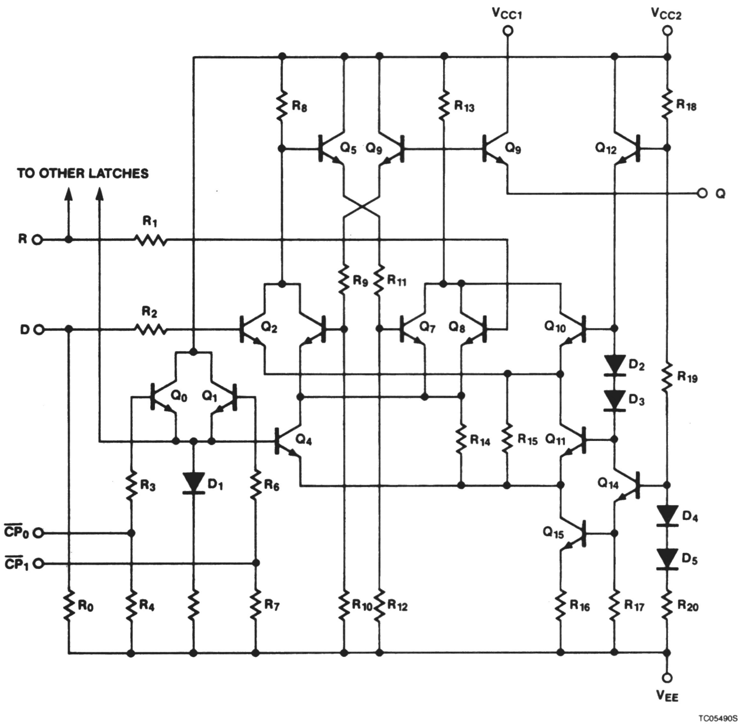

VCC1
VCC2
R8
R13
R18
Q5
Q9
Q9
Q12
TO OTHER LATCHES
Q
R
R1
R9
R11
D
R2
Q2
Q7
Q8
Q10
D2
R19
D3
Q0
Q1
Q4
R14
R15
Q11
R3
D1
R6
Q14
D4
CP̄0
Q15
CP̄1
D5
R0
R4
R7
R10
R12
R16
R17
R20
VEE
TC05490S

Figure 3. Circuit Diagram (One Latch)

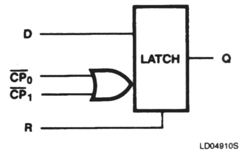

D
CP̄0
CP̄1
LATCH
Q
R
LD04910S

Figure 4. Logic Diagram

## FUNCTION TABLE

| $\overline{CP}_0$ | $\overline{CP}_1$ | R | D | $Q_{n+1}$ |
|---|---|---|---|---|
| L | L | X | L | L |
| L | L | X | H | H |
| H | X | L | X | $Q_n$ |
| X | H | L | X | $Q_n$ |
| H | X | H | X | L |
| X | H | H | X | L |

Positive Logic:
H = HIGH state (the more positive voltage) = 1
L = LOW state (the less positive voltage) = 0
X = Don't Care

## Latch

## 10175

**ABSOLUTE MAXIMUM RATINGS** (Operation beyond the limits set forth in this table may impair useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | | 10K ECL | UNIT |
|---|---|---|---|---|
| $V_{EE}$ | Supply voltage | | -8.0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | | 0 to $V_{EE}$ | V |
| $I_O$ | Output source current | | -50 | mA |
| $T_S$ | Storage temperature | | -55 to +150 | °C |
| $T_J$ | Maximum junction temperature | Ceramic package | +165 | °C |
| | | Plastic package | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | 10K ECL | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | -5.2 | | V |
| $V_{IH}$ | HIGH level input voltage | $T_A = -30°C$ | | | -890 | mV |
| | | $T_A = +25°C$ | | | -810 | mV |
| | | $T_A = +85°C$ | | | -700 | mV |
| $V_{IHT}$ | HIGH level input threshold voltage | $T_A = -30°C$ | -1205 | | | mV |
| | | $T_A = +25°C$ | -1105 | | | mV |
| | | $T_A = +85°C$ | -1035 | | | mV |
| $V_{ILT}$ | LOW level input threshold voltage | $T_A = -30°C$ | | | -1500 | mV |
| | | $T_A = +25°C$ | | | -1475 | mV |
| | | $T_A = +85°C$ | | | -1440 | mV |
| $V_{IL}$ | LOW level input voltage | $T_A = -30°C$ | -1890 | | | mV |
| | | $T_A = +25°C$ | -1850 | | | mV |
| | | $T_A = +85°C$ | -1825 | | | mV |
| $T_A$ | Operating ambient temperature | | -30 | +25 | +85 | °C |

**NOTE:**
When operating at $V_{EE}$ other than specified voltage (-5.2V), the DC and AC Characteristics will vary slightly from specified values.
(See table of DC Characteristics)

# Latch

# 10175

**DC ELECTRICAL CHARACTERISTICS** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$, output loading with 50Ω to $-2.0V \pm 0.010V$ unless otherwise specified[1,3]

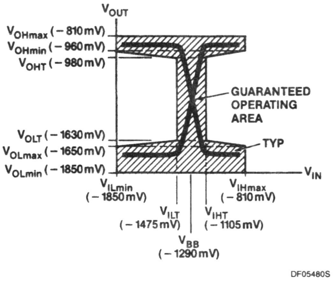
| PARAMETER | | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | | $T_A = -30°C$ | −1060 | | −890 | mV | Apply $V_{IHmax}$ to each $D_n$ input, with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | −960 | | −810 | mV | |
| | | | $T_A = +85°C$ | −890 | | −700 | mV | |
| $V_{OHT}$ | HIGH level output threshold voltage | | $T_A = -30°C$ | −1080 | | | mV | Apply $V_{IHT}$ to each $D_n$ input, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | −980 | | | mV | |
| | | | $T_A = +85°C$ | −910 | | | mV | |
| $V_{OLT}$ | LOW level output threshold voltage | | $T_A = -30°C$ | | | −1655 | mV | Apply $V_{ILT}$ to each input, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | | | −1630 | mV | |
| | | | $T_A = +85°C$ | | | −1595 | mV | |
| $V_{OL}$ | LOW level output voltage | | $T_A = -30°C$ | −1890 | | −1675 | mV | Apply $V_{ILmin}$ to all inputs. |
| | | | $T_A = +25°C$ | −1850 | | −1650 | mV | |
| | | | $T_A = +85°C$ | −1825 | | −1615 | mV | |
| $I_{IH}$ | HIGH level input current | Other inputs | $T_A = -30°C$ | | | 480 | μA | Apply $V_{IHmax}$ to each input under test, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | | | 290 | μA | |
| | | | $T_A = +85°C$ | | | 290 | μA | |
| | | R input | $T_A = -30°C$ | | | 1000 | μA | Apply $V_{IHmax}$ to R input with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | | | 650 | μA | |
| | | | $T_A = +85°C$ | | | 650 | μA | |
| $I_{IL}$ | LOW level input current | | $T_A = -30°C$ | 0.5 | | | μA | Apply $V_{ILmin}$ to each input under test, one at a time, with $V_{IHmax}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | 0.5 | | | μA | |
| | | | $T_A = +85°C$ | 0.3 | | | μA | |
| $-I_{EE}$ | $V_{EE}$ supply current | | $T_A = -30°C$ | | | 107 | mA | |
| | | | $T_A = +25°C$ | | 78 | 97 | mA | |
| | | | $T_A = +85°C$ | | | 107 | mA | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | | $T_A = +25°C$ | | 0.016 | | V/V | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | | 0.250 | | V/V | |
| $\frac{\Delta V_{BB}}{\Delta V_{EE}}$ | Reference bias voltage compensation | | | | 0.148 | | V/V | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst-case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 5.

# Latch

# 10175



**NOTES:**

| | |
|---|---|
| $V_{IHmax}$ | – Maximum HIGH level input voltage (the most positive $V_{IH}$). |
| $V_{IHT}$ | – HIGH level input threshold voltage. |
| $V_{ILT}$ | – LOW level input threshold voltage. |
| $V_{ILmin}$ | – Minimum LOW level input voltage (the most negative $V_{IL}$). |
| $V_{OHmax}$ | – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition. |
| $V_{OHmin}$ | – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition. |
| $V_{OHT}$ | – HIGH level output threshold voltage with the inputs set to their respective threshold levels. |
| $V_{OLT}$ | – LOW level output threshold voltage with the inputs set to their respective threshold levels. |
| $V_{OLmax}$ | – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions. |
| $V_{OLmin}$ | – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions. |
| $V_{BB}$ | – Reference bias voltage (the internally generated reference voltage which is used to set the input and output threshold level). |

**Figure 5. Transfer Characteristics**

## AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$

| PARAMETER | | $T_A = -30°C$ | | $T_A = +25°C$ | | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Typ | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 1.0 | 3.6 | 1.0 | 2.5 | 3.5 | 1.0 | 3.6 | ns | Figs. 6, 8, 9 |
| $t_{PHL}$ | $D_n$ to $Q_n$ | 1.0 | 3.6 | 1.0 | 2.5 | 3.5 | 1.0 | 3.6 | ns | |
| $t_{PLH}$ | Propagation delay | 1.0 | 4.7 | 1.0 | | 4.3 | 1.0 | 4.4 | ns | Figs. 6, 8, 9 |
| $t_{PHL}$ | $\overline{CP}_n$ to $Q_n$ | 1.0 | 4.7 | 1.0 | | 4.3 | 1.0 | 4.4 | ns | |
| $t_{PLH}$ | Propagation delay | 1.0 | 4.0 | 1.0 | | 3.9 | 1.0 | 4.2 | ns | |
| $t_{PHL}$ | R to $Q_n$ | 1.0 | 4.0 | 1.0 | | 3.9 | 1.0 | 4.2 | ns | |
| $t_s$ | Setup time $D_n$ to $\overline{CP}_n$ | 2.5 | | 2.5 | | | 2.5 | | ns | Figs. 7, 8, 9 |
| $t_h$ | Hold time $D_n$ to $\overline{CP}_n$ | 1.5 | | 1.5 | | | 1.5 | | ns | |
| $t_{TLH}$ | Transition time | 1.0 | 3.6 | 1.1 | | 3.5 | 1.1 | 3.7 | ns | Figs. 6, 8, 9 |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 1.0 | 3.6 | 1.1 | | 3.5 | 1.1 | 3.7 | ns | |

## AC WAVEFORMS

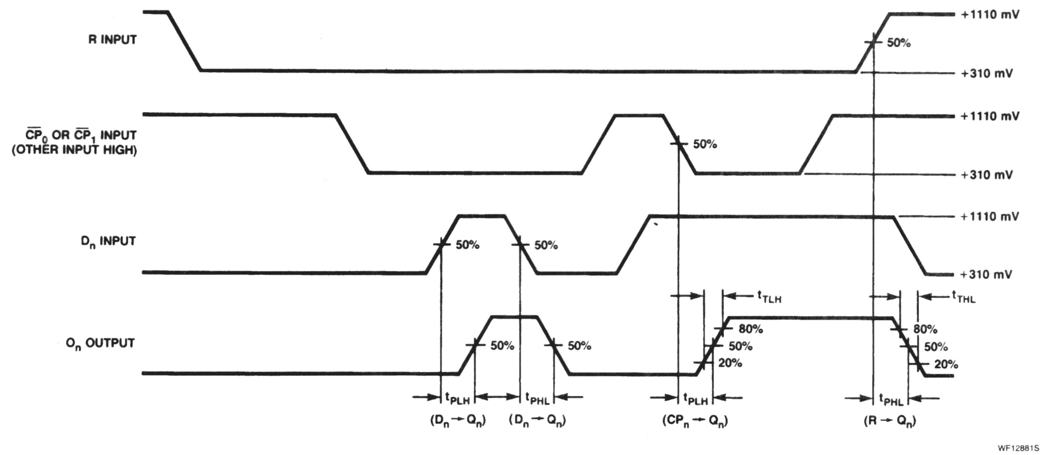

R INPUT
$\overline{CP}_0$ OR $\overline{CP}_1$ INPUT (OTHER INPUT HIGH)
$D_n$ INPUT
$O_n$ OUTPUT
+1110 mV
+310 mV
50%
80%
20%
$t_{PLH}$
$t_{PHL}$
$t_{TLH}$
$t_{THL}$
($D_n \rightarrow Q_n$)
($CP_n \rightarrow Q_n$)
($R \rightarrow Q_n$)
WF12881S

Figure 6. Propagation Delay and Transition Times

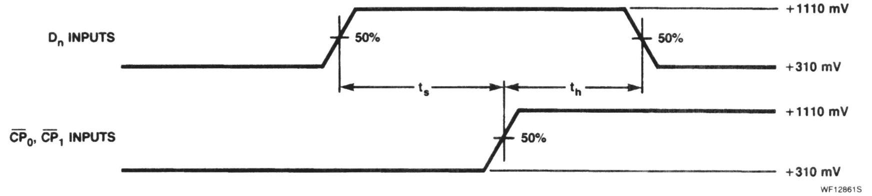
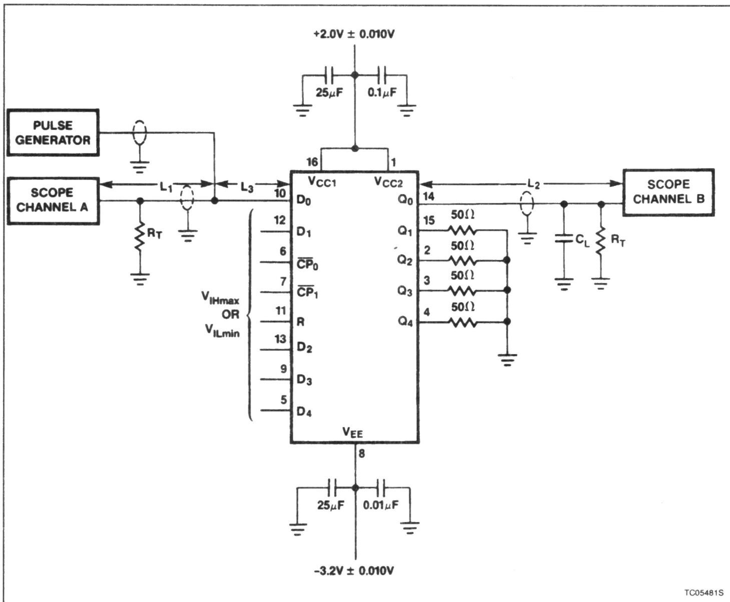

$D_n$ INPUTS
$\overline{CP}_0$, $\overline{CP}_1$ INPUTS
+1110 mV
+310 mV
50%
$t_s$
$t_h$
WF12861S

Figure 7. Setup and Hold Times for Data to Clock

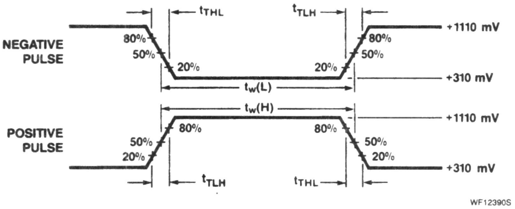
## TEST CIRCUITS AND WAVEFORMS


+2.0V ± 0.010V
25µF
0.1µF
PULSE GENERATOR
SCOPE CHANNEL A
L1
L3
RT
16
1
VCC1
VCC2
10
D0
Q0
14
12
D1
Q1
15
50Ω
6
CP0
Q2
2
7
CP1
Q3
3
11
R
Q4
4
13
D2
9
D3
5
D4
VIHmax OR VILmin
VEE
8
L2
SCOPE CHANNEL B
CL
RT
25µF
0.01µF
-3.2V ± 0.010V
TC05481S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1µF and 25µF from GND to $V_{CC}$, 0.01µF and 25µF from GND to $V_{EE}$. (0.01 and 0.1µF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance $\leqslant$ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.

Figure 8. AC Test Circuit


tTHL
tTLH
NEGATIVE PULSE
80%
50%
20%
20%
80%
50%
+1110 mV
+310 mV
tw(L)
tw(H)
+1110 mV
POSITIVE PULSE
80%
80%
50%
20%
50%
20%
+310 mV
tTLH
tTHL
WF12390S

**INPUT PULSE REQUIREMENTS**
$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$, $V_T$ = GND (0V)

| Family | Amplitude | Rep Rate | Pulse Width | $t_{TLH}$ | $t_{THL}$ |
|---|---|---|---|---|---|
| 10K ECL | 800mVp-p | 1MHz | 500ns | 2.0 ± 0.2ns | 2.0 ± 0.2ns |

Figure 9. Input Pulse Definition

**Signetics**

**ECL Products**

# 10176
## Flip-Flop

**Hex D-Type Master-Slave Flip-Flop**
***Product Specification***

## DESCRIPTION

The 10176 includes six high-speed master-slave D-type flip-flops with one common input Clock for all six. Data enters into the master during the LOW state of the Clock and is transferred to the slave during the positive-going Clock transition. Due to the master-slave structure of the device, a change in the information present at the data ($D_n$) input will not modify the output information at any other time. All unused inputs must be tied LOW to $V_{IL}$ or $V_{EE}$.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 10176 | 150MHz | 88mA |

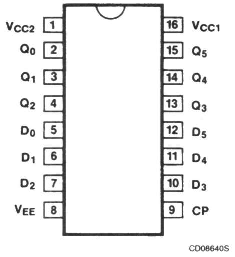
## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} = GND$; $V_{EE} = -5.2V$<br>$T_A = -30°C$ to $+85°C$ |
|---|---|
| Plastic DIP | 10176N |
| Ceramic DIP | 10176F |

## PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_0 - D_5$ | Data Input |
| CP | Clock Input |
| $Q_0 - Q_5$ | Data Outputs |

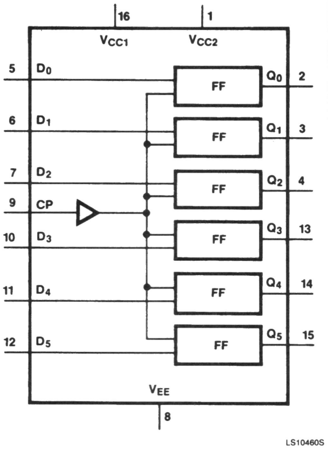
## PIN CONFIGURATION



$V_{CC2}$ 1
$Q_0$ 2
$Q_1$ 3
$Q_2$ 4
$D_0$ 5
$D_1$ 6
$D_2$ 7
$V_{EE}$ 8
16 $V_{CC1}$
15 $Q_5$
14 $Q_4$
13 $Q_3$
12 $D_5$
11 $D_4$
10 $D_3$
9 CP
CD08640S

Figure 1

## LOGIC SYMBOL

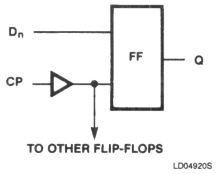


16
1
$V_{CC1}$
$V_{CC2}$
5 $D_0$
6 $D_1$
7 $D_2$
9 CP
10 $D_3$
11 $D_4$
12 $D_5$
FF
$Q_0$ 2
$Q_1$ 3
$Q_2$ 4
$Q_3$ 13
$Q_4$ 14
$Q_5$ 15
$V_{EE}$
8
LS10460S

Figure 2

# Flip-Flop

# 10176



**NOTE:**
C at LOW state; data enters into the master. A clock H means a clock transition from a LOW to a HIGH state; data transfer to the slave output.

Figure 3. Logic Diagram

## FUNCTION TABLE

| CP | $D_n$ | $Q_{n+1}$ |
|---|---|---|
| L | X | $Q_n$ |
| H | L | L |
| H | H | H |

Positive Logic:
H = HIGH state (the more positive voltage) = 1
L = LOW state (the less positive voltage) = 0
X = Don't Care

## ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | | 10K ECL | UNIT |
|---|---|---|---|---|
| $V_{EE}$ | Supply voltage | | −8.0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | | 0 to $V_{EE}$ | V |
| $I_O$ | Output source current | | −50 | mA |
| $T_S$ | Storage temperature | | −55 to +150 | °C |
| $T_J$ | Maximum junction temperature | Ceramic package | +165 | °C |
| | | Plastic package | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | 10K ECL | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | −5.2 | | V |
| $V_{IH}$ | HIGH level input voltage | $T_A = -30°C$ | | | −890 | mV |
| | | $T_A = +25°C$ | | | −810 | mV |
| | | $T_A = +85°C$ | | | −700 | mV |
| $V_{IHT}$ | HIGH level input threshold voltage | $T_A = -30°C$ | −1205 | | | mV |
| | | $T_A = +25°C$ | −1105 | | | mV |
| | | $T_A = +85°C$ | −1035 | | | mV |
| $V_{ILT}$ | LOW level input threshold voltage | $T_A = -30°C$ | | | −1500 | mV |
| | | $T_A = +25°C$ | | | −1475 | mV |
| | | $T_A = +85°C$ | | | −1440 | mV |
| $V_{IL}$ | LOW level input voltage | $T_A = -30°C$ | −1890 | | | mV |
| | | $T_A = +25°C$ | −1850 | | | mV |
| | | $T_A = +85°C$ | −1825 | | | mV |
| $T_A$ | Operating ambient temperature | | −30 | +25 | +85 | °C |

**NOTE:**
When operating at $V_{EE}$ other than specified voltage (−5.2V), the DC and AC Characteristics will vary slightly from specified values. (See table of DC Characteristics)

## Flip-Flop

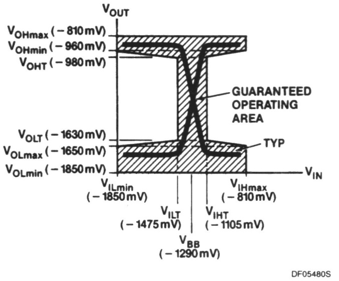
## 10176

**DC ELECTRICAL CHARACTERISTICS** $V_{CC1} = V_{CC2} =$ GND, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$, output loading with 50Ω to $-2.0V \pm 0.010V$ unless otherwise specified[1,3]

| PARAMETER | | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | | $T_A = -30°C$ | -1060 | | -890 | mV | Apply $V_{ILmin}$ to CP input with $V_{IHmax}$ applied to all other inputs. Raise CP from $V_{ILmin}$ to $V_{IHmax}$ and measure $V_{OH}$. |
| | | | $T_A = +25°C$ | -960 | | -810 | mV | |
| | | | $T_A = +85°C$ | -890 | | -700 | mV | |
| $V_{OHT}$ | HIGH level output threshold voltage | | $T_A = -30°C$ | -1080 | | | mV | Apply $V_{ILmin}$ to CP input with $V_{IHmax}$ applied to all other inputs. Raise CP from $V_{ILmin}$ to $V_{IHT}$ and measure $V_{OHT}$. |
| | | | $T_A = +25°C$ | -980 | | | mV | |
| | | | $T_A = +85°C$ | -910 | | | mV | |
| $V_{OLT}$ | LOW level output threshold voltage | | $T_A = -30°C$ | | | -1655 | mV | Apply $V_{ILmin}$ to all inputs. Raise CP input from $V_{ILmin}$ to $V_{IHT}$ and measure $V_{OLT}$. |
| | | | $T_A = +25°C$ | | | -1630 | mV | |
| | | | $T_A = +85°C$ | | | -1595 | mV | |
| $V_{OL}$ | LOW level output voltage | | $T_A = -30°C$ | -1890 | | -1675 | mV | Apply $V_{ILmin}$ to all inputs. Raise CP input from $V_{ILmin}$ to $V_{IHmax}$. Measure $V_{OL}$. |
| | | | $T_A = +25°C$ | -1850 | | -1650 | mV | |
| | | | $T_A = +85°C$ | -1825 | | -1615 | mV | |
| $I_{IH}$ | HIGH level input current | Other inputs | $T_A = -30°C$ | | | 350 | μA | Apply $V_{IHmax}$ to each $D_n$ input under test, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | | | 220 | μA | |
| | | | $T_A = +85°C$ | | | 220 | μA | |
| | | CP input | $T_A = -30°C$ | | | 495 | μA | Apply $V_{IHmax}$ to C input with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | | | 310 | μA | |
| | | | $T_A = +85°C$ | | | 310 | μA | |
| $I_{IL}$ | LOW level input current | | $T_A = -30°C$ | 0.5 | | | μA | Apply $V_{ILmin}$ to each input under test, one at a time, with $V_{IHmax}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | 0.5 | | | μA | |
| | | | $T_A = +85°C$ | 0.3 | | | μA | |
| $-I_{EE}$ | $V_{EE}$ supply current | | $T_A = -30°C$ | | | 121 | mA | |
| | | | $T_A = +25°C$ | | 88 | 110 | mA | |
| | | | $T_A = +85°C$ | | | 121 | mA | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | | $T_A = +25°C$ | | 0.016 | | V/V | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | | 0.250 | | V/V | |
| $\frac{\Delta V_{BB}}{\Delta V_{EE}}$ | Reference bias voltage compensation | | | | 0.148 | | V/V | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst-case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 4.


$V_{OUT}$
$V_{OHmax}$ (−810mV)
$V_{OHmin}$ (−960mV)
$V_{OHT}$ (−980mV)
GUARANTEED OPERATING AREA
TYP
$V_{OLT}$ (−1630mV)
$V_{OLmax}$ (−1650mV)
$V_{OLmin}$ (−1850mV)
$V_{IN}$
$V_{ILmin}$ (−1850mV)
$V_{IHmax}$ (−810mV)
$V_{ILT}$ (−1475mV)
$V_{IHT}$ (−1105mV)
$V_{BB}$ (−1290mV)
DF05480S

**NOTES:**

$V_{IHmax}$ – Maximum HIGH level input voltage (the most positive $V_{IH}$).
$V_{IHT}$ – HIGH level input threshold voltage.
$V_{ILT}$ – LOW level input threshold voltage.
$V_{ILmin}$ – Minimum LOW level input voltage (the most negative $V_{IL}$).
$V_{OHmax}$ – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition.
$V_{OHmin}$ – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition.
$V_{OHT}$ – HIGH level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLT}$ – LOW level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLmax}$ – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions.
$V_{OLmin}$ – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions.
$V_{BB}$ – Reference bias voltage (the internally generated reference voltage which is used to set the input and output threshold level).

**Figure 4. Transfer Characteristics**

## AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$

| PARAMETER | $T_A = -30°C$ | | $T_A = +25°C$ | | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | **Min** | **Max** | **Min** | **Typ** | **Max** | **Min** | **Max** | | |
| $f_{MAX}$ Maximum clock frequency | 125 | | 125 | 150 | | 125 | | MHz | |
| $t_{PLH}$ Propagation delay<br>$t_{PHL}$ CP to $Q_n$ | 1.6<br>1.6 | 4.6<br>4.6 | 1.6<br>1.6 | | 4.5<br>4.5 | 1.6<br>1.6 | 5.0<br>5.0 | ns<br>ns | Figs. 5, 7, 8 |
| $t_s$ Setup time $D_n$ to CP | 2.5 | | 2.5 | | | 2.5 | | ns | Figs. 6, 7, 8 |
| $t_h$ Hold time $D_n$ to CP | 1.5 | | 1.5 | | | 1.5 | | ns | |
| $t_{TLH}$ Transition time<br>$t_{THL}$ 20% to 80%, 80% to 20% | 1.0<br>1.0 | 4.1<br>4.1 | 1.1<br>1.1 | | 4.0<br>4.0 | 1.1<br>1.1 | 4.4<br>4.4 | ns<br>ns | Figs. 5, 7, 8 |

## AC WAVEFORMS

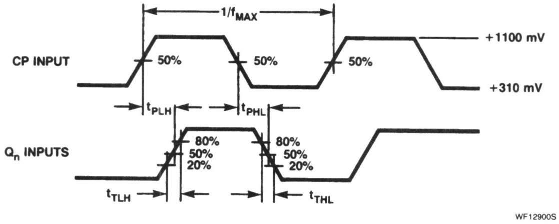

$1/f_{MAX}$
CP INPUT
50%
50%
50%
+1100 mV
+310 mV
$t_{PLH}$
$t_{PHL}$
$Q_n$ INPUTS
80%
50%
20%
80%
50%
20%
$t_{TLH}$
$t_{THL}$
WF12900S

**Figure 5. Propagation Delay and Transition Times for CP to $Q_n$**

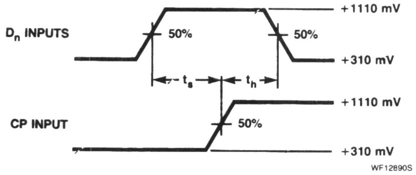
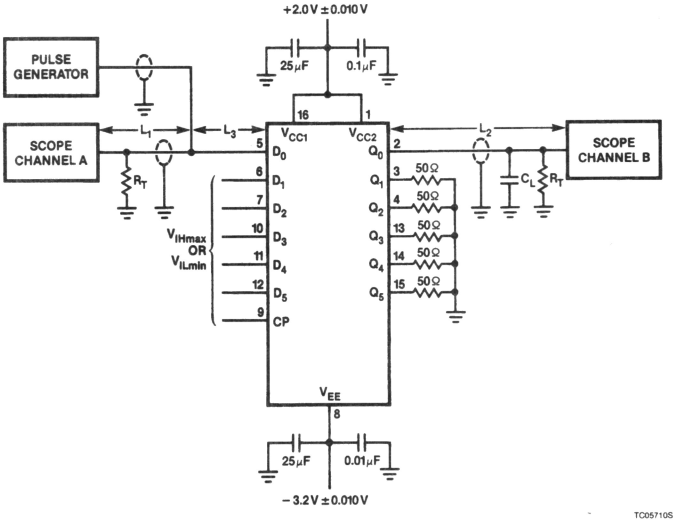

$D_n$ INPUTS
50%
50%
+1110 mV
+310 mV
$t_s$
$t_h$
CP INPUT
50%
+1110 mV
+310 mV
WF12890S

**Figure 6. Setup and Hold Times for $D_n$ to CP**

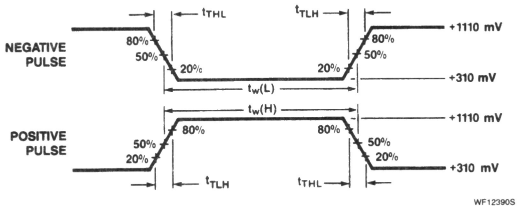
## TEST CIRCUITS AND WAVEFORMS


+2.0V ±0.010V
PULSE GENERATOR
SCOPE CHANNEL A
SCOPE CHANNEL B
25μF
0.1μF
L1
L3
L2
RT
CL
16
1
5
6
7
10
11
12
9
2
3
4
13
14
15
8
VCC1
VCC2
D0
D1
D2
D3
D4
D5
CP
Q0
Q1
Q2
Q3
Q4
Q5
50Ω
VIHmax OR VILmin
VEE
25μF
0.01μF
−3.2V ±0.010V
TC05710S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1μF and 25μF from GND to $V_{CC}$, 0.01μF and 25μF from GND to $V_{EE}$. (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T = 50\Omega$ terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance $\leq$ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.

Figure 7. AC Test Circuit


NEGATIVE PULSE
POSITIVE PULSE
tTHL
tTLH
80%
50%
20%
tw(L)
tw(H)
+1110 mV
+310 mV
WF12390S

| INPUT PULSE REQUIREMENTS<br>$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$, $V_T$ = GND (0V) | | | | | |
|---|---|---|---|---|---|
| Family | Amplitude | Rep Rate | Pulse Width | $t_{TLH}$ | $t_{THL}$ |
| 10K ECL | 800mVp-p | 1MHz | 500ns | 2.0 ±0.2ns | 2.0 ±0.2ns |

Figure 8. Input Pulse Definition

Signetics

# 10179
# Look-Ahead Carry Block

**Look-Ahead Carry Block**
***Product Specification***

**ECL Products**

## DESCRIPTION

The 10179 is a Look-Ahead Carry Block. It can be used in conjunction with the 10181 4-bit arithmetic/logic unit to perform a high order look-ahead carry, in applications requiring high-speed arithmetic operation on long words. All unused inputs can be left open due to integrated pull-down resistors, which avoid the need for a supply voltage.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT $(-I_{EE})$ |
|---|---|---|
| 10179 | 2.3ns | 58mA |

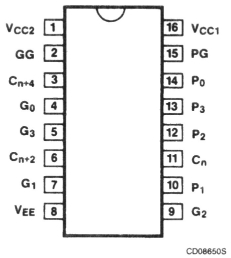
## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} = GND$; $V_{EE} = -5.2V$<br>$T_A = -30°C$ to $+85°C$ |
|---|---|
| Plastic DIP | 10179N |
| Ceramic DIP | 10179F |

## PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $C_n$ | Carry Input |
| $P_0 - P_3$ | Carry Propagate Input |
| $G_0 - G_3$ | Carry Generate Inputs |
| $C_{n+2}$, $C_{n+4}$ | Carry Outputs |
| PG | Carry Propagate Output |
| GG | Carry Generate Output |

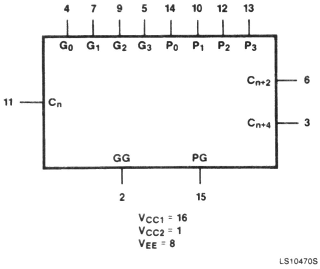
## PIN CONFIGURATION



$V_{CC2}$ 1
GG 2
$C_{n+4}$ 3
$G_0$ 4
$G_3$ 5
$C_{n+2}$ 6
$G_1$ 7
$V_{EE}$ 8
9 $G_2$
10 $P_1$
11 $C_n$
12 $P_2$
13 $P_3$
14 $P_0$
15 PG
16 $V_{CC1}$
CD08650S

Figure 1

## LOGIC SYMBOL



4 7 9 5 14 10 12 13
$G_0$ $G_1$ $G_2$ $G_3$ $P_0$ $P_1$ $P_2$ $P_3$
11 $C_n$
$C_{n+2}$ 6
$C_{n+4}$ 3
GG 2
PG 15
$V_{CC1}$ = 16
$V_{CC2}$ = 1
$V_{EE}$ = 8
LS10470S

Figure 2

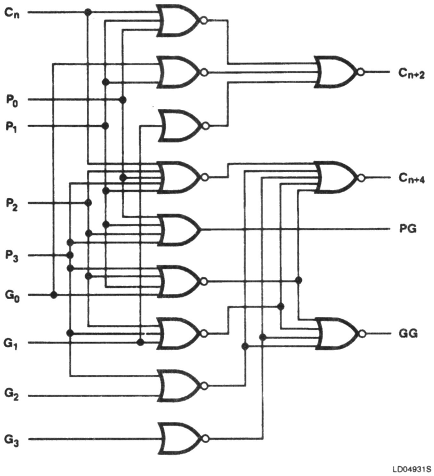


**Figure 3. Logic Diagram**

## LOGIC FUNCTION

$P_G = P_1 + P_2 + {}_3 + P_4,\ P_n = P_{n-1}$

$G_G = G_4\ (G_3 + P_4)\ (G_2 + P_3 + P_4)\ (G_1 + P_2 + P_3 + P_4),\ G_n = G_{n-1},\ P_n = P_{n-1}$

$C_{n+2} = G_2\ (G_1 + P_2)\ (C_n + P_1 + P_2),\ G_n = G_{n-1},\ P_n = P_{n-1}$

$C_{n+4} = G_4\ (G_3 + P_4)\ (G_2 + G_3 + P_4)\ (G_1 + P_2 + P_3 + P_4)\ (C_n + P_1 + P_2 + P_3 + P_4),\ G_n = G_{n-1},\ P_n = P_{n-1}$

In Positive Logic: H = HIGH state (the more positive voltage) = 1
L = LOW state (the less positive voltage) = 0

The overall carry function is invariant with the polarity (positive or negative) of the logic if the P and G inputs are interchanged.

# Look-Ahead Carry Block

# 10179

**ABSOLUTE MAXIMUM RATINGS** (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | | 10K ECL | UNIT |
|---|---|---|---|---|
| $V_{EE}$ | Supply voltage | | -8.0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | | 0 to $V_{EE}$ | V |
| $I_O$ | Output source current | | -50 | mA |
| $T_S$ | Storage temperature | | -55 to +150 | °C |
| $T_J$ | Maximum junction temperature | Ceramic package | +165 | °C |
| | | Plastic package | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | 10K ECL | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | -5.2 | | V |
| $V_{IH}$ | HIGH level input voltage | $T_A = -30°C$ | | | -890 | mV |
| | | $T_A = +25°C$ | | | -810 | mV |
| | | $T_A = +85°C$ | | | -700 | mV |
| $V_{IHT}$ | HIGH level input threshold voltage | $T_A = -30°C$ | -1205 | | | mV |
| | | $T_A = +25°C$ | -1105 | | | mV |
| | | $T_A = +85°C$ | -1035 | | | mV |
| $V_{ILT}$ | LOW level input threshold voltage | $T_A = -30°C$ | | | -1500 | mV |
| | | $T_A = +25°C$ | | | -1475 | mV |
| | | $T_A = +85°C$ | | | -1440 | mV |
| $V_{IL}$ | LOW level input voltage | $T_A = -30°C$ | -1890 | | | mV |
| | | $T_A = +25°C$ | -1850 | | | mV |
| | | $T_A = +85°C$ | -1825 | | | mV |
| $T_A$ | Operating ambient temperature | | -30 | +25 | +85 | °C |

**NOTE:**
When operating at $V_{EE}$ other than specified voltage (-5.2V), the DC and AC Characteristics will vary slightly from specified values.
(See table of DC Characteristics)

# Look-Ahead Carry Block

# 10179

## DC ELECTRICAL CHARACTERISTICS

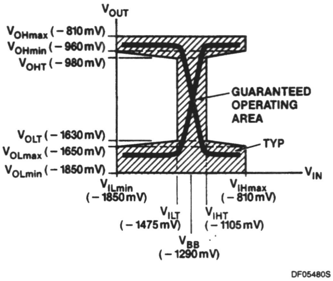
$V_{CC1} = V_{CC2}$ = GND, $V_{EE}$ = −5.2V ±0.010V, $T_A$ = −30°C to +85°C, output loading with 50Ω to −2.0V ±0.010V unless otherwise specified[1,3]

| PARAMETER | | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | | $T_A$ = −30°C | −1060 | | −890 | mV | For GG output, apply $V_{IHmax}$ to all $G_n$ inputs with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A$ = +25°C | −960 | | −810 | mV | |
| | | | $T_A$ = +85°C | −890 | | −700 | mV | |
| $V_{OHT}$ | HIGH level output threshold voltage | | $T_A$ = −30°C | −1080 | | | mV | For GG output, apply $V_{IHT}$ to each $G_n$ input, one at a time, $V_{IHmax}$ applied to all other $G_n$ inputs. |
| | | | $T_A$ = +25°C | −980 | | | mV | |
| | | | $T_A$ = +85°C | −910 | | | mV | |
| $V_{OLT}$ | LOW level ouput threshold voltage | | $T_A$ = −30°C | | | −1655 | mV | For GG output, apply $V_{ILT}$ to $G_3$ input with $V_{IHmax}$ applied to all other inputs. |
| | | | $T_A$ = +25°C | | | −1630 | mV | |
| | | | $T_A$ = +85°C | | | −1595 | mV | |
| $V_{OL}$ | LOW level output voltage | | $T_A$ = −30°C | −1890 | | −1675 | mV | For GG output, apply $V_{ILmin}$ to all $G_n$ inputs with $V_{IHmax}$ applied to all other inputs. |
| | | | $T_A$ = +25°C | −1850 | | −1650 | mV | |
| | | | $T_A$ = +85°C | −1825 | | −1615 | mV | |
| $I_{IH}$ | HIGH level input current | $G_0$, $G_1$, $C_n$ inputs | $T_A$ = −30°C | | | 430 | μA | Apply $V_{IHmax}$ to each input under test, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A$ = +25°C | | | 270 | μA | |
| | | | $T_A$ = +85°C | | | 270 | μA | |
| | | $G_2$, $G_3$ inputs | $T_A$ = −30°C | | | 360 | μA | |
| | | | $T_A$ = +25°C | | | 225 | μA | |
| | | | $T_A$ = +85°C | | | 225 | μA | |
| | | $P_0$ input | $T_A$ = −30°C | | | 565 | μA | Apply $V_{IHmax}$ to $P_0$ input with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A$ = +25°C | | | 355 | μA | |
| | | | $T_A$ = +85°C | | | 355 | μA | |
| | | $P_1$, $P_3$ inputs | $T_A$ = −30°C | | | 700 | μA | Apply $V_{IHmax}$ to each input under test, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A$ = +25°C | | | 440 | μA | |
| | | | $T_A$ = +85°C | | | 440 | μA | |
| | | $P_2$ input | $T_A$ = −30°C | | | 630 | μA | Apply $V_{IHmax}$ to $P_3$ input with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A$ = +25°C | | | 395 | μA | |
| | | | $T_A$ = +85°C | | | 395 | μA | |
| $I_{IL}$ | LOW level input current | | $T_A$ = −30°C | 0.5 | | | μA | Apply $V_{ILmin}$ to each input, one at a time, with $V_{IHmax}$ applied to all other inputs. |
| | | | $T_A$ = +25°C | 0.5 | | | μA | |
| | | | $T_A$ = +85°C | 0.3 | | | μA | |
| $-I_{EE}$ | $V_{EE}$ supply current | | $T_A$ = −30°C | | | 79 | mA | |
| | | | $T_A$ = +25°C | | 58 | 72 | mA | |
| | | | $T_A$ = +85°C | | | 79 | mA | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | | $T_A$ = +25°C | | 0.016 | | V/V | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | | 0.250 | | V/V | |
| $\frac{\Delta V_{BB}}{\Delta V_{EE}}$ | Reference bias voltage compensation | | | | 0.148 | | V/V | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst-case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 4.

# Look-Ahead Carry Block 10179


$V_{OUT}$
$V_{OHmax}$ (−810mV)
$V_{OHmin}$ (−960mV)
$V_{OHT}$ (−980mV)
GUARANTEED OPERATING AREA
$V_{OLT}$ (−1630mV)
$V_{OLmax}$ (−1650mV)
$V_{OLmin}$ (−1850mV)
TYP
$V_{IN}$
$V_{ILmin}$ (−1850mV)
$V_{IHmax}$ (−810mV)
$V_{ILT}$ (−1475mV)
$V_{IHT}$ (−1105mV)
$V_{BB}$ (−1290mV)
DF05480S

**NOTES:**

| | |
|---|---|
| $V_{IHmax}$ | – Maximum HIGH level input voltage (the most positive $V_{IH}$). |
| $V_{IHT}$ | – HIGH level input threshold voltage. |
| $V_{ILT}$ | – LOW level input threshold voltage. |
| $V_{ILmin}$ | – Minimum LOW level input voltage (the most negative $V_{IL}$). |
| $V_{OHmax}$ | – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition. |
| $V_{OHmin}$ | – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition. |
| $V_{OHT}$ | – HIGH level output threshold voltage with the inputs set to their respective threshold levels. |
| $V_{OLT}$ | – LOW level output threshold voltage with the inputs set to their respective threshold levels. |
| $V_{OLmax}$ | – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions. |
| $V_{OLmin}$ | – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions. |
| $V_{BB}$ | – Reference bias voltage. The internally generated reference voltage which is used to set the input and output threshold level. |

**Figure 4. Transfer Characteristics**

## AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$

| PARAMETER | $T_A = -30°C$ | | $T_A = +25°C$ | | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Typ | Max | Min | Max | | |
| $t_{PLH}$ Propagation delay<br>$t_{PHL}$ $P_n$ to PG | 1.0<br>1.0 | 3.7<br>3.7 | 1.0<br>1.0 | 2.3<br>1.8 | 3.5<br>3.5 | 1.0<br>1.0 | 3.9<br>3.9 | ns<br>ns | Figs. 5, 6, 7 |
| $t_{PLH}$ Propagation delay<br>$t_{PHL}$ $C_n$ to $C_{n+2}$ | 1.0<br>1.0 | 5.8<br>5.8 | 1.0<br>1.0 | 3.0<br>3.0 | 4.5<br>4.5 | 1.0<br>1.0 | 6.1<br>6.1 | ns<br>ns | |
| $t_{PLH}$ Propagation delay<br>$t_{PHL}$ $G_n$ to GG | 1.0<br>1.0 | 5.8<br>5.8 | 1.0<br>1.0 | 3.2<br>3.2 | 5.5<br>5.5 | 1.0<br>1.0 | 6.1<br>6.1 | ns<br>ns | |
| $t_{TLH}$ Transition time<br>$t_{THL}$ 20% to 80%, 80% to 20% | 1.3<br>1.3 | 3.5<br>3.5 | 1.3<br>1.3 | 2.5<br>2.5 | 3.5<br>3.5 | 1.3<br>1.3 | 3.5<br>3.5 | ns<br>ns | |

## AC WAVEFORMS

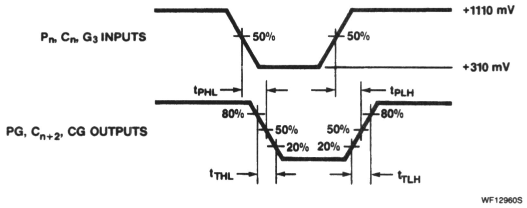
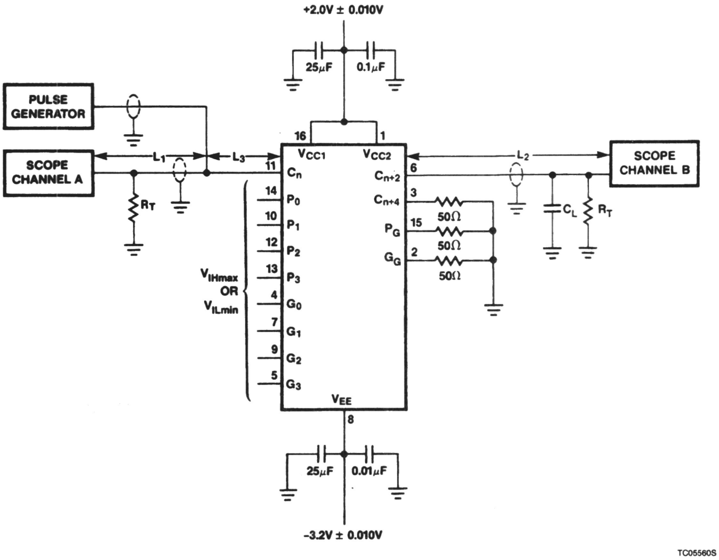

$P_n$, $C_n$, $G_3$ INPUTS
50%
50%
+1110 mV
+310 mV
$t_{PHL}$
$t_{PLH}$
PG, $C_{n+2}$, CG OUTPUTS
80%
80%
50%
50%
20%
20%
$t_{THL}$
$t_{TLH}$
WF12960S

**Figure 5. Propagation Delay and Transition Times**

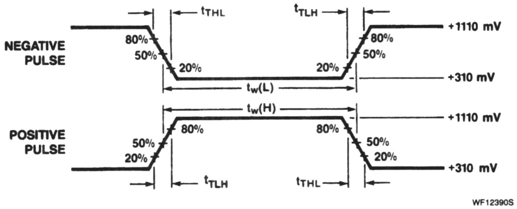
## TEST CIRCUITS AND WAVEFORMS


+2.0V ± 0.010V
25µF
0.1µF
PULSE GENERATOR
SCOPE CHANNEL A
L1
L3
RT
16
1
11
VCC1
VCC2
Cn
Cn+2
6
14
P0
Cn+4
3
10
P1
PG
15
12
P2
GG
2
13
P3
4
G0
7
G1
9
G2
5
G3
VIHmax OR VILmin
VEE
8
50Ω
50Ω
50Ω
L2
SCOPE CHANNEL B
CL
RT
25µF
0.01µF
-3.2V ± 0.010V
TC05560S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1µF and 25µF from GND to $V_{CC}$, 0.01µF and 25µF from GND to $V_{EE}$ (0.01 and 0.1µF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than ¼ inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed ¼ inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than ¼ inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance ≤ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed ¼ inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.

Figure 6. AC Test Circuit


NEGATIVE PULSE
POSITIVE PULSE
tTHL
tTLH
80%
50%
20%
tw(L)
tw(H)
+1110 mV
+310 mV
+1110 mV
+310 mV
WF12390S

| INPUT PULSE REQUIREMENTS<br>$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$, $V_T$ = GND (0V) | | | | | |
|---|---|---|---|---|---|
| Family | Amplitude | Rep Rate | Pulse Width | $t_{TLH}$ | $t_{THL}$ |
| 10K ECL | 800mVp-p | 1MHz | 500ns | 2.0 ±0.2ns | 2.0 ±0.2ns |

Figure 7. Input Pulse Definition

Signetics

# 10180
## Adder/Subtractor

**Dual 2-Bit Adder/Subtractor**
***Product Specification***

**ECL Products**

## DESCRIPTION

The 10180 is a high-speed, low power, general purpose adder/subtractor. Inputs for each adder are: Carry-in ($C_{0in}$, $C_{1in}$), Operand A ($A_0$, $A_1$), Operand B ($B_0$, $B_1$). Outputs are Sum ($F_0$, $F_1$), $\overline{\text{Sum}}$ ($\overline{F}_0$, $\overline{F}_1$) and Carry-out ($C_{0out}$, $C_{1out}$). Common select inputs act as control lines to invert A or B for subtraction. A very high-speed operation is possible with Operand in the Sum or Carryout propagation delay of 4.5ns, and Carry-in to Carry-out propagation delay of 2.2ns. The 10180 is designed to be used in special purpose adder/subtractor or in high-speed multiplier arrays.

All unused inputs can be left open due to integrated pull-down resistors which avoid the need for a supply voltage.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 10180 | $A_n$, $B_n$ to $C_{out}$ 4.5ns | 70mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC}$ = GND; $V_{EE}$ = −5.2V<br>$T_A$ = −30°C to +85°C |
|---|---|
| Plastic DIP | 10180N |
| Ceramic DIP | 10180F |

## PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $A_0$, $A_1$ | A Operand Inputs |
| $B_0$, $B_1$ | B Operand Inputs |
| $S_0$, $S_1$ | Select Inputs |
| $C_{0in}$, $C_{1in}$ | Carry-in Inputs |
| $C_{0out}$, $C_{1out}$ | Carry-out Outputs |
| $F_0$, $\overline{F}_0$, $F_1$, $\overline{F}_1$ | Sum Outputs |

## PIN CONFIGURATION

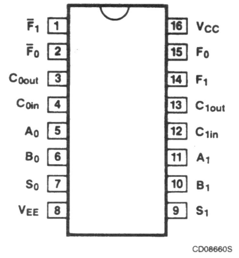

F̄1 1
F̄0 2
C0out 3
C0in 4
A0 5
B0 6
S0 7
VEE 8
16 VCC
15 F0
14 F1
13 C1out
12 C1in
11 A1
10 B1
9 S1
CD08660S

Figure 1

## LOGIC SYMBOL

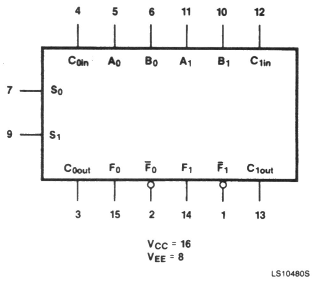

4
5
6
11
10
12
C0in
A0
B0
A1
B1
C1in
7
S0
9
S1
C0out
F0
F̄0
F1
F̄1
C1out
3
15
2
14
1
13
VCC = 16
VEE = 8
LS10480S

Figure 2

## Adder/Subtractor 10180

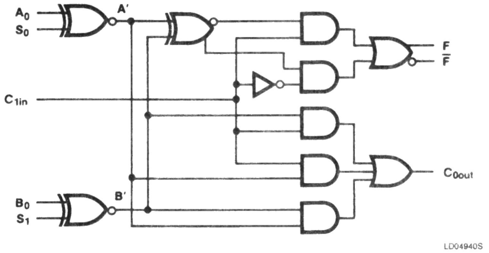


**Figure 3. Logic Function (One Adder/Subtractor)**

### FUNCTION SELECT TABLE

| $S_0$ | $S_1$ | FUNCTIONS F |
|---|---|---|
| H | H | $A + B + C_{in}$ |
| H | L | $C_{in} + A - B$ |
| L | H | $C_{in} + B - A$ |
| L | L | $C_{in} - A - B$ |

Positive Logic:
H = HIGH state = 1
L = LOW state = 0
Positive logic only:
$A' = \overline{A \oplus S_0} = A \odot S_0$
$B' = \overline{B \oplus S_1} = B \odot S_1$
Both positive and negative logic:
$F = \overline{C}_{in}\ (\overline{A}'B' + A'\overline{B}') + C_{in}\ (A'B' + \overline{A}'\overline{B}')$
$C_{out} = C_{in}A' + C_{in}B' + A'B'$

### FUNCTION TABLE

| FUNCTION | INPUTS | | | | | OUTPUTS | | |
|---|---|---|---|---|---|---|---|---|
| | $S_0$ | $S_1$ | A | B | $C_{in}$ | F | $\overline{F}$ | $C_{out}$ |
| ADD<br>$(A + B + C_1)$ | H | H | L | L | L | L | H | L |
| | H | H | L | L | H | H | L | L |
| | H | H | L | H | L | H | L | L |
| | H | H | L | H | H | L | H | H |
| | H | H | H | L | L | H | L | L |
| | H | H | H | L | H | L | H | H |
| | H | H | H | H | L | L | H | H |
| | H | H | H | H | H | H | L | H |
| SUBTRACT<br>$(C_1 + A - B)$ | H | L | L | L | L | H | L | L |
| | H | L | L | L | H | L | H | H |
| | H | L | L | H | L | L | H | L |
| | H | L | L | H | H | H | L | L |
| | H | L | H | L | L | L | H | H |
| | H | L | H | L | H | H | L | H |
| | H | L | H | H | L | H | L | L |
| | H | L | H | H | H | L | H | H |
| Reverse<br>SUBTRACT<br>$(C_1 + B - A)$ | L | H | L | L | L | H | L | L |
| | L | H | L | L | H | L | H | H |
| | L | H | L | H | L | L | H | H |
| | L | H | L | H | H | H | L | H |
| | L | H | H | L | L | L | H | L |
| | L | H | H | L | H | H | L | L |
| | L | H | H | H | L | H | L | L |
| | L | H | H | H | H | L | H | H |
| $(C_1 - A - B)$ | L | L | L | L | L | L | H | H |
| | L | L | L | L | H | H | L | H |
| | L | L | L | H | L | H | L | L |
| | L | L | L | H | H | L | H | H |
| | L | L | H | L | L | H | L | L |
| | L | L | H | L | H | L | H | H |
| | L | L | H | H | L | L | H | L |
| | L | L | H | H | H | H | L | L |

6

# Adder/Subtractor 10180

## ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | | 10K ECL | UNIT |
|---|---|---|---|---|
| $V_{EE}$ | Supply voltage | | –8.0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | | 0 to $V_{EE}$ | V |
| $I_O$ | Output source current | | –50 | mA |
| $T_S$ | Storage temperature | | –55 to +150 | °C |
| $T_J$ | Maximum junction temperature | Ceramic package | +165 | °C |
| | | Plastic package | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | 10K ECL | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | |
| $V_{CC}$ | Circuit ground | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | –5.2 | | V |
| $V_{IH}$ | HIGH level input voltage | $T_A$ = –30°C | | | –890 | mV |
| | | $T_A$ = +25°C | | | –810 | mV |
| | | $T_A$ = +85°C | | | –700 | mV |
| $V_{IHT}$ | HIGH level input threshold voltage | $T_A$ = –30°C | –1205 | | | mV |
| | | $T_A$ = +25°C | –1105 | | | mV |
| | | $T_A$ = +85°C | –1035 | | | mV |
| $V_{ILT}$ | LOW level input threshold voltage | $T_A$ = –30°C | | | –1500 | mV |
| | | $T_A$ = +25°C | | | –1475 | mV |
| | | $T_A$ = +85°C | | | –1440 | mV |
| $V_{IL}$ | LOW level input voltage | $T_A$ = –30°C | –1890 | | | mV |
| | | $T_A$ = +25°C | –1850 | | | mV |
| | | $T_A$ = +85°C | –1825 | | | mV |
| $T_A$ | Operating ambient temperature | | –30 | +25 | +85 | °C |

**NOTE:**
When operating at $V_{EE}$ other than specified voltage (–5.2V), the DC and AC Characteristics will vary slightly from specified values.
(See table of DC Characteristics)

# Adder/Subtractor 10180

## DC ELECTRICAL CHARACTERISTICS

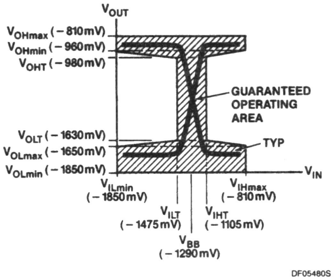
$V_{CC}$ = GND, $V_{EE}$ = −5.2V ±0.010V, $T_A$ = −30°C to +85°C, output loading with 50Ω to −2.0V ±0.010V unless otherwise specified[1,3]

| PARAMETER | | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | | $T_A$ = −30°C | −1060 | | −890 | mV | Using $V_{IHmax}$ and $V_{ILmin}$, apply a functional pattern as indicated in the FUNCTION TABLE and measure $V_{OH}$ on the respective outputs. |
| | | | $T_A$ = +25°C | −960 | | −810 | mV | |
| | | | $T_A$ = +85°C | −890 | | −700 | mV | |
| $V_{OHT}$ | HIGH level output threshold voltage | | $T_A$ = −30°C | −1080 | | | mV | Apply $V_{IHT}$ or $V_{ILT}$ to one input at a time while applying $V_{IHmax}$ or $V_{ILmin}$ to all other inputs in accordance with the FUNCTION TABLE and measure $V_{OHT}$ on the respective outputs. |
| | | | $T_A$ = +25°C | −980 | | | mV | |
| | | | $T_A$ = +85°C | −910 | | | mV | |
| $V_{OLT}$ | LOW level output threshold voltage | | $T_A$ = −30°C | | | −1655 | mV | Apply $V_{ILT}$ or $V_{IHT}$ to one input at a time while applying $V_{IHmax}$ or $V_{ILmin}$ to all other inputs in accordance with the FUNCTION TABLE and measure $V_{OLT}$ on the respective outputs. |
| | | | $T_A$ = +25°C | | | −1630 | mV | |
| | | | $T_A$ = +85°C | | | −1595 | mV | |
| $V_{OL}$ | LOW level output voltage | | $T_A$ = −30°C | −1890 | | −1675 | mV | Using $V_{IHmax}$ and $V_{ILmin}$, apply a functional pattern as indicated in the FUNCTION TABLE and measure $V_{OL}$ on the respective outputs. |
| | | | $T_A$ = +25°C | −1850 | | −1650 | mV | |
| | | | $T_A$ = +85°C | −1825 | | −1615 | mV | |
| $I_{IH}$ | HIGH level input current | $C_{0in}$ $C_{1in}$ outputs | $T_A$ = −30°C | | | 590 | μA | Apply $V_{IHmax}$ to each input under test, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A$ = +25°C | | | 370 | μA | |
| | | | $T_A$ = +85°C | | | 370 | μA | |
| | | $A_0$, $A_1$, $B_0$, $B_1$ inputs | $T_A$ = −30°C | | | 350 | μA | |
| | | | $T_A$ = +25°C | | | 220 | μA | |
| | | | $T_A$ = +85°C | | | 220 | μA | |
| | | $S_0$, $S_1$ inputs | $T_A$ = −30°C | | | 460 | μA | |
| | | | $T_A$ = +25°C | | | 290 | μA | |
| | | | $T_A$ = +85°C | | | 290 | μA | |
| $I_{IL}$ | LOW level input current | | $T_A$ = −30°C | 0.5 | | | μA | Apply $V_{ILmin}$ to each input under test, one at a time, with $V_{IHmax}$ applied to all other inputs. |
| | | | $T_A$ = +25°C | 0.5 | | | μA | |
| | | | $T_A$ = +85°C | 0.3 | | | μA | |
| $-I_{EE}$ | $V_{EE}$ supply current | | $T_A$ = −30°C | | | 95 | mA | |
| | | | $T_A$ = +25°C | | 70 | 86 | mA | |
| | | | $T_A$ = +85°C | | | 95 | mA | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | | $T_A$ = +25°C | | 0.016 | | V/V | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | | 0.250 | | V/V | |
| $\frac{\Delta V_{BB}}{\Delta V_{EE}}$ | Reference bias voltage compensation | | | | 0.148 | | V/V | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst-case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 4.

# Adder/Subtractor 10180



**NOTES:**

$V_{IHmax}$ – Maximum HIGH level input voltage (the most positive $V_{IH}$).
$V_{IHT}$ – HIGH level input threshold voltage.
$V_{ILT}$ – LOW level input threshold voltage.
$V_{ILmin}$ – Minimum LOW level input voltage (the most negative $V_{IL}$).
$V_{OHmax}$ – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition.
$V_{OHmin}$ – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition.
$V_{OHT}$ – HIGH level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLT}$ – LOW level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLmax}$ – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions.
$V_{OLmin}$ – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions.
$V_{BB}$ – Reference bias voltage (the internally generated reference voltage which is used to set the input and output threshold level).

**Figure 4. Transfer Characteristics**

## AC ELECTRICAL CHARACTERISTICS $V_{CC} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$

| PARAMETER | | $T_A = -30°C$ | | $T_A = +25°C$ | | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Typ | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 1.3 | 5.8 | 1.3 | 4.5 | 5.4 | 1.1 | 5.8 | ns | Figs. 5, 6, 7 |
| $t_{PHL}$ | $A_0$, $A_1$, $B_0$, $B_1$, to $F_0$, $F_1$ | 1.3 | 5.8 | 1.3 | 4.5 | 5.4 | 1.1 | 5.8 | ns | |
| $t_{PLH}$ | Propagation delay | 1.0 | 3.4 | 1.0 | 2.2 | 3.3 | 0.9 | 3.6 | ns | |
| $t_{PHL}$ | $C_{0in}$ to $C_{0out}$ | 1.0 | 3.4 | 1.0 | 2.2 | 3.3 | 0.9 | 3.6 | ns | |
| $t_{PLH}$ | Propagation delay | 1.3 | 5.8 | 1.3 | 4.5 | 5.4 | 1.1 | 5.8 | ns | |
| $t_{PHL}$ | $S_0$, $S_1$ to $\overline{F}_0$, $\overline{F}_1$ | 1.3 | 5.8 | 1.3 | 4.5 | 5.4 | 1.1 | 5.8 | ns | |
| $t_{TLH}$ | Transition time | 1.0 | 3.8 | 1.1 | 2.4 | 3.7 | 1.1 | 3.9 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 1.0 | 3.8 | 1.1 | 2.4 | 3.7 | 1.1 | 3.9 | ns | |

## AC WAVEFORMS

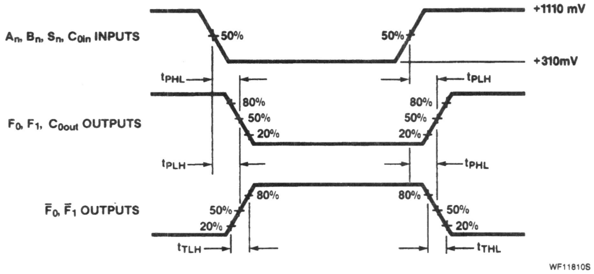
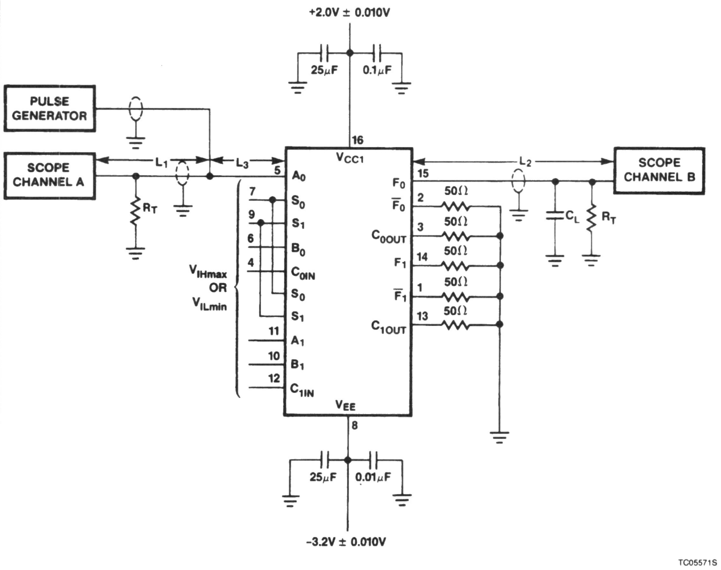


**Figure 5. Propagation Delay and Transition Times for Operands, Selects, and Carry-in Inputs to Carry-out and Sum Outputs**

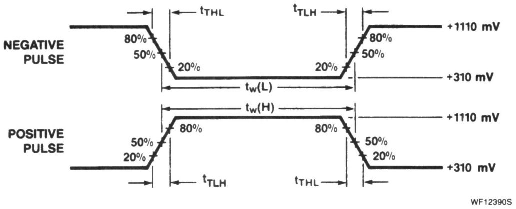
## TEST CIRCUITS AND WAVEFORMS


+2.0V ± 0.010V
25μF
0.1μF
PULSE GENERATOR
SCOPE CHANNEL A
$L_1$
$L_3$
$R_T$
16
$V_{CC1}$
5
$A_0$
7
$S_0$
9
$S_1$
6
$B_0$
4
$C_{0IN}$
$S_0$
$S_1$
11
$A_1$
10
$B_1$
12
$C_{1IN}$
$V_{IHmax}$ OR $V_{ILmin}$
$V_{EE}$
8
$F_0$
15
$\overline{F}_0$
2
$C_{0OUT}$
3
$F_1$
14
$\overline{F}_1$
1
$C_{1OUT}$
13
50Ω
50Ω
50Ω
50Ω
50Ω
$L_2$
$C_L$
$R_T$
SCOPE CHANNEL B
25μF
0.01μF
-3.2V ± 0.010V
TC05571S

**NOTES:**

1. $V_{CC} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1μF and 25μF from GND to $V_{CC}$, 0.01μF and 25μF from GND to $V_{EE}$. (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T = 50\Omega$ terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance $\leqslant 3pF$.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ±1% or better.

Figure 6. AC Test Circuit for 10180


NEGATIVE PULSE
POSITIVE PULSE
$t_{THL}$
$t_{TLH}$
80%
50%
20%
$t_w(L)$
$t_w(H)$
+1110 mV
+310 mV
WF12390S

| INPUT PULSE REQUIREMENTS<br>$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$, $V_T$ = GND (0V) | | | | | |
|---|---|---|---|---|---|
| **Family** | **Amplitude** | **Rep Rate** | **Pulse Width** | **$t_{TLH}$** | **$t_{THL}$** |
| 10K ECL | 800mVp-p | 1MHz | 500ns | 2.0 ±0.2ns | 2.0 ±0.2ns |

Figure 7. Input Pulse Definition

**Signetics**

**ECL Products**

# 10181
# Arithmetic Unit

**4-Bit Arithmetic Logic Unit/Function Generator**
***Product Specification***

## DESCRIPTION

The 10181 is a high-speed, Arithmetic Logic Unit. It performs 16 logic operations and 16 arithmetic operations on two 4-bit words. Arithmetic or logic mode of operation is selected by the mode control (M). Arithmetic logic operations are selected by a 4-bit select input ($S_0 - S_3$) in accordance with the function table. The device provides a group Carry Propagate (PG) and a Carry Generate (GG) for high-speed operations on very long words, using a 10179 as a high order look-ahead carry block. The internal carry is enabled while the mode control input (M) is LOW (arithmetic operation).

All unused inputs can be left open due to integrated pull-down resistors which avoid the need for a supply voltage.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 10181 | 4.2ns | 130mA |

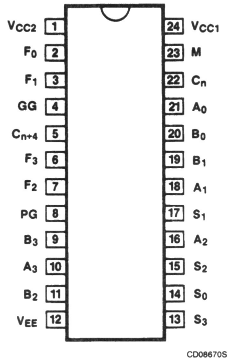
## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} = \text{GND}$; $V_{EE} = -5.2V$<br>$T_A = -30°C$ to $+85°C$ |
|---|---|
| Plastic DIP | 10181N |
| Ceramic DIP | 10181F |

## PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| M | Mode Control Input |
| $A_0 - A_3$, $B_0 - B_3$ | Operand Inputs |
| $S_0 - S_3$ | Function Select Inputs |
| $C_n$ | Carry Inputs |
| $F_0 - F_3$ | Data Outputs |
| $C_{n+4}$ | Carry Output |
| GG | Carry Generate Output |
| PG | Carry Propagate Output |

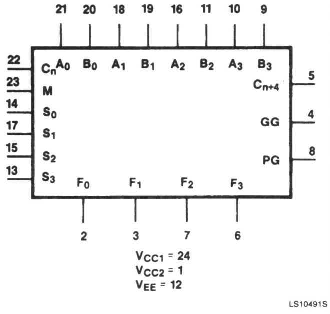
## PIN CONFIGURATION



VCC2 1
F0 2
F1 3
GG 4
Cn+4 5
F3 6
F2 7
PG 8
B3 9
A3 10
B2 11
VEE 12
24 VCC1
23 M
22 Cn
21 A0
20 B0
19 B1
18 A1
17 S1
16 A2
15 S2
14 S0
13 S3
CD08670S

Figure 1

## LOGIC SYMBOL



21 20 18 19 16 11 10 9
Cn A0 B0 A1 B1 A2 B2 A3 B3
22 23 14 17 15 13
M S0 S1 S2 S3
Cn+4 5
GG 4
PG 8
F0 F1 F2 F3
2 3 7 6
VCC1 = 24
VCC2 = 1
VEE = 12
LS10491S

Figure 2

## Arithmetic Unit 10181

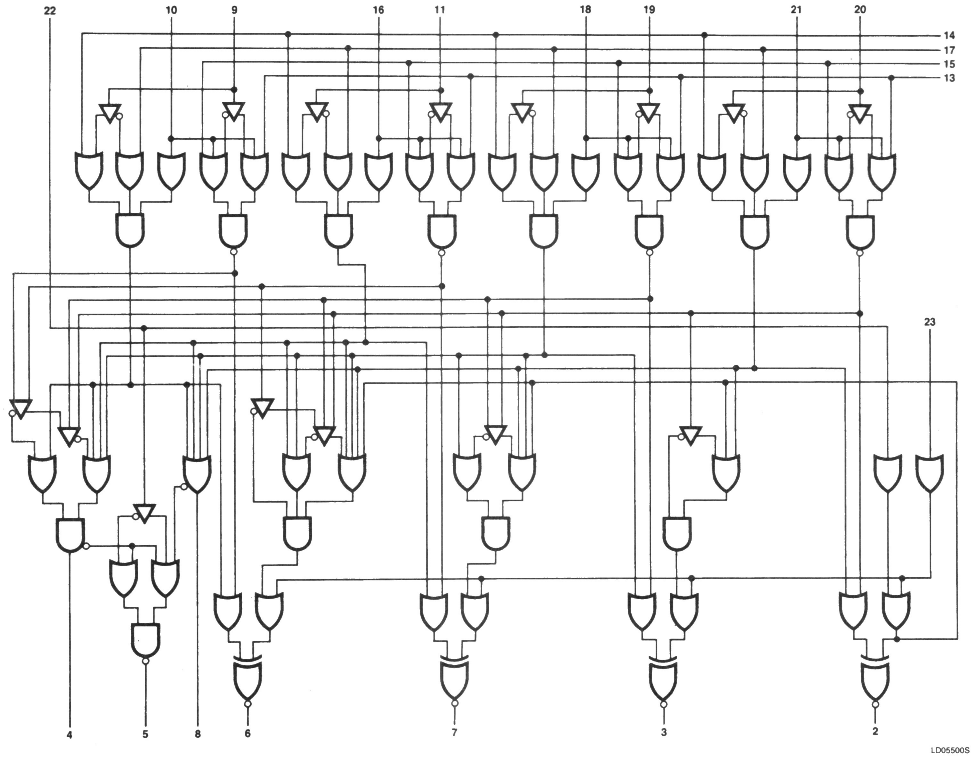


Figure 3. Logic Diagram

## FUNCTION TABLE

| FUNCTION SELECT INPUTS | | | | LOGIC FUNCTION MODE | ARITHMETIC OPERATION MODE |
|---|---|---|---|---|---|
| $S_3$ | $S_2$ | $S_1$ | $S_0$ | F (M = HIGH) | F (M = LOW; $C_n$ = LOW) |
| L | L | L | L | $\overline{A}$ | A |
| L | L | L | H | $\overline{A} + \overline{B}$ | A plus $(A \cdot \overline{B})$ |
| L | L | H | L | $\overline{A} + B$ | A plus $(A \cdot B)$ |
| L | L | H | H | logic "1" | A times 2 |
| L | H | L | L | $\overline{A} \cdot \overline{B}$ | $(A + B)$ plus 0 |
| L | H | L | H | $\overline{B}$ | $(A + B)$ plus $(A \cdot \overline{B})$ |
| L | H | H | L | $AB + \overline{A}\overline{B}$ | A plus B |
| L | H | H | H | $A + \overline{B}$ | A plus $(A + B)$ |
| H | L | L | L | $\overline{A} \cdot B$ | $(A + \overline{B})$ plus 0 |
| H | L | L | H | $A\overline{B} + \overline{A}B$ | A minus B minus 1 |
| H | L | H | L | B | $(A + \overline{B})$ plus $(A \cdot B)$ |
| H | L | H | H | $A + B$ | A plus $(A + \overline{B})$ |
| H | H | L | L | logic "0" | minus 1 (two's complement) |
| H | H | L | H | $A \cdot \overline{B}$ | $(A \cdot \overline{B})$ minus 1 |
| H | H | H | L | AB | $(A \cdot B)$ minus 1 |
| H | H | H | H | A | A minus 1 |

Positive Logic: H = HIGH state = 1
L = LOW state = 0

## Arithmetic Unit 10181

### ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | | 10K ECL | UNIT |
|---|---|---|---|---|
| $V_{EE}$ | Supply voltage | | −8.0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | | 0 to $V_{EE}$ | V |
| $I_O$ | Output source current | | −50 | mA |
| $T_S$ | Storage temperature | | −55 to +150 | °C |
| $T_J$ | Maximum junction temperature | Ceramic package | +165 | °C |
| | | Plastic package | +150 | °C |

### DC OPERATING CONDITIONS

| PARAMETER | | | 10K ECL Min | 10K ECL Nom | 10K ECL Max | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | −5.2 | | V |
| $V_{IH}$ | HIGH level input voltage | $T_A$ = −30°C | | | −890 | mV |
| | | $T_A$ = +25°C | | | −810 | mV |
| | | $T_A$ = +85°C | | | −700 | mV |
| $V_{IHT}$ | HIGH level input threshold voltage | $T_A$ = −30°C | −1205 | | | mV |
| | | $T_A$ = +25°C | −1105 | | | mV |
| | | $T_A$ = +85°C | −1035 | | | mV |
| $V_{ILT}$ | LOW level input threshold voltage | $T_A$ = −30°C | | | −1500 | mV |
| | | $T_A$ = +25°C | | | −1475 | mV |
| | | $T_A$ = +85°C | | | −1440 | mV |
| $V_{IL}$ | LOW level input voltage | $T_A$ = −30°C | −1890 | | | mV |
| | | $T_A$ = +25°C | −1850 | | | mV |
| | | $T_A$ = +85°C | −1825 | | | mV |
| $T_A$ | Operating ambient temperature | | −30 | +25 | +85 | °C |

**NOTE:**
When operating at $V_{EE}$ other than specified voltage (−5.2V), the DC and AC Characteristics will vary slightly from specified values.
(See table of DC Characteristics)

## Arithmetic Unit

## 10181

**DC ELECTRICAL CHARACTERISTICS** $V_{CC1} = V_{CC2} =$ GND, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$, output loading with 50Ω to $-2.0V \pm 0.010V$ unless otherwise specified[1,3]

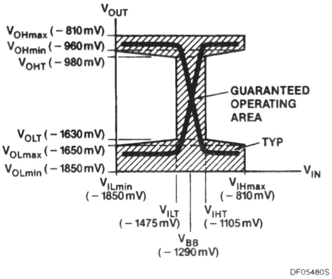
| PARAMETER | | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | | $T_A = -30°C$ | −1060 | | −890 | mV | All input/output combinations in accordance with the functional table. Input conditions: $V_{ILmin}$, $V_{IHmax}$ (for $V_{OH}$ and $V_{OL}$) or $V_{ILT}$, $V_{IHT}$ (for $V_{OHT}$ and $V_{OLT}$).<br>Only 1 input at a time should be at $V_{IHT}$ or $V_{ILT}$. All other inputs should be at $V_{IHmax}$ or $V_{ILmin}$ during test. |
| | | | $T_A = +25°C$ | −960 | | −810 | mV | |
| | | | $T_A = +85°C$ | −890 | | −700 | mV | |
| $V_{OHT}$ | HIGH level output threshold voltage | | $T_A = -30°C$ | −1080 | | | mV | |
| | | | $T_A = +25°C$ | −980 | | | mV | |
| | | | $T_A = +85°C$ | −910 | | | mV | |
| $V_{OLT}$ | LOW level output threshold voltage | | $T_A = -30°C$ | | | −1655 | mV | |
| | | | $T_A = +25°C$ | | | −1630 | mV | |
| | | | $T_A = +85°C$ | | | −1595 | mV | |
| $V_{OL}$ | LOW level output voltage | | $T_A = -30°C$ | −1890 | | −1675 | mV | |
| | | | $T_A = +25°C$ | −1850 | | −1650 | mV | |
| | | | $T_A = +85°C$ | −1825 | | −1615 | mV | |
| $I_{IH}$ | HIGH level input current | $A_n$ inputs | $T_A = -30°C$ | | | 350 | µA | Apply $V_{IHmax}$ to each input under test, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | | | 220 | µA | |
| | | | $T_A = +85°C$ | | | 220 | µA | |
| | | $B_n$ inputs | $T_A = -30°C$ | | | 390 | µA | |
| | | | $T_A = +25°C$ | | | 245 | µA | |
| | | | $T_A = +85°C$ | | | 245 | µA | |
| | | $S_n$ inputs | $T_A = -30°C$ | | | 425 | µA | |
| | | | $T_A = +25°C$ | | | 265 | µA | |
| | | | $T_A = +85°C$ | | | 265 | µA | |
| | | $C_n$ input | $T_A = -30°C$ | | | 460 | µA | Apply $V_{IHmax}$ to $C_n$ input with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | | | 290 | µA | |
| | | | $T_A = +85°C$ | | | 290 | µA | |
| | | M input | $T_A = -30°C$ | | | 320 | µA | Apply $V_{IHmax}$ to M input with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | | | 200 | µA | |
| | | | $T_A = +85°C$ | | | 200 | µA | |
| $I_{IL}$ | LOW level input current | | $T_A = -30°C$ | 0.5 | | | µA | Apply $V_{ILmin}$ to each input under test, one at a time, with $V_{IHmax}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | 0.5 | | | µA | |
| | | | $T_A = +85°C$ | 0.3 | | | µA | |
| $-I_{EE}$ | $V_{EE}$ supply current | | $T_A = -30°C$ | | | 150 | mA | Apply $V_{IHmax}$ to all inputs. |
| | | | $T_A = +25°C$ | | 130 | 145 | mA | |
| | | | $T_A = +85°C$ | | | 150 | mA | |

## DC ELECTRICAL CHARACTERISTICS (Continued)

| PARAMETER | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] |
|---|---|---|---|---|---|---|---|
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | $T_A = +25°C$ | | 0.016 | | V/V | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | 0.250 | | V/V | |
| $\frac{\Delta V_{BB}}{\Delta V_{EE}}$ | Reference bias voltage compensation | | | 0.148 | | V/V | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst-case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 4.



**NOTES:**

$V_{IHmax}$ – Maximum HIGH level input voltage (the most positive $V_{IH}$).
$V_{IHT}$ – HIGH level input threshold voltage.
$V_{ILT}$ – LOW level input threshold voltage.
$V_{ILmin}$ – Minimum LOW level input voltage (the most negative $V_{IL}$).
$V_{OHmax}$ – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition.
$V_{OHmin}$ – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition.
$V_{OHT}$ – HIGH level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLT}$ – LOW level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLmax}$ – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions.
$V_{OLmin}$ – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions.
$V_{BB}$ – Reference bias voltage (the internally generated reference voltage which is used to set the input and output threshold level).

Figure 4. Transfer Characteristics

**AC ELECTRICAL CHARACTERISTICS** $V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$

| PARAMETER | | $T_A = -30°C$ | | $T_A = +25°C$ | | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS[1] |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Typ | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 1.0 | 5.1 | 1.1 | 3.1 | 5.0 | 1.1 | 5.4 | ns | Figs. 5, 6, 7 |
| $t_{PHL}$ | $C_n$ to $C_{n+4}$ | 1.0 | 5.1 | 1.1 | 3.1 | 5.0 | 1.1 | 5.4 | ns | $A_0$, $A_1$, $A_2$, $A_3$ |
| $t_{TLH}$ | Transition time[2] | 1.0 | 3.2 | 1.0 | 2.0 | 3.0 | 1.0 | 3.2 | ns | Figs. 5, 6, 7 |
| $t_{THL}$ | $C_n$ to $C_{n+4}$ | 1.0 | 3.2 | 1.0 | 2.0 | 3.0 | 1.0 | 3.2 | ns | $A_0$, $A_1$, $A_2$, $A_3$ |
| $t_{PLH}$ | Propagation delay | 1.7 | 7.2 | 2.0 | 4.5 | 7.0 | 2.0 | 7.5 | ns | Figs. 5, 6, 7 |
| $t_{PHL}$ | $C_n$ to $F_1$ | 1.7 | 7.2 | 2.0 | 4.5 | 7.0 | 2.0 | 7.5 | ns | $A_0$ |
| $t_{TLH}$ | Transition time[2] | 1.3 | 5.3 | 1.5 | 3.0 | 5.0 | 1.5 | 5.3 | ns | Figs. 5, 6, 7 |
| $t_{THL}$ | $C_n$ to $F_1$ | 1.3 | 5.3 | 1.5 | 3.0 | 5.0 | 1.5 | 5.3 | ns | $A_0$ |
| $t_{PLH}$ | Propagation delay | 2.6 | 10.4 | 3.0 | 6.5 | 10.0 | 3.0 | 10.8 | ns | Figs. 5, 6, 7 |
| $t_{PHL}$ | $A_1$ to $F_1$ | 2.6 | 10.4 | 3.0 | 6.5 | 10.0 | 3.0 | 10.8 | ns | |
| $t_{TLH}$ | Transition time[2] | 1.3 | 5.4 | 1.5 | 3.0 | 5.0 | 1.5 | 5.3 | ns | Figs. 5, 6, 7 |
| $t_{THL}$ | $A_1$ to $F_1$ | 1.3 | 5.4 | 1.5 | 3.0 | 5.0 | 1.5 | 5.3 | ns | |
| $t_{PLH}$ | Propagation delay | 1.6 | 7.0 | 2.0 | 5.0 | 6.5 | 2.0 | 7.0 | ns | Figs. 5, 6, 7 |
| $t_{PHL}$ | $A_1$ to PG | 1.6 | 7.0 | 2.0 | 5.0 | 6.5 | 2.0 | 7.0 | ns | $S_0$, $S_3$ |
| $t_{TLH}$ | Transition time[2] | 0.8 | 3.7 | 1.1 | 2.0 | 3.5 | 1.1 | 3.8 | ns | Figs. 5, 6, 7 |
| $t_{THL}$ | $A_1$ to PG | 0.8 | 3.7 | 1.1 | 2.0 | 3.5 | 1.1 | 3.8 | ns | $S_0$, $S_3$ |
| $t_{PLH}$ | Propagation delay | 1.1 | 7.4 | 2.0 | 4.5 | 7.0 | 1.3 | 7.7 | ns | Figs. 5, 6, 7 |
| $t_{PHL}$ | $A_1$ to GG | 1.1 | 7.4 | 2.0 | 4.5 | 7.0 | 1.3 | 7.7 | ns | $A_0$, $A_2$, $A_3$, $C_n$ |
| $t_{TLH}$ | Transition time[2] | 1.2 | 5.1 | 1.5 | 4.0 | 5.0 | 1.2 | 5.3 | ns | Figs. 5, 6, 7 |
| $t_{THL}$ | $A_1$ to GG | 1.2 | 5.1 | 1.5 | 4.0 | 5.0 | 1.2 | 5.3 | ns | $A_0$, $A_2$, $A_3$, $C_n$ |
| $t_{PLH}$ | Propagation delay | 1.7 | 7.3 | 2.0 | 5.0 | 7.0 | 2.0 | 7.8 | ns | Figs. 5, 6, 7 |
| $t_{PHL}$ | $A_1$ to $C_{n+4}$ | 1.7 | 7.3 | 2.0 | 5.0 | 7.0 | 2.0 | 7.8 | ns | $A_0$, $A_2$, $A_3$, $C_n$ |
| $t_{TLH}$ | Transition time[2] | 1.0 | 3.1 | 1.0 | 2.0 | 3.0 | 1.0 | 3.2 | ns | Figs. 5, 6, 7 |
| $t_{THL}$ | $A_1$ to $C_{n+4}$ | 1.0 | 3.1 | 1.0 | 2.0 | 3.0 | 1.0 | 3.2 | ns | $A_0$, $A_2$, $A_3$, $C_n$ |
| $t_{PLH}$ | Propagation delay | 2.7 | 11.3 | 3.0 | 8.0 | 11.0 | 3.0 | 11.9 | ns | Figs. 5, 6, 7 |
| $t_{PHL}$ | $B_1$ to $F_1$ | 2.7 | 11.3 | 3.0 | 8.0 | 11.0 | 3.0 | 11.9 | ns | $S_3$, $C_n$ |
| $t_{TLH}$ | Transition time[2] | 1.2 | 5.3 | 1.5 | 3.5 | 5.0 | 1.5 | 5.3 | ns | Figs. 5, 6, 7 |
| $t_{THL}$ | $B_1$ to $F_1$ | 1.2 | 5.3 | 1.5 | 3.5 | 5.0 | 1.5 | 5.3 | ns | $S_3$, $C_n$ |
| $t_{PLH}$ | Propagation delay | 1.6 | 7.7 | 2.0 | 6.0 | 7.5 | 2.0 | 8.0 | ns | Figs. 5, 6, 7 |
| $t_{PHL}$ | $B_1$ to PG | 1.6 | 7.7 | 2.0 | 6.0 | 7.5 | 2.0 | 8.0 | ns | $S_0$, $S_3$ |
| $t_{TLH}$ | Transition time[2] | 1.0 | 3.6 | 1.1 | 2.0 | 3.5 | 1.1 | 3.9 | ns | Figs. 5, 6, 7 |
| $t_{THL}$ | $B_1$ to PG | 1.0 | 3.6 | 1.1 | 2.0 | 3.5 | 1.1 | 3.9 | ns | $S_0$, $S_3$ |
| $t_{PLH}$ | Propagation delay | 1.7 | 8.2 | 2.0 | 6.0 | 8.0 | 2.0 | 8.6 | ns | Figs. 5, 6, 7 |
| $t_{PHL}$ | $B_1$ to GG | 1.7 | 8.2 | 2.0 | 6.0 | 8.0 | 2.0 | 8.6 | ns | $S_3$, $C_n$ |
| $t_{TLH}$ | Transition time[2] | 1.4 | 5.2 | 1.5 | 3.0 | 5.0 | 1.2 | 5.4 | ns | Figs. 5, 6, 7 |
| $t_{THL}$ | $B_1$ to GG | 1.4 | 5.2 | 1.5 | 3.0 | 5.0 | 1.2 | 5.4 | ns | $S_3$, $C_n$ |
| $t_{PLH}$ | Propagation delay | 1.8 | 8.2 | 2.0 | 6.0 | 8.0 | 2.0 | 8.7 | ns | Figs. 5, 6, 7 |
| $t_{PHL}$ | $B_1$ to $C_{n+4}$ | 1.8 | 8.2 | 2.0 | 6.0 | 8.0 | 2.0 | 8.7 | ns | $S_3$, $C_n$ |
| $t_{TLH}$ | Transition time[2] | 0.9 | 3.1 | 1.0 | 2.0 | 3.0 | 1.0 | 3.2 | ns | Figs. 5, 6, 7 |
| $t_{THL}$ | $B_1$ to $C_{n+4}$ | 0.9 | 3.1 | 1.0 | 2.0 | 3.0 | 1.0 | 3.2 | ns | $S_3$, $C_n$ |
| $t_{PLH}$ | Propagation delay | 2.4 | 10.3 | 3.0 | 6.5 | 10.0 | 3.0 | 10.8 | ns | Figs. 5, 6, 7 |
| $t_{PHL}$ | M to $F_1$ | 2.4 | 10.3 | 3.0 | 6.5 | 10.0 | 3.0 | 10.8 | ns | |
| $t_{TLH}$ | Transition time[2] | 1.1 | 5.1 | 1.5 | 4.0 | 5.0 | 1.5 | 5.3 | ns | Figs. 5, 6, 7 |
| $t_{THL}$ | M to $F_1$ | 1.1 | 5.1 | 1.5 | 4.0 | 5.0 | 1.5 | 5.3 | ns | |
| $t_{PLH}$ | Propagation delay | 2.5 | 10.7 | 3.0 | 6.5 | 10.0 | 3.0 | 10.8 | ns | Figs. 5, 6, 7 |
| $t_{PHL}$ | $S_1$ to $F_1$ | 2.5 | 10.7 | 3.0 | 6.5 | 10.0 | 3.0 | 10.8 | ns | $A_1$, $B_1$ |
| $t_{TLH}$ | Transition time[2] | 1.0 | 5.4 | 1.5 | 3.0 | 5.0 | 1.5 | 5.4 | ns | Figs. 5, 6, 7 |
| $t_{THL}$ | $S_1$ to $F_1$ | 1.0 | 5.4 | 1.5 | 3.0 | 5.0 | 1.5 | 5.4 | ns | $A_3$, $B_3$ |

# Arithmetic Unit 10181

## AC ELECTRICAL CHARACTERISTICS (Continued)

| PARAMETER | | $T_A = -30°C$ | | $T_A = +25°C$ | | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS[1] |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Typ | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 1.7 | 8.3 | 2.0 | 6.0 | 8.0 | 2.0 | 8.4 | ns | Figs. 5, 6, 7 |
| $t_{PHL}$ | $S_1$ to PG | 1.7 | 8.3 | 2.0 | 6.0 | 8.0 | 2.0 | 8.4 | ns | $A_3$, $B_3$ |
| $t_{TLH}$ | Transition time[2] | 0.8 | 5.1 | 1.1 | 3.0 | 5.0 | 1.1 | 5.2 | ns | Figs. 5, 6, 7 |
| $t_{THL}$ | $S_1$ to PG | 0.8 | 5.1 | 1.1 | 3.0 | 5.0 | 1.1 | 5.2 | ns | $A_3$, $B_3$ |
| $t_{PLH}$ | Propagation delay | 1.6 | 9.3 | 2.0 | 6.0 | 9.0 | 2.0 | 9.9 | ns | Figs. 5, 6, 7 |
| $t_{PHL}$ | $S_1$ to $C_{n+4}$ | 1.6 | 9.3 | 2.0 | 6.0 | 9.0 | 2.0 | 9.9 | ns | $A_3$, $B_3$ |
| $t_{TLH}$ | Transition time[2] | 0.9 | 5.3 | 1.1 | 3.0 | 5.0 | 1.0 | 5.2 | ns | Figs. 5, 6, 7 |
| $t_{THL}$ | $S_1$ to $C_{n+4}$ | 0.9 | 5.3 | 1.1 | 3.0 | 5.0 | 1.0 | 5.2 | ns | $A_3$, $B_3$ |
| $t_{PLH}$ | Propagation delay | 1.5 | 9.6 | 2.0 | 6.0 | 9.0 | 1.9 | 9.7 | ns | Figs. 5, 6, 7 |
| $t_{PHL}$ | $S_1$ to GG | 1.5 | 9.6 | 2.0 | 6.0 | 9.0 | 1.9 | 9.7 | ns | $A_3$, $B_3$ |
| $t_{TLH}$ | Transition time[2] | 0.8 | 6.2 | 0.8 | 3.0 | 6.0 | 0.8 | 6.5 | ns | Figs. 5, 6, 7 |
| $t_{THL}$ | $S_1$ to GG | 0.8 | 6.2 | 0.8 | 3.0 | 6.0 | 0.8 | 6.5 | ns | $A_3$, $B_3$ |

**NOTES:**

1. Apply 1110mV to pins listed with 310mV applied to all other inputs.
2. All transition times are from 20% to 80% and 80% to 20% (refer to Figs. 5, 6, 7).

## AC WAVEFORMS

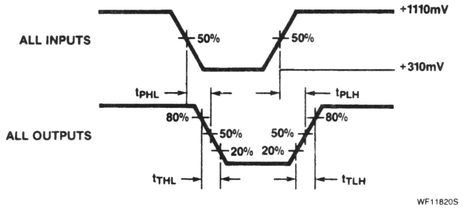
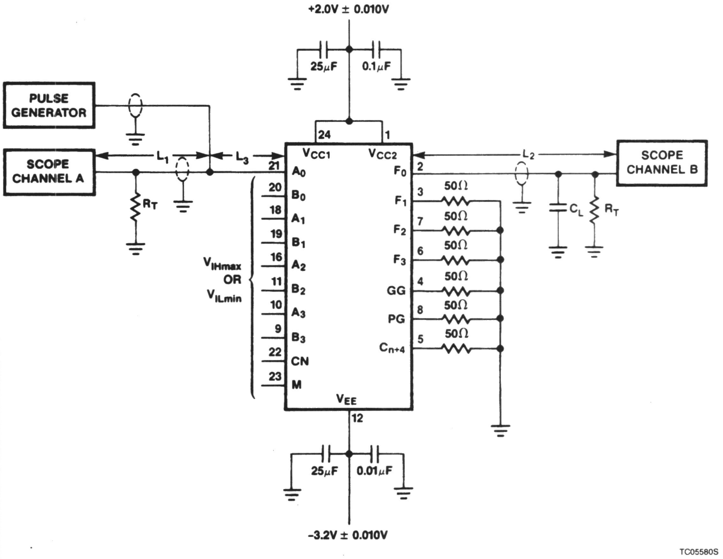


Figure 5. Propagation Delay and Transition Times

# Arithmetic Unit 10181

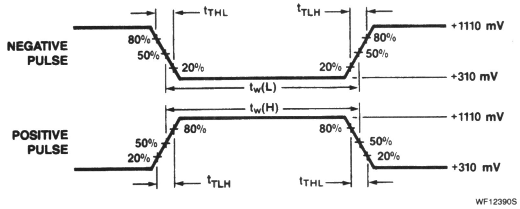
## TEST CIRCUITS AND WAVEFORMS


+2.0V ± 0.010V
25μF
0.1μF
PULSE GENERATOR
SCOPE CHANNEL A
L1
L3
RT
24
1
VCC1
VCC2
21 A0
20 B0
18 A1
19 B1
16 A2
11 B2
10 A3
9 B3
22 CN
23 M
VIHmax OR VILmin
F0 2
F1 3
F2 7
F3 6
GG 4
PG 8
Cn+4 5
50Ω
L2
SCOPE CHANNEL B
CL
RT
VEE
12
25μF
0.01μF
-3.2V ± 0.010V
TC05580S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$
2. Decoupling 0.1μF and 25μF from GND to $V_{CC}$, 0.01μF and 25μF from GND to $V_{EE}$. (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance ≤ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ±1% or better.

Figure 6. AC Test Circuit for 10181


NEGATIVE PULSE
POSITIVE PULSE
tTHL
tTLH
80%
50%
20%
tw(L)
tw(H)
+1110 mV
+310 mV
WF12390S

| INPUT PULSE REQUIREMENTS<br>$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$, $V_T$ = GND (0V) | | | | | |
|---|---|---|---|---|---|
| **Family** | **Amplitude** | **Rep Rate** | **Pulse Width** | $t_{TLH}$ | $t_{THL}$ |
| 10K ECL | 800mVp-p | 1MHz | 500ns | 2.0 ±0.2ns | 2.0 ±0.2ns |

Figure 7. Input Pulse Definition

Signetics

# 10188

## Hex Buffer

**Hex Buffer With Enable (Non-Inverting)**
***Product Specification***

**ECL Products**

## DESCRIPTION

The 10188 includes six buffers offering individual inputs and outputs and a common Enable input, driving all outputs LOW. Each input is connected to $V_{EE}$ via a pull-down resistor resulting in high input impedance and eliminating the need for connecting unused inputs LOW.

Due to open emitter outputs the 10188 features OR capability with high fan-out for driving 50Ω lines.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 10188 | 2.0ns | 33mA |

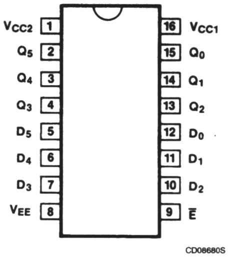
## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} = \text{GND}$; $V_{EE} = -5.2V$<br>$T_A = -30°C$ to $+85°C$ |
|---|---|
| Plastic DIP | 10188N |
| Ceramic DIP | 10188F |

## PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_0 - D_5$ | Data Inputs |
| $\overline{E}$ | Common Enable Input |
| $Q_0 - Q_5$ | Data Outputs |

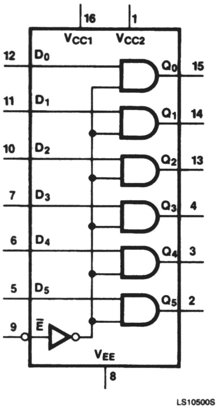
## PIN CONFIGURATION



$V_{CC2}$ 1
$Q_5$ 2
$Q_4$ 3
$Q_3$ 4
$D_5$ 5
$D_4$ 6
$D_3$ 7
$V_{EE}$ 8
16 $V_{CC1}$
15 $Q_0$
14 $Q_1$
13 $Q_2$
12 $D_0$
11 $D_1$
10 $D_2$
9 $\overline{E}$
CD08680S

Figure 1

## LOGIC SYMBOL

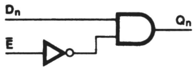


16
1
$V_{CC1}$
$V_{CC2}$
12 $D_0$
11 $D_1$
10 $D_2$
7 $D_3$
6 $D_4$
5 $D_5$
9 $\overline{E}$
$Q_0$ 15
$Q_1$ 14
$Q_2$ 13
$Q_3$ 4
$Q_4$ 3
$Q_5$ 2
$V_{EE}$
8
LS10500S

Figure 2

# Hex Buffer

# 10188



**LOGIC FUNCTION**
$Q_n = D_n \cdot E$

**Figure 3. Logic Diagram (One Buffer)**

## FUNCTION TABLE

| INPUTS | | OUTPUT |
|---|---|---|
| $\overline{E}$ | $D_n$ | $Q_n$ |
| L | L | L |
| L | H | H |
| H | X | L |

Positive Logic:
H = HIGH state = 1
L = LOW state = 0
X = Don't Care

## ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | | 10K ECL | UNIT |
|---|---|---|---|---|
| $V_{EE}$ | Supply voltage | | −8.0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | | 0 to $V_{EE}$ | V |
| $I_O$ | Output source current | | −50 | mA |
| $T_S$ | Storage temperature | | −55 to +150 | °C |
| $T_J$ | Maximum junction temperature | Ceramic package | +165 | °C |
| | | Plastic package | +155 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | 10K ECL | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | −5.2 | | V |
| $V_{IH}$ | HIGH level input voltage | $T_A = -30°C$ | | | −890 | mV |
| | | $T_A = +25°C$ | | | −810 | mV |
| | | $T_A = +85°C$ | | | −700 | mV |
| $V_{IHT}$ | HIGH level input threshold voltage | $T_A = -30°C$ | −1205 | | | mV |
| | | $T_A = +25°C$ | −1105 | | | mV |
| | | $T_A = +85°C$ | −1035 | | | mV |
| $V_{ILT}$ | LOW level input threshold voltage | $T_A = -30°C$ | | | −1500 | mV |
| | | $T_A = +25°C$ | | | −1475 | mV |
| | | $T_A = +85°C$ | | | −1440 | mV |
| $V_{IL}$ | LOW level input voltage | $T_A = -30°C$ | −1890 | | | mV |
| | | $T_A = +25°C$ | −1850 | | | mV |
| | | $T_A = +85°C$ | −1825 | | | mV |
| $T_A$ | Operating ambient temperature | | −30 | +25 | +85 | °C |

**NOTE:**
When operating at $V_{EE}$ other than specified voltage (−5.2V), the DC and AC Characteristics will vary slightly from specified values.
(See table of DC Characteristics)

**DC ELECTRICAL CHARACTERISTICS** $V_{CC1} = V_{CC2} =$ GND, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$, output loading with 50Ω to −2.0V ±0.010V unless otherwise specified[1,3]

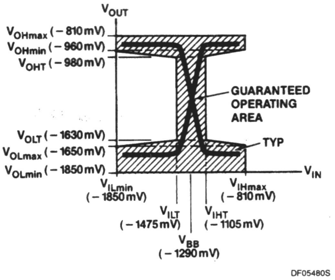
| PARAMETER | | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | | $T_A = -30°C$ | −1060 | | −890 | mV | Apply $V_{ILmin}$ to $\overline{E}$ input with $V_{IHmax}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | −960 | | −810 | mV | |
| | | | $T_A = +85°C$ | −890 | | −700 | mV | |
| $V_{OHT}$ | HIGH level output threshold voltage | | $T_A = -30°C$ | −1080 | | | mV | Apply $V_{ILT}$ to $\overline{E}$ input with $V_{IHmax}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | −980 | | | mV | |
| | | | $T_A = +85°C$ | −910 | | | mV | |
| $V_{OLT}$ | LOW level output threshold voltage | | $T_A = -30°C$ | | | −1655 | mV | Apply $V_{IHT}$ to $\overline{E}$ input with $V_{IHmax}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | | | −1630 | mV | |
| | | | $T_A = +85°C$ | | | −1595 | mV | |
| $V_{OL}$ | LOW level output voltage | | $T_A = -30°C$ | −1890 | | −1675 | mV | Apply $V_{ILmin}$ to all inputs. |
| | | | $T_A = +25°C$ | −1850 | | −1650 | mV | |
| | | | $T_A = +85°C$ | −1825 | | −1615 | mV | |
| $I_{IH}$ | HIGH level input current | Other inputs | $T_A = -30°C$ | | | 425 | µA | Apply $V_{IHmax}$ to each input under test, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | | | 265 | µA | |
| | | | $T_A = +85°C$ | | | 265 | µA | |
| | | $\overline{E}$ input | $T_A = -30°C$ | | | 460 | µA | Apply $V_{IHmax}$ to $\overline{E}$ with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | | | 290 | µA | |
| | | | $T_A = +85°C$ | | | 290 | µA | |
| $I_{IL}$ | LOW level input current | | $T_A = -30°C$ | 0.5 | | | µA | Apply $V_{ILmin}$ to each input under test, one at a time, with $V_{IHmax}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | 0.5 | | | µA | |
| | | | $T_A = +85°C$ | 0.3 | | | µA | |
| $-I_{EE}$ | $V_{EE}$ supply current | | $T_A = -30°C$ | | | 46 | mA | |
| | | | $T_A = +25°C$ | | 33 | 42 | mA | |
| | | | $T_A = +85°C$ | | | 46 | mA | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | | $T_A = +25°C$ | | 0.016 | | V/V | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | | 0.250 | | V/V | |
| $\frac{\Delta V_{BB}}{\Delta V_{EE}}$ | Reference bias voltage compensation | | | | 0.148 | | V/V | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst-case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 4.

## Hex Buffer

## 10188



$V_{IHmax}$ – Maximum HIGH level input voltage (the most positive $V_{IH}$).
$V_{IHT}$ – HIGH level input threshold voltage.
$V_{ILT}$ – LOW level input threshold voltage.
$V_{ILmin}$ – Minimum LOW level input voltage (the most negative $V_{IL}$).
$V_{OHmax}$ – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition.
$V_{OHmin}$ – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition.
$V_{OHT}$ – HIGH level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLT}$ – LOW level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLmax}$ – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions.
$V_{OLmin}$ – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions.
$V_{BB}$ – Reference bias voltage. The internally generated reference voltage which is used to set the input and output threshold level.

**Figure 4. Transfer Characteristics**

## AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$

| PARAMETER | | $T_A = -30°C$ | | $T_A = +25°C$ | | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Typ | Max | Min | Max | | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$D_n$ to $Q_n$ | 1.0<br>1.0 | 3.3<br>3.3 | 1.0<br>1.0 | 2.0<br>2.0 | 2.9<br>2.9 | 1.0<br>1.0 | 3.3<br>3.3 | ns<br>ns | Figs. 5, 7, 8 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$\overline{E}$ to $Q_n$ | 1.1<br>1.1 | 3.9<br>3.9 | 1.1<br>1.1 | 2.5<br>2.5 | 3.5<br>3.5 | 1.1<br>1.1 | 3.9<br>3.9 | ns<br>ns | Figs. 6, 7, 8 |
| $t_{TLH}$<br>$t_{THL}$ | Transition time<br>20% to 80%, 80% to 20% | 1.1<br>1.1 | 3.7<br>3.7 | 1.1<br>1.1 | 2.0<br>2.0 | 3.3<br>3.3 | 1.1<br>1.1 | 3.7<br>3.7 | ns<br>ns | Figs. 5, 6, 7, 8 |

## AC WAVEFORMS

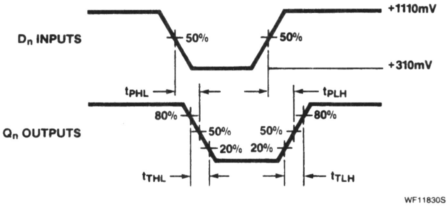


**Figure 5. Propagation Delay and Transition Times for Data to Output**

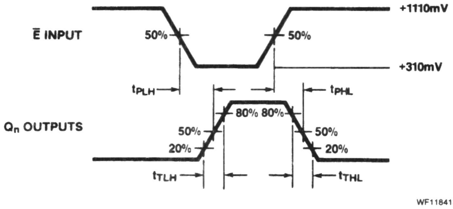
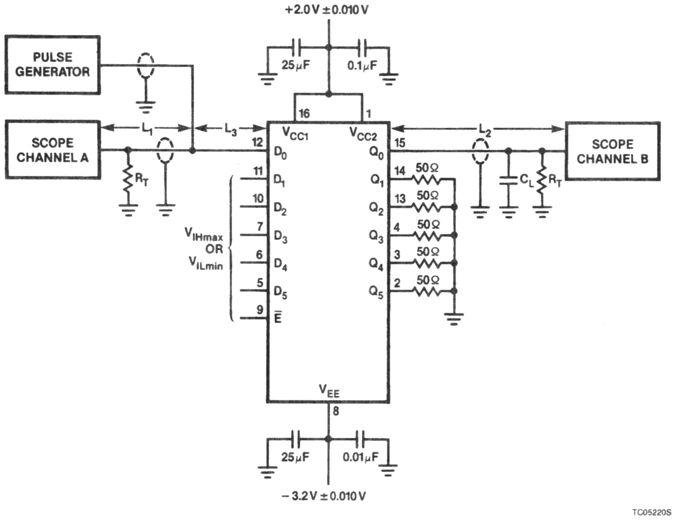


**Figure 6. Propagation Delay and Transition Times for Enable To Output**

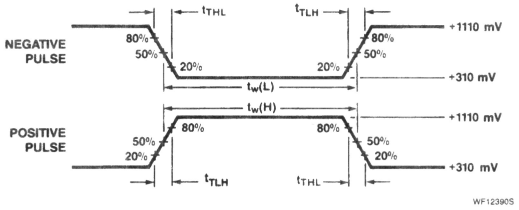
## TEST CIRCUITS AND WAVEFORMS


+2.0V ±0.010V
25µF
0.1µF
16
1
PULSE GENERATOR
SCOPE CHANNEL A
L1
L3
L2
12
$V_{CC1}$
$V_{CC2}$
$D_0$
$Q_0$
15
11
$D_1$
$Q_1$
14
50Ω
10
$D_2$
$Q_2$
13
50Ω
7
$D_3$
$Q_3$
4
50Ω
6
$D_4$
$Q_4$
3
50Ω
5
$D_5$
$Q_5$
2
50Ω
9
$\overline{E}$
$V_{IHmax}$ OR $V_{ILmin}$
$R_T$
$C_L$
$R_T$
SCOPE CHANNEL B
$V_{EE}$
8
25µF
0.01µF
−3.2V ±0.010V
TC05220S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$
2. Decoupling 0.1µF and 25µF from GND to $V_{CC}$, 0.01µF and 25µF from GND to $V_{EE}$. (0.01 and 0.1µF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance ≤ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.

Figure 7. AC Test Circuit for 10188


NEGATIVE PULSE
POSITIVE PULSE
$t_{THL}$
$t_{TLH}$
80%
50%
20%
20%
50%
80%
+1110 mV
+310 mV
$t_w(L)$
$t_w(H)$
+1110 mV
80%
80%
50%
20%
50%
20%
+310 mV
$t_{TLH}$
$t_{THL}$
WF12390S

**INPUT PULSE REQUIREMENTS**
**$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$, $V_T$ = GND (0V)**

| Family | Amplitude | Rep Rate | Pulse Width | $t_{TLH}$ | $t_{THL}$ |
|---|---|---|---|---|---|
| 10K ECL | 800mVp-p | 1MHz | 500ns | 2.0 ±0.2ns | 2.0 ±0.2ns |

Figure 8. Input Pulse Definition

**Signetics**

# 10189
## Inverter

**Hex Inverter With Enable**
***Product Specification***

**ECL Products**

## DESCRIPTION

The 10189 includes six inverters offering individual inputs and outputs and a common enable input, driving all outputs LOW. Each input is connected to $V_{EE}$ via a pull-down resistor resulting in high input impedance and eliminating the need for tying unused inputs LOW.

Due to open emitter outputs, the 10189 features OR capability with high fan-out for driving 50Ω lines.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 10189 | 2.0ns | 30mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} = GND$; $V_{EE} = -5.2V$<br>$T_A = -30°C$ to $+85°C$ |
|---|---|
| Plastic DIP | 10189N |
| Ceramic DIP | 10189F |

## PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_0 - D_5$ | Data Inputs |
| $\overline{E}$ | Common Enable Input |
| $\overline{Q}_0 - \overline{Q}_5$ | Data Outputs |

## PIN CONFIGURATION

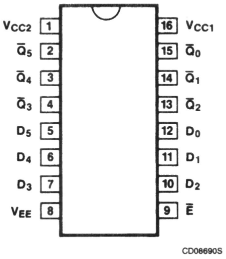

$V_{CC2}$ 1
$\overline{Q}_5$ 2
$\overline{Q}_4$ 3
$\overline{Q}_3$ 4
$D_5$ 5
$D_4$ 6
$D_3$ 7
$V_{EE}$ 8
16 $V_{CC1}$
15 $\overline{Q}_0$
14 $\overline{Q}_1$
13 $\overline{Q}_2$
12 $D_0$
11 $D_1$
10 $D_2$
9 $\overline{E}$
CD08690S

Figure 1

## LOGIC SYMBOL

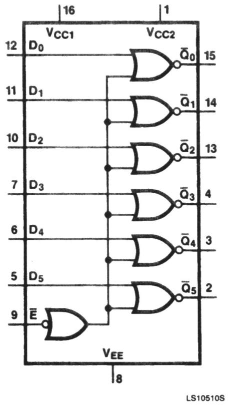
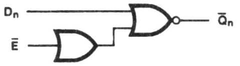

16
1
$V_{CC1}$
$V_{CC2}$
12 $D_0$
11 $D_1$
10 $D_2$
7 $D_3$
6 $D_4$
5 $D_5$
9 $\overline{E}$
$\overline{Q}_0$ 15
$\overline{Q}_1$ 14
$\overline{Q}_2$ 13
$\overline{Q}_3$ 4
$\overline{Q}_4$ 3
$\overline{Q}_5$ 2
$V_{EE}$
8
LS10510S

Figure 2

# Inverter

# 10189



LOGIC FUNCTION
$Q_n = \overline{D_n + \overline{E}}$
Positive logic
H = HIGH state (the more positive voltage) = 1
L = LOW state (the less positive voltage) = 0

LD04961S

**Figure 3. Logic Diagram (One Inverter)**

**ABSOLUTE MAXIMUM RATINGS** (Operation beyond the limits set forth in this table may impair useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | | 10K ECL | UNIT |
|---|---|---|---|---|
| $V_{EE}$ | Supply voltage | | -8.0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | | 0 to $V_{EE}$ | V |
| $I_O$ | Output source current | | -50 | mA |
| $T_S$ | Storage temperature | | -55 to +150 | °C |
| $T_J$ | Maximum junction temperature | Ceramic package | +165 | °C |
| | | Plastic package | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | 10K ECL | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | -5.2 | | V |
| $V_{IH}$ | HIGH level input voltage | $T_A$ = -30°C | | | -890 | mV |
| | | $T_A$ = +25°C | | | -810 | mV |
| | | $T_A$ = +85°C | | | -700 | mV |
| $V_{IHT}$ | HIGH level input threshold voltage | $T_A$ = -30°C | -1205 | | | mV |
| | | $T_A$ = +25°C | -1105 | | | mV |
| | | $T_A$ = +85°C | -1035 | | | mV |
| $V_{ILT}$ | LOW level input threshold voltage | $T_A$ = -30°C | | | -1500 | mV |
| | | $T_A$ = +25°C | | | -1475 | mV |
| | | $T_A$ = +85°C | | | -1440 | mV |
| $V_{IL}$ | LOW level input voltage | $T_A$ = -30°C | -1890 | | | mV |
| | | $T_A$ = +25°C | -1850 | | | mV |
| | | $T_A$ = +85°C | -1825 | | | mV |
| $T_A$ | Operating ambient temperature | | -30 | +25 | +85 | °C |

**NOTE:**
When operating at $V_{EE}$ other than specified voltage (-5.2V), the DC and AC Characteristics will vary slightly from specified values.
(See table of DC Characteristics)

## DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = GND, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$, output loading with 50Ω to $\pm 2.0V + 0.010V$ unless otherwise specified[1,3]

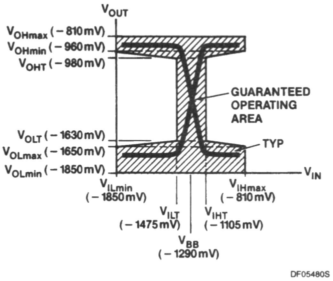
| PARAMETER | | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | | $T_A = -30°C$ | −1060 | | −890 | mV | Apply $V_{ILmin}$ to all inputs. |
| | | | $T_A = +25°C$ | −960 | | −810 | mV | |
| | | | $T_A = +85°C$ | −890 | | −700 | mV | |
| $V_{OHT}$ | HIGH level output threshold voltage | | $T_A = -30°C$ | −1080 | | | mV | Apply $V_{ILT}$ to each $D_n$ input one at a time, with $V_{ILmin}$ applied to $\overline{E}$ input and $V_{IHmax}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | −980 | | | mV | |
| | | | $T_A = +85°C$ | −910 | | | mV | |
| $V_{OLT}$ | LOW level output threshold voltage | | $T_A = -30°C$ | | | −1655 | mV | Apply $V_{IHT}$ to each $D_n$ input one at a time, with $V_{ILmin}$ applied to $\overline{E}$ input and $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | | | −1630 | mV | |
| | | | $T_A = +85°C$ | | | −1595 | mV | |
| $V_{OL}$ | LOW level output voltage | | $T_A = -30°C$ | −1890 | | −1675 | mV | Apply $V_{IHmax}$ to all $D_n$ inputs with $V_{ILmin}$ applied to $\overline{E}$ input. |
| | | | $T_A = +25°C$ | −1850 | | −1650 | mV | |
| | | | $T_A = +85°C$ | −1825 | | −1615 | mV | |
| $I_{IH}$ | HIGH level input current | Other inputs | $T_A = -30°C$ | | | 425 | μA | Apply $V_{IHmax}$ to each input under test, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | | | 265 | μA | |
| | | | $T_A = +85°C$ | | | 265 | μA | |
| | | $\overline{E}$ input | $T_A = -30°C$ | | | 890 | μA | Apply $V_{IHmax}$ to $\overline{E}$ input with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | | | 555 | μA | |
| | | | $T_A = +85°C$ | | | 555 | μA | |
| $I_{IL}$ | LOW level input current | | $T_A = -30°C$ | 0.5 | | | μA | Apply $V_{ILmin}$ to each input under test, one at at time, with $V_{IHmax}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | 0.5 | | | μA | |
| | | | $T_A = +85°C$ | 0.3 | | | μA | |
| $-I_{EE}$ | $V_{EE}$ supply current | | $T_A = -30°C$ | | | 44 | mA | |
| | | | $T_A = +25°C$ | | 30 | 40 | mA | |
| | | | $T_A = +85°C$ | | | 44 | mA | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | | $T_A = +25°C$ | | 0.016 | | V/V | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | | 0.250 | | V/V | |
| $\frac{\Delta V_{BB}}{\Delta V_{EE}}$ | Reference bias voltage compensation | | | | 0.148 | | V/V | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst-case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 4.

## Inverter

## 10189



**NOTES:**

$V_{IHmax}$ – Maximum HIGH level input voltage (the most positive $V_{IH}$).
$V_{IHT}$ – HIGH level input threshold voltage.
$V_{ILT}$ – LOW level input threshold voltage.
$V_{ILmin}$ – Minimum LOW level input voltage (the most negative $V_{IL}$).
$V_{OHmax}$ – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition.
$V_{OHmin}$ – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition.
$V_{OHT}$ – HIGH level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLT}$ – LOW level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLmax}$ – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions.
$V_{OLmin}$ – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions.
$V_{BB}$ – Reference bias voltage (the internally generated reference voltage which is used to set the input and output threshold level).

Figure 4. Transfer Characteristics

## AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$

| PARAMETER | | $T_A = -30°C$ | | $T_A = +25°C$ | | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Typ | Max | Min | Max | | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$D_n$ to $\overline{Q}_n$ | 1.0<br>1.0 | 3.3<br>3.3 | 1.0<br>1.0 | 2.0<br>2.0 | 2.9<br>2.9 | 1.0<br>1.0 | 3.3<br>3.3 | ns<br>ns | Figs. 5, 7, 8 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$\overline{E}$ to $\overline{Q}_n$ | 1.1<br>1.1 | 3.9<br>3.9 | 1.1<br>1.1 | 2.5<br>2.5 | 3.5<br>3.5 | 1.1<br>1.1 | 3.9<br>3.9 | ns<br>ns | Figs. 6, 7, 8 |
| $t_{TLH}$<br>$t_{THL}$ | Transition time<br>20% to 80%, 80% to 20% | 1.1<br>1.1 | 3.6<br>3.6 | 1.1<br>1.1 | 2.0<br>2.0 | 3.3<br>3.3 | 1.1<br>1.1 | 3.7<br>3.7 | ns<br>ns | Figs. 5, 6, 7, 8 |

## AC WAVEFORMS

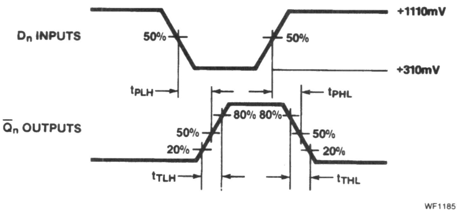

$D_n$ INPUTS
+1110mV
50%
50%
+310mV
$t_{PLH}$
$t_{PHL}$
$\overline{Q}_n$ OUTPUTS
80% 80%
50%
20%
50%
20%
$t_{TLH}$
$t_{THL}$
WF11851S

Figure 5. Propagation Delay and Transition Times for Data to Output

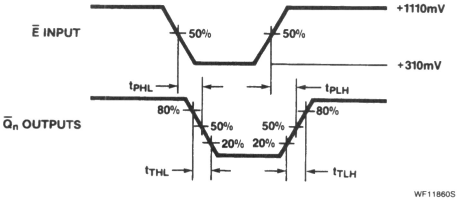
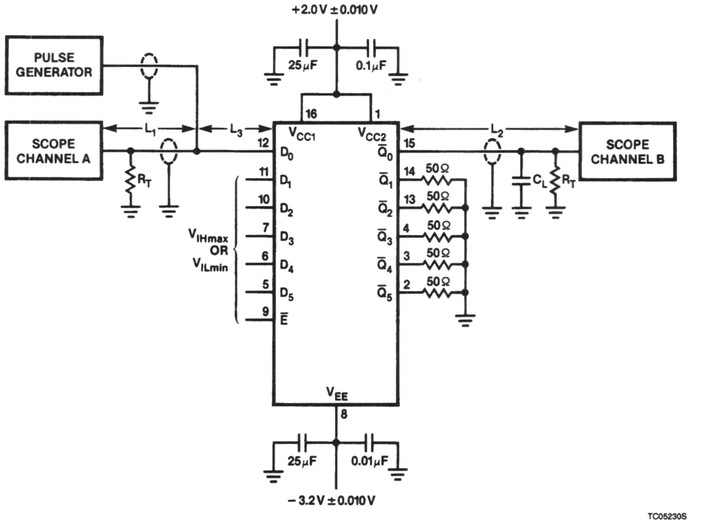

$\overline{E}$ INPUT
+1110mV
50%
50%
+310mV
$t_{PHL}$
$t_{PLH}$
$\overline{Q}_n$ OUTPUTS
80%
80%
50%
50%
20% 20%
$t_{THL}$
$t_{TLH}$
WF11860S

Figure 6. Propagation Delay and Transition Times for Enable to Output

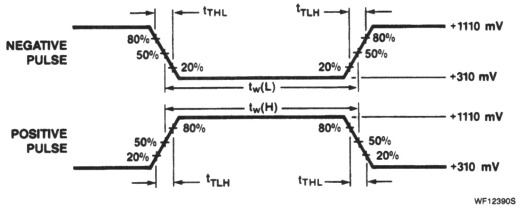
## TEST CIRCUITS AND WAVEFORMS


+2.0V ±0.010V
25μF
0.1μF
PULSE GENERATOR
SCOPE CHANNEL A
L1
L3
R_T
16
1
12
V_CC1
V_CC2
D0
Q̄0
15
11
D1
Q̄1
14
50Ω
10
D2
Q̄2
13
50Ω
7
D3
Q̄3
4
50Ω
6
D4
Q̄4
3
50Ω
5
D5
Q̄5
2
50Ω
9
Ē
V_IHmax OR V_ILmin
L2
C_L
R_T
SCOPE CHANNEL B
V_EE
8
25μF
0.01μF
−3.2V ±0.010V
TC05230S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1μF and 25μF from GND to $V_{CC}$, 0.01μF and 25μF from GND to $V_{EE}$. (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T = 50\Omega$ terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance $\leqslant$ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ±1% or better.

Figure 7. AC Test Circuit for 10189


NEGATIVE PULSE
t_THL
t_TLH
80%
50%
20%
20%
80%
50%
t_w(L)
+1110 mV
+310 mV
POSITIVE PULSE
t_w(H)
80%
80%
50%
20%
50%
20%
t_TLH
t_THL
+1110 mV
+310 mV
WF12390S

| INPUT PULSE REQUIREMENTS<br>$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$, $V_T$ = GND (0V) | | | | | |
|---|---|---|---|---|---|
| **Family** | **Amplitude** | **Rep Rate** | **Pulse Width** | $t_{TLH}$ | $t_{THL}$ |
| 10K ECL | 800mVp-p | 1MHz | 500ns | 2.0 ±0.2ns | 2.0 ±0.2ns |

Figure 8. Input Pulse Definition

**Signetics**

# 10192
# Bus Driver

**Quad Bus Driver**
***Product Specification***

**ECL Products**

## DESCRIPTION

The 10192 contains four line drivers with complementary outputs. Each driver has a Data ($D_n$) input and shares an Enable ($\overline{E}_n$) input with another driver. The two driver outputs are the uncommitted collectors of a pair of NPN transistors operating as a current switch. Each driver accepts 10K ECL input signals and provides a nominal signal of 800mV across a 50Ω load at each output collector. Outputs can drive higher values of load resistance, provided that the combination of IR drop and load return voltage VLR does not cause an output collector to go more negative than −2.4V with respect to $V_{CC}$. To avoid output transistor breakdown, the load return voltage should not be more positive than +5.5V with respect to $V_{CC}$. When the $\overline{E}_n$ input is HIGH, both output transistors of a driver are nonconducting. When not used, the $\overline{E}_n$ inputs, as well as the $D_n$ inputs, may be left open.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 10192 | 3.0ns | 110mA |

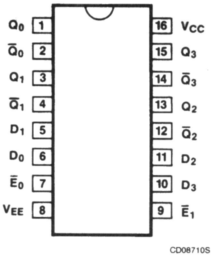
## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC}$ = GND; $V_{EE}$ = −5.2V<br>$T_A$ = −30°C to +85°C |
|---|---|
| Plastic DIP | 10192N |
| Ceramic DIP | 10192F |

## PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_0 - D_3$ | Data Inputs |
| $\overline{E}_0$, $\overline{E}_1$ | Enable Inputs |
| $Q_0 - Q_3$, $\overline{Q}_0 - \overline{Q}_3$ | Data Outputs |

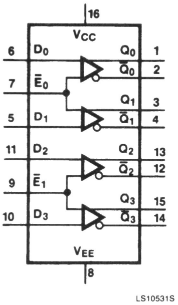
## PIN CONFIGURATION



Q0 1
Q̄0 2
Q1 3
Q̄1 4
D1 5
D0 6
Ē0 7
VEE 8
16 VCC
15 Q3
14 Q̄3
13 Q2
12 Q̄2
11 D2
10 D3
9 Ē1
CD08710S

Figure 1

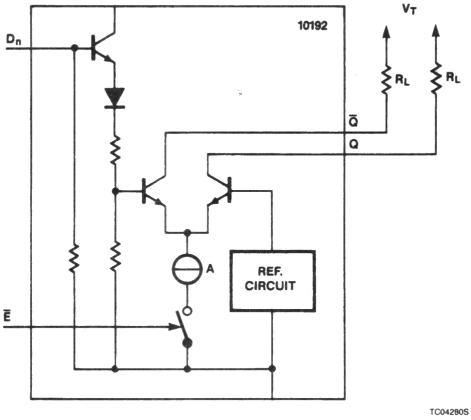
## LOGIC SYMBOL



16
VCC
6 D0
7 Ē0
5 D1
11 D2
9 Ē1
10 D3
Q0 1
Q̄0 2
Q1 3
Q̄1 4
Q2 13
Q̄2 12
Q3 15
Q̄3 14
VEE
8
LS10531S

Figure 2

# Bus Driver 10192



**NOTES:**
A = 16mA switched current source.
$V_T$ should not exceed +5.5V and $R_L$ and $V_T$ should be chosen so that $V_C$ does not go more negative than −2.4V.

**Figure 3. Simplified Circuit Diagram**

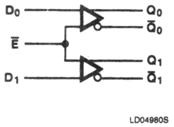


**Figure 4. Logic Function**

**Basic driver operation**
$V_{OH} = V_T$
$V_{OL} = V_T - 0.016.\ R_L$ (typ.)

## FUNCTION TABLE

| INPUTS | | OUTPUTS | | | |
|---|---|---|---|---|---|
| | | Current | | Voltage | |
| $\bar{E}$ | D | $\bar{Q}$ | Q | $\bar{Q}$ | Q |
| L | L | L | H | H | L |
| L | H | H | L | L | H |
| H | X | L | L | H | H |

Positive Logic:
H (Voltage) = HIGH state (the more positive voltage) = 1
H (Current) = Output transistor not conducting (the least current flow)
L (Voltage) = LOW state (the more negative voltage) = 0
L (Current) = Output transistor conducting (the most current flow)
X = Don't Care
Z = High Impedance (Current source turned off)

# Bus Driver

# 10192

**ABSOLUTE MAXIMUM RATINGS** (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | | 10K ECL | UNIT |
|---|---|---|---|---|
| $V_{EE}$ | Supply voltage | | -8.0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | | 0 to $V_{EE}$ | V |
| $V_T$ | Load termination voltage | | 5.5 | V |
| $V_O$ | Output voltage (at collector) | Max | +5.5 | V |
| | | Min | -2.4 | V |
| $T_S$ | Storage temperature | | -55 to +150 | °C |
| $T_J$ | Maximum junction temperature | Ceramic package | +165 | °C |
| | | Plastic package | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | 10K ECL | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | |
| $V_{CC}$ | Circuit ground | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | -5.2 | | V |
| $V_{IH}$ | HIGH level input voltage | $T_A = -30°C$ | | | -890 | mV |
| | | $T_A = +25°C$ | | | -810 | mV |
| | | $T_A = +85°C$ | | | -700 | mV |
| $V_{IHT}$ | HIGH level input threshold voltage | $T_A = -30°C$ | -1205 | | | mV |
| | | $T_A = +25°C$ | -1105 | | | mV |
| | | $T_A = +85°C$ | -1035 | | | mV |
| $V_{ILT}$ | LOW level input threshold voltage | $T_A = -30°C$ | | | -1500 | mV |
| | | $T_A = +25°C$ | | | -1475 | mV |
| | | $T_A = +85°C$ | | | -1440 | mV |
| $V_{IL}$ | LOW level input voltage | $T_A = -30°C$ | -1890 | | | mV |
| | | $T_A = +25°C$ | -1850 | | | mV |
| | | $T_A = +85°C$ | -1825 | | | mV |
| $T_A$ | Operating ambient temperature | | -30 | +25 | +85 | °C |

**NOTE:**
When operating at $V_{EE}$ other than specified voltage (-5.2V), the DC and AC Characteristics will vary slightly from specified values. (See table of DC Characteristics)

**DC ELECTRICAL CHARACTERISTICS** $V_{CC}$ = GND, $V_{EE}$ = −5.2V ±0.010V, $T_A$ = −30°C to +85°C, output loading with 50Ω to $V_T$ unless otherwise specified[1, 3]

| PARAMETER | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] |
|---|---|---|---|---|---|---|---|
| $I_{OH}$ | Output current HIGH state | $T_A$ = −30°C | | | 2.0 | mA | For $\overline{Q}$ outputs, apply $V_{ILmin}$ to all inputs.<br>For Q outputs, apply $V_{ILmin}$ to $\overline{E}_n$ inputs with $V_{IHmax}$ applied to $D_n$ inputs. |
| | | $T_A$ = +25°C | | | 2.0 | mA | |
| | | $T_A$ = +85°C | | | 2.0 | mA | |
| $I_{OHT}$ | Output threshold current HIGH state | $T_A$ = −30°C | | | | mA | For Q outputs, apply $V_{IHT}$ to each $D_n$ input, one at a time, with $V_{ILmin}$ applied to all other inputs.<br>For $\overline{Q}$ outputs, apply $V_{ILT}$ to each $D_n$ input, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | $T_A$ = +25°C | | | 2.0 | mA | |
| | | $T_A$ = +85°C | | | | mA | |
| $I_{OLT}$ | Output threshold current LOW state | $T_A$ = −30°C | 13.5 | | | mA | For Q outputs, apply $V_{ILT}$ to each $D_n$ input, one at a time, with $V_{ILmin}$ applied to all other inputs.<br>For $\overline{Q}$ outputs, apply $V_{IHT}$ to each $D_n$ input, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | $T_A$ = +25°C | 14 | | | mA | |
| | | $T_A$ = +85°C | 14 | | | mA | |
| $I_{OL}$ | Output current LOW state | $T_A$ = −30°C | 13.5 | | 18 | mA | For $\overline{Q}$ outputs, apply $V_{IHmax}$ to $D_n$ inputs with $V_{ILmin}$ applied to $\overline{E}_n$ inputs.<br>For Q outputs, apply $V_{ILmin}$ to all inputs. |
| | | $T_A$ = +25°C | 14 | | 18 | mA | |
| | | $T_A$ = +85°C | 14 | | 19 | mA | |
| $I_{OZ}$ | Output leakage current HIGH impedance | $T_A$ = −30°C | | | 300 | μA | Apply $V_{IHmax}$ to all inputs. |
| | | $T_A$ = +25°C | | | 300 | μA | |
| | | $T_A$ = +85°C | | | 300 | μA | |
| $I_{IH}$ | HIGH level input current | $T_A$ = −30°C | | | 425 | μA | Apply $V_{IHmax}$ to each input under test, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | $T_A$ = +25°C | | | 265 | μA | |
| | | $T_A$ = +85°C | | | 265 | μA | |
| $I_{IL}$ | LOW level input current | $T_A$ = −30°C | 0.5 | | | μA | Apply $V_{ILmin}$ to each input under test, one at a time, with $V_{IHmax}$ applied to all other inputs. |
| | | $T_A$ = +25°C | 0.5 | | | μA | |
| | | $T_A$ = +85°C | 0.3 | | | μA | |
| $-I_{EE}$ | $V_{EE}$ supply current | $T_A$ = −30°C | | | 154 | mA | |
| | | $T_A$ = +25°C | | 110 | 140 | mA | |
| | | $T_A$ = +85°C | | | 154 | mA | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | $T_A$ = +25°C | | 0.016 | | V/V | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | 0.250 | | V/V | |
| $\frac{\Delta V_{BB}}{\Delta V_{EE}}$ | Reference bias voltage compensation | | | 0.148 | | V/V | |

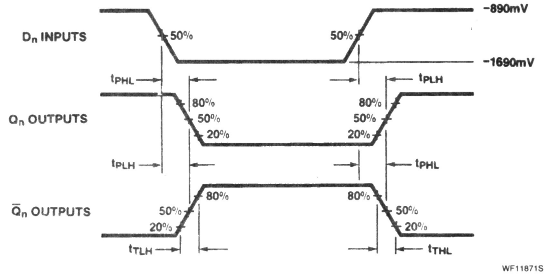
**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges
2. Conditions for testing shown in the tables are not necessarily worst case. For worst-case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board.

## AC ELECTRICAL CHARACTERISTICS $V_{CC}$ = 0V (GND), $V_{EE}$ = −5.2V ±0.010V, $V_T$ = GND (0V)

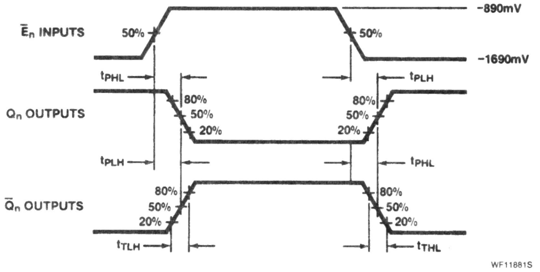
| PARAMETER | | $T_A$ = 30°C | | $T_A$ = +25°C | | | $T_A$ = +85°C | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Typ | Max | Min | Max | | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$D_n$ to $Q_n$, $\overline{Q}_n$ | 2.0<br>2.0 | 4.7<br>4.7 | 2.0<br>2.0 | 3.0<br>3.0 | 4.5<br>4.5 | 2.0<br>2.0 | 4.8<br>4.8 | ns<br>ns | Figs. 5, 7, 8 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$\overline{E}_n$ to $Q_n$, $\overline{Q}_n$ | 2.5<br>2.5 | 6.3<br>6.3 | 2.5<br>2.5 | 3.5<br>3.5 | 6.0<br>6.0 | 2.5<br>2.5 | 6.6<br>6.6 | ns<br>ns | Figs. 6, 7, 8 |
| $t_{TLH}$<br>$t_{THL}$ | Transition time<br>20% to 80%, 80% to 20% | 1.3<br>1.3 | 3.5<br>3.5 | 1.3<br>1.3 | 2.3<br>2.3 | 3.3<br>3.3 | 1.3<br>1.3 | 3.5<br>3.5 | ns<br>ns | Figs. 5, 6, 7, 8 |

## AC WAVEFORMS


$D_n$ INPUTS
50%
50%
−890mV
−1690mV
$t_{PHL}$
$t_{PLH}$
$Q_n$ OUTPUTS
80%
50%
20%
80%
50%
20%
$t_{PLH}$
$t_{PHL}$
$\overline{Q}_n$ OUTPUTS
80%
80%
50%
20%
50%
20%
$t_{TLH}$
$t_{THL}$
WF11871S

NOTE:
Output waveforms represent voltage across load resistor ($R_L$).

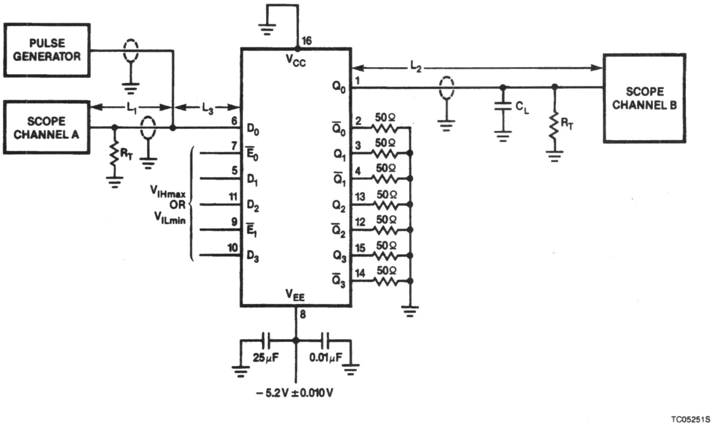
Figure 5. Propagation Delay and Transition Times for Data to Outputs


$\overline{E}_n$ INPUTS
50%
50%
−890mV
−1690mV
$t_{PHL}$
$t_{PLH}$
$Q_n$ OUTPUTS
80%
50%
20%
80%
50%
20%
$t_{PLH}$
$t_{PHL}$
$\overline{Q}_n$ OUTPUTS
80%
50%
20%
80%
50%
20%
$t_{TLH}$
$t_{THL}$
WF11881S

NOTE:
Output waveforms represent voltage across load resistor ($R_L$).

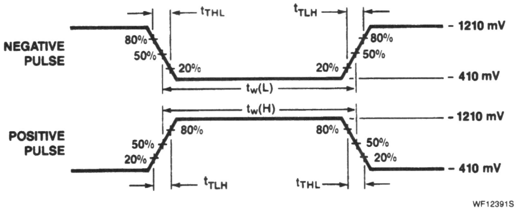
Figure 6. Propagation Delay and Transition Times for Enable to Outputs

## TEST CIRCUITS AND WAVEFORMS


PULSE GENERATOR
SCOPE CHANNEL A
SCOPE CHANNEL B
L1
L2
L3
RT
CL
16
VCC
VEE
8
1
Q0
2
$\overline{Q}_0$
3
Q1
4
$\overline{Q}_1$
13
Q2
12
$\overline{Q}_2$
15
Q3
14
$\overline{Q}_3$
50Ω
6
D0
7
$\overline{E}_0$
5
D1
11
D2
9
$\overline{E}_1$
10
D3
VIHmax OR VILmin
25μF
0.01μF
−5.2V ±0.010V
TC05251S

NOTES:
1. $V_{CC1} = V_{CC2}$ = GND (0V), $V_{EE}$ = −5.2V ±0.010V.
2. Decoupling 0.01μF and 25μF from GND to $V_{EE}$ (0.01μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than ¼ inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed ¼ inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than ¼ inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance ≤ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed ¼ inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ±1% or better.

Figure 7. AC Test Circuit for 10192


NEGATIVE PULSE
POSITIVE PULSE
tTHL
tTLH
80%
50%
20%
tw(L)
tw(H)
1210 mV
410 mV
WF12391S

| INPUT PULSE REQUIREMENTS<br>$V_{CC1}$ = GND (0V), $V_{EE}$ = −5.2V ±0.010V, $V_T$ = GND (0V) | | | | | |
|---|---|---|---|---|---|
| **Family** | **Amplitude** | **Rep Rate** | **Pulse Width** | **$t_{TLH}$** | **$t_{THL}$** |
| 10K ECL | 800mVp-p | 1MHz | 500ns | 2.0 ±0.2ns | 2.0 ±0.2ns |

Figure 8. Input Pulse Definition

# 10210
## Line Driver

**High-Speed Dual 3-Input/3-Output OR Line Driver**
***Product Specification***

### DESCRIPTION

The 10210 is a high-speed dual 3-input/3-output OR line driver intended to drive up to six transmission lines simultaneously. This feature makes the device particularly useful in clock distribution applications. The 10210 is a higher speed version of the 10110. It is a pin-for-pin replacement for the device. All unused inputs can be left open due to integrated pull-down resistors, which avoid the need for a supply voltage.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 10210 | 1.5ns | 31mA |

### ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} = GND$; $V_{EE} = -5.2V$<br>$T_A = -30°C$ to $+85°C$ |
|---|---|
| Plastic DIP | 10210N |
| Ceramic DIP | 10210F |

### PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_0 - D_5$ | Data Inputs |
| $Q_0 - Q_5$ | Data Outputs (OR) |

### PIN CONFIGURATION

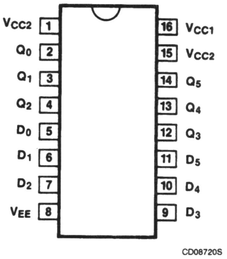

VCC2 1
Q0 2
Q1 3
Q2 4
D0 5
D1 6
D2 7
VEE 8
16 VCC1
15 VCC2
14 Q5
13 Q4
12 Q3
11 D5
10 D4
9 D3
CD08720S

Figure 1

### LOGIC SYMBOL

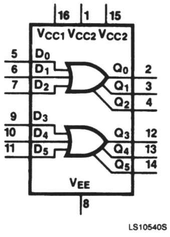

16 1 15
VCC1 VCC2 VCC2
5 D0
6 D1
7 D2
Q0 2
Q1 3
Q2 4
9 D3
10 D4
11 D5
Q3 12
Q4 13
Q5 14
VEE
8
LS10540S

Figure 2

# Line Driver 10210

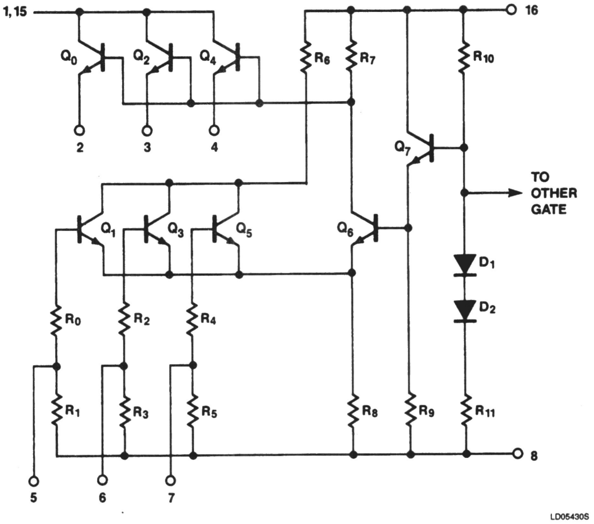
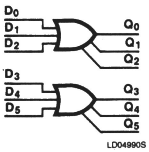

1, 15
16
Q0
Q2
Q4
R6
R7
R10
2
3
4
Q7
TO OTHER GATE
Q1
Q3
Q5
Q6
D1
D2
R0
R2
R4
R1
R3
R5
R8
R9
R11
8
5
6
7
LD05430S

Figure 3. Circuit Diagram (One Gate)


D0
D1
D2
Q0
Q1
Q2
D3
D4
D5
Q3
Q4
Q5
LD04990S

$Q_0 = Q_1 = Q_2 = D_0 + D_1 + D_2$
$Q_3 = Q_4 = Q_5 = D_3 + D_4 + D_5$

**Positive Logic:**
**HIGH state (the more positive voltage) = 1**
**LOW state (the less positive voltage) = 0**

Figure 4. Logic Diagram

## Line Driver

## 10210

**ABSOLUTE MAXIMUM RATINGS** (Operation beyond the limits set forth in this table may impair useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | | 10K ECL | UNIT |
|---|---|---|---|---|
| $V_{EE}$ | Supply voltage | | −8.0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | | 0 to $V_{EE}$ | V |
| $I_O$ | Output source current | | −50 | mA |
| $T_S$ | Storage temperature | | −55 to +150 | °C |
| $T_J$ | Maximum junction temperature | Ceramic package | +165 | °C |
| | | Plastic package | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | 10K ECL | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | −5.2 | | V |
| $V_{IH}$ | HIGH level input voltage | $T_A = -30°C$ | | | −890 | mV |
| | | $T_A = +25°C$ | | | −810 | mV |
| | | $T_A = +85°C$ | | | −700 | mV |
| $V_{IHT}$ | HIGH level input threshold voltage | $T_A = -30°C$ | −1205 | | | mV |
| | | $T_A = +25°C$ | −1105 | | | mV |
| | | $T_A = +85°C$ | −1035 | | | mV |
| $V_{ILT}$ | LOW level input threshold voltage | $T_A = -30°C$ | | | −1500 | mV |
| | | $T_A = +25°C$ | | | −1475 | mV |
| | | $T_A = +85°C$ | | | −1440 | mV |
| $V_{IL}$ | LOW level input voltage | $T_A = -30°C$ | −1890 | | | mV |
| | | $T_A = +25°C$ | −1850 | | | mV |
| | | $T_A = +85°C$ | −1825 | | | mV |
| $T_A$ | Operating ambient temperature | | −30 | +25 | +85 | °C |

**NOTE:**
When operating at $V_{EE}$ other than specified voltage (−5.2V), the DC and AC Characteristics will vary slightly from specified values.
(See table of DC Characteristics)

## DC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$, output loading with 50Ω to −2.0V ±0.010V unless otherwise specified[1,3]

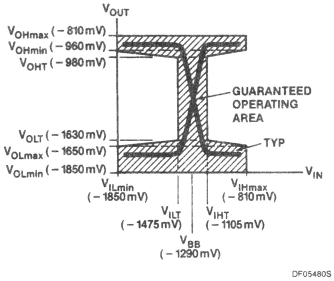
| PARAMETER | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | $T_A = -30°C$ | −1060 | | −890 | mV | Apply $V_{IHmax}$ to all inputs. |
| | | $T_A = +25°C$ | −960 | | −810 | mV | |
| | | $T_A = +85°C$ | −890 | | −700 | mV | |
| $V_{OHT}$ | HIGH level output threshold voltage | $T_A = -30°C$ | −1080 | | | mV | Apply $V_{IHT}$ to each $D_n$ input, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | $T_A = +25°C$ | −980 | | | mV | |
| | | $T_A = +85°C$ | −910 | | | mV | |
| $V_{OLT}$ | LOW level output threshold voltage | $T_A = -30°C$ | | | −1655 | mV | Apply $V_{ILT}$ to each $D_n$ input, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | $T_A = +25°C$ | | | −1630 | mV | |
| | | $T_A = +85°C$ | | | −1595 | mV | |
| $V_{OL}$ | LOW level output voltage | $T_A = -30°C$ | −1890 | | −1675 | mV | Apply $V_{ILmin}$ to all inputs. |
| | | $T_A = +25°C$ | −1850 | | −1650 | mV | |
| | | $T_A = +85°C$ | −1825 | | −1615 | mV | |
| $I_{IH}$ | HIGH level input current | $T_A = -30°C$ | | | 650 | µA | Apply $V_{IHmax}$ to each input under test, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | $T_A = +25°C$ | | | 410 | µA | |
| | | $T_A = +85°C$ | | | 410 | µA | |
| $I_{IL}$ | LOW level input current | $T_A = -30°C$ | 0.5 | | | µA | Apply $V_{ILmin}$ to each input under test, one at a time, with $V_{IHmax}$ applied to all other inputs. |
| | | $T_A = +25°C$ | 0.5 | | | µA | |
| | | $T_A = +85°C$ | 0.3 | | | µA | |
| $-I_{EE}$ | $V_{EE}$ supply current | $T_A = -30°C$ | | | 42 | mA | |
| | | $T_A = +25°C$ | | 31 | 38 | mA | |
| | | $T_A = +85°C$ | | | 42 | mA | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | $T_A = +25°C$ | | 0.016 | | V/V | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | 0.250 | | V/V | |
| $\frac{\Delta V_{BB}}{\Delta V_{EE}}$ | Reference bias voltage compensation | | | 0.148 | | V/V | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst-case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 5.

# Line Driver

# 10210



**NOTES:**

$V_{IHmax}$ – Maximum HIGH level input voltage (the most positive $V_{IH}$).
$V_{IHT}$ – HIGH level input threshold voltage.
$V_{ILT}$ – LOW level input threshold voltage.
$V_{ILmin}$ – Minimum LOW level input voltage (the most negative $V_{IL}$).
$V_{OHmax}$ – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition.
$V_{OHmin}$ – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition.
$V_{OHT}$ – HIGH level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLT}$ – LOW level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLmax}$ – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions.
$V_{OLmin}$ – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions.
$V_{BB}$ – Reference bias voltage (the internally generated reference voltage which is used to set the input and output threshold level).

**Figure 5. Transfer Characteristics**

## AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$

| PARAMETER | $T_A = -30°C$ | | $T_A = +25°C$ | | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Typ | Max | Min | Max | | |
| $t_{PLH}$ Propagation delay | 1.0 | 2.6 | 1.0 | 1.5 | 2.5 | 1.0 | 2.8 | ns | Figs. 6, 7, 8 |
| $t_{PHL}$ $D_n$ to $Q_n$ | 1.0 | 2.6 | 1.0 | 1.5 | 2.5 | 1.0 | 2.8 | ns | |
| $t_{TLH}$ Transition time | 1.0 | 2.6 | 1.0 | 1.5 | 2.5 | 1.0 | 2.8 | ns | Figs. 6, 7, 8 |
| $t_{THL}$ 20% to 80%, 80% to 20% | 1.0 | 2.6 | 1.0 | 1.5 | 2.5 | 1.0 | 2.8 | ns | |

## AC WAVEFORMS

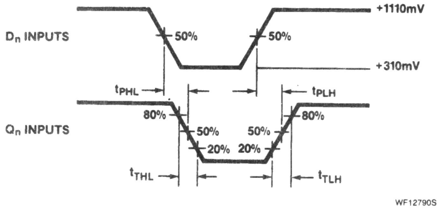
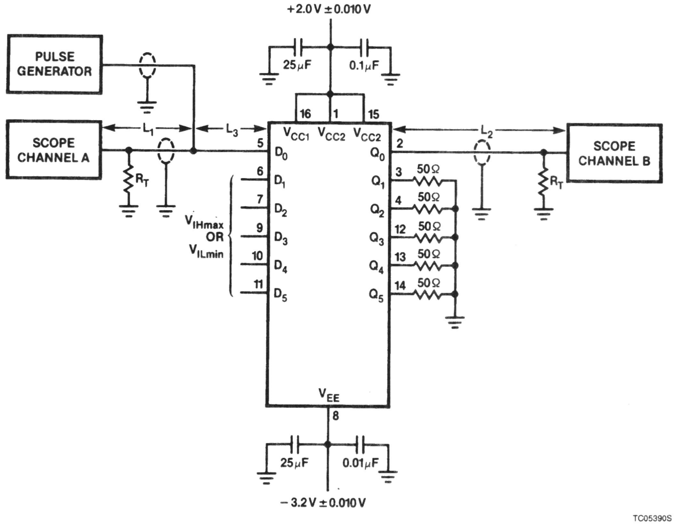


**Figure 6. Propagation Delay and Transition Times for Data to Output**

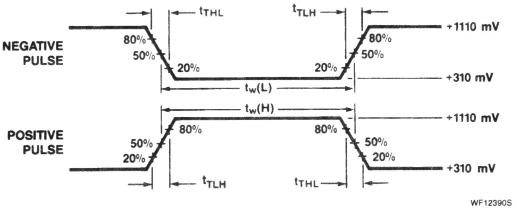
## TEST CIRCUITS AND WAVEFORMS


+2.0V ±0.010V
25μF
0.1μF
PULSE GENERATOR
SCOPE CHANNEL A
L1
L3
L2
RT
16
1
15
VCC1 VCC2 VCC2
5 D0
6 D1
7 D2
9 D3
10 D4
11 D5
VIHmax OR VILmin
2 Q0
3 Q1
4 Q2
12 Q3
13 Q4
14 Q5
50Ω
SCOPE CHANNEL B
VEE
8
25μF
0.01μF
−3.2V ±0.010V
TC05390S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$
2. Decoupling 0.1μF and 25μF from GND to $V_{CC}$, 0.01μF and 25μF from GND to $V_{EE}$. (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance ⩽ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ±1% or better.

Figure 7. AC Test Circuit for 10210


NEGATIVE PULSE
POSITIVE PULSE
tTHL
tTLH
80%
50%
20%
tw(L)
tw(H)
+1110 mV
+310 mV
WF12390S

**INPUT PULSE REQUIREMENTS**

**$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$, $V_T$ = GND (0V)**

| Family | Amplitude | Rep Rate | Pulse Width | $t_{TLH}$ | $t_{THL}$ |
|---|---|---|---|---|---|
| 10K ECL | 800mVp-p | 1MHz | 500ns | 2.0 ±0.2ns | 2.0 ±0.2ns |

Figure 8. Input Pulse Definition

# 10211

# Line Driver

**High-Speed Dual 3-Input/3-Output NOR Line Driver**
***Product Specification***

## DESCRIPTION

The 10211 is a high-speed dual 3-input/3-output NOR line driver intended to drive up to three transmission lines simultaneously. This feature makes the device particularly useful in clock distribution applications. The 10211 is a higher speed version of 10111. It is a pin-for-pin replacement for this type. All unused inputs can be left open due to integrated pull-down resistors, which avoid the need for a supply voltage.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 10211 | 1.5ns | 30mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} = GND$; $V_{EE} = -5.2V$<br>$T_A = -30°C$ to $+85°C$ |
|---|---|
| Plastic DIP | 10210N |
| Ceramic DIP | 10210F |

## PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_0 - D_5$ | Data Inputs |
| $\overline{Q}_0 - \overline{Q}_5$ | Data Outputs |

## PIN CONFIGURATION

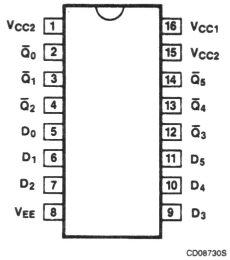

VCC2 1
Q̄0 2
Q̄1 3
Q̄2 4
D0 5
D1 6
D2 7
VEE 8
16 VCC1
15 VCC2
14 Q̄5
13 Q̄4
12 Q̄3
11 D5
10 D4
9 D3
CD08730S

Figure 1

## LOGIC SYMBOL

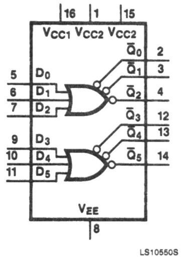

16
1
15
VCC1 VCC2 VCC2
Q̄0 2
Q̄1 3
Q̄2 4
5 D0
6 D1
7 D2
Q̄3 12
Q̄4 13
Q̄5 14
9 D3
10 D4
11 D5
VEE
8
LS10550S

Figure 2

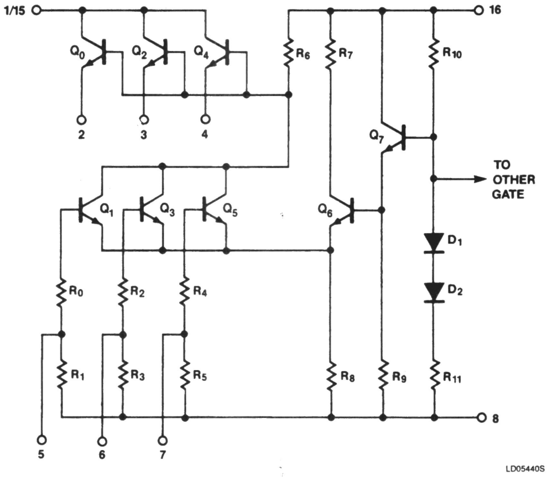
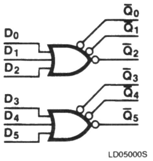

1/15
16
Q0
Q2
Q4
R6
R7
R10
2
3
4
Q7
TO OTHER GATE
Q1
Q3
Q5
Q6
D1
D2
R0
R2
R4
R1
R3
R5
R8
R9
R11
8
5
6
7
LD05440S

Figure 3. Circuit Diagram


D0
D1
D2
Q̄0
Q̄1
Q̄2
D3
D4
D5
Q̄3
Q̄4
Q̄5
LD05000S

$Q_0 = Q_1 = Q_2 = \overline{D_0 + D_1 + D_2}$

$Q_3 = Q_4 = Q_5 = \overline{D_3 + D_4 + D_5}$

**Positive Logic:**

**HIGH state (the more positive voltage) = 1**

**LOW state (the less positive voltage) = 0**

Figure 4. Logic Diagram

## Line Driver

## 10211

**ABSOLUTE MAXIMUM RATINGS** (Operation beyond the limits set forth in this table may impair useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | | 10K ECL | UNIT |
|---|---|---|---|---|
| $V_{EE}$ | Supply voltage | | −8.0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | | 0 to $V_{EE}$ | V |
| $I_O$ | Output source current | | −50 | mA |
| $T_S$ | Storage temperature | | −55 to +150 | °C |
| $T_J$ | Maximum junction temperature | Ceramic package | +165 | °C |
| | | Plastic package | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | 10K ECL | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | −5.2 | | V |
| $V_{IH}$ | HIGH level input voltage | $T_A$ = −30°C | | | −890 | mV |
| | | $T_A$ = +25°C | | | −810 | mV |
| | | $T_A$ = +85°C | | | −700 | mV |
| $V_{IHT}$ | HIGH level input threshold voltage | $T_A$ = −30°C | −1205 | | | mV |
| | | $T_A$ = +25°C | −1105 | | | mV |
| | | $T_A$ = +85°C | −1035 | | | mV |
| $V_{ILT}$ | LOW level input threshold voltage | $T_A$ = −30°C | | | −1500 | mV |
| | | $T_A$ = +25°C | | | −1475 | mV |
| | | $T_A$ = +85°C | | | −1440 | mV |
| $V_{IL}$ | LOW level input voltage | $T_A$ = −30°C | −1890 | | | mV |
| | | $T_A$ = +25°C | −1850 | | | mV |
| | | $T_A$ = +85°C | −1825 | | | mV |
| $T_A$ | Operating ambient temperature | | −30 | +25 | +85 | °C |

**NOTE:**
When operating at $V_{EE}$ other than specified voltage (−5.2V), the DC and AC Characteristics will vary slightly from specified values. (See table of DC Characteristics)

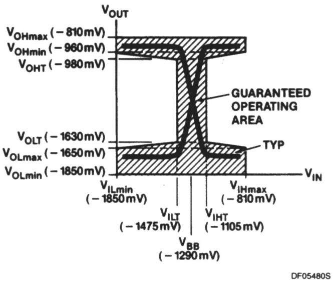
**DC ELECTRICAL CHARACTERISTICS** $V_{CC1} = V_{CC2} = \text{GND}$, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$, output loading with 50Ω to −2.0V ±0.010V unless otherwise specified[1,3]

| PARAMETER | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | $T_A = -30°C$ | −1060 | | −890 | mV | Apply $V_{ILmin}$ to all inputs. |
| | | $T_A = +25°C$ | −960 | | −810 | mV | |
| | | $T_A = +85°C$ | −890 | | −700 | mV | |
| $V_{OHT}$ | HIGH level output threshold voltage | $T_A = -30°C$ | −1080 | | | mV | Apply $V_{ILT}$ to each input, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | $T_A = +25°C$ | −980 | | | mV | |
| | | $T_A = +85°C$ | −910 | | | mV | |
| $V_{OLT}$ | LOW level output threshold voltage | $T_A = -30°C$ | | | −1655 | mV | Apply $V_{IHT}$ to each input, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | $T_A = +25°C$ | | | −1630 | mV | |
| | | $T_A = +85°C$ | | | −1595 | mV | |
| $V_{OL}$ | LOW level output voltage | $T_A = -30°C$ | −1890 | | −1675 | mV | Apply $V_{IHmax}$ to all inputs. |
| | | $T_A = +25°C$ | −1850 | | −1650 | mV | |
| | | $T_A = +85°C$ | −1825 | | −1615 | mV | |
| $I_{IH}$ | HIGH level input current | $T_A = -30°C$ | | | 650 | μA | Apply $V_{IHmax}$ to each input under test, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | $T_A = +25°C$ | | | 410 | μA | |
| | | $T_A = +85°C$ | | | 410 | μA | |
| $I_{IL}$ | LOW level input current | $T_A = -30°C$ | 0.5 | | | μA | Apply $V_{ILmin}$ to each input under test, one at a time, with $V_{IHmax}$ applied to all other inputs. |
| | | $T_A = +25°C$ | 0.5 | | | μA | |
| | | $T_A = +85°C$ | 0.3 | | | μA | |
| $-I_{EE}$ | $V_{EE}$ supply current | $T_A = -30°C$ | | | 42 | mA | |
| | | $T_A = +25°C$ | | 30 | 38 | mA | |
| | | $T_A = +85°C$ | | | 42 | mA | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | $T_A = +25°C$ | | 0.016 | | V/V | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | 0.250 | | V/V | |
| $\frac{\Delta V_{BB}}{\Delta V_{EE}}$ | Reference bias voltage compensation | | | 0.148 | | V/V | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst-case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 5.

## Line Driver 10211



**NOTES:**

$V_{IHmax}$ – Maximum HIGH level input voltage (the most positive $V_{IH}$).
$V_{IHT}$ – HIGH level input threshold voltage.
$V_{ILT}$ – LOW level input threshold voltage.
$V_{ILmin}$ – Minimum LOW level input voltage (the most negative $V_{IL}$).
$V_{OHmax}$ – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition.
$V_{OHmin}$ – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition.
$V_{OHT}$ – HIGH level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLT}$ – LOW level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLmax}$ – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions.
$V_{OLmin}$ – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions.
$V_{BB}$ – Reference bias voltage (the internally generated reference voltage which is used to set the input and output threshold level).

**Figure 5. Transfer Characteristics**

## AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$

| PARAMETER | | $T_A = -30°C$ | | $T_A = +25°C$ | | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Typ | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 1.0 | 2.6 | 1.0 | 1.5 | 2.5 | 1.0 | 2.8 | ns | Figs. 6, 7, 8 |
| $t_{PHL}$ | $D_n$ to $\overline{Q}_n$ | 1.0 | 2.6 | 1.0 | 1.5 | 2.5 | 1.0 | 2.8 | ns | |
| $t_{TLH}$ | Transition time | 1.0 | 2.6 | 1.0 | 1.5 | 2.5 | 1.0 | 2.8 | ns | Figs. 6, 7, 8 |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 1.0 | 2.6 | 1.0 | 1.5 | 2.5 | 1.0 | 2.8 | ns | |

## AC WAVEFORMS

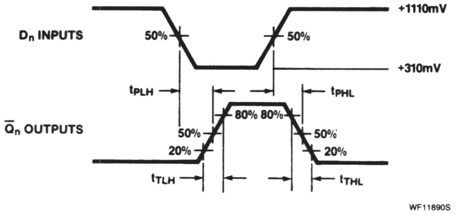
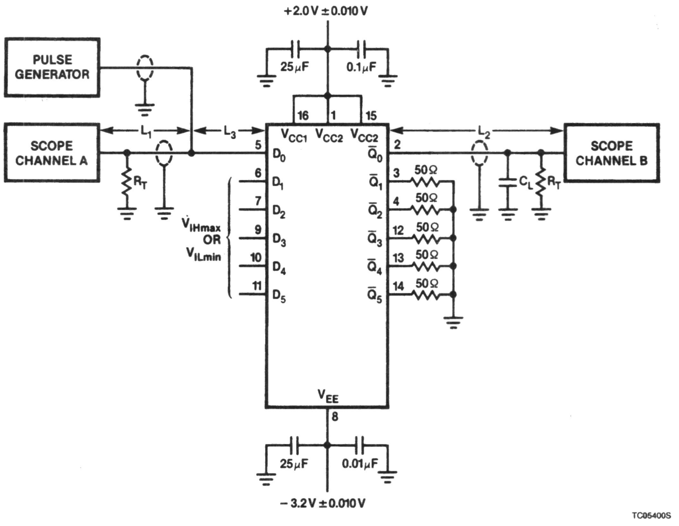


**Figure 6. Propagation Delay and Transition Times for Data to Output**

# Line Driver 10211

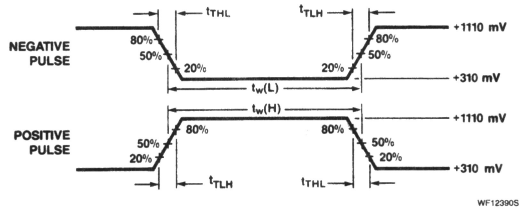
## TEST CIRCUITS AND WAVEFORMS


+2.0V ±0.010V
25µF
0.1µF
PULSE GENERATOR
SCOPE CHANNEL A
L1
L3
16
1
15
VCC1 VCC2 VCC2
5 D0
6 D1
7 D2
9 D3
10 D4
11 D5
RT
VIHmax OR VILmin
2 Q̄0
3 Q̄1
4 Q̄2
12 Q̄3
13 Q̄4
14 Q̄5
50Ω
L2
CL
RT
SCOPE CHANNEL B
VEE
8
25µF
0.01µF
−3.2V ±0.010V
TC05400S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$
2. Decoupling 0.1µF and 25µF from GND to $V_{CC}$, 0.01µF and 25µF from GND to $V_{EE}$. (0.01 and 0.1µF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance ⩽3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ±1% or better.

Figure 7. AC Test Circuit for 10211


NEGATIVE PULSE
POSITIVE PULSE
tTHL
tTLH
80%
50%
20%
tw(L)
tw(H)
+1110 mV
+310 mV
WF12390S

| INPUT PULSE REQUIREMENTS<br>$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$, $V_T$ = GND (0V) | | | | | |
|---|---|---|---|---|---|
| Family | Amplitude | Rep Rate | Pulse Width | $t_{TLH}$ | $t_{THL}$ |
| 10K ECL | 800mVp-p | 1MHz | 500ns | 2.0 ±0.2ns | 2.0 ±0.2ns |

Figure 8. Input Pulse Definition

Signetics

# 10216

# Line Receiver

**Triple Differential OR/NOR Line Receiver (High-Speed)**
***Product Specification***

**ECL Products**

## DESCRIPTION

The 10216 is a high-speed triple differential amplifier for use in sensing differential signals over long lines. The Reference Bias Voltage ($V_{BB}$) is made available at pin 11 to make the device useful as a Schmitt Trigger or in other applications where a stable reference voltage is necessary. Active current sources provide the 10216 with excellent common-mode noise rejection. If any amplifier in a package is not used the input of that amplifier must be tied to $V_{BB}$ (pin 11) to prevent upsetting the current source bias network.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 10216 | 1.5ns | 20mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} = GND$; $V_{EE} = -5.2V$<br>$T_A = -30°C$ to $+85°C$ |
|---|---|
| Plastic DIP | 10216N |
| Ceramic DIP | 10216F |

## PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $\overline{D}_0$, $\overline{D}_2$, $\overline{D}_4$, $D_1$, $D_3$, $D_5$ | Data Inputs |
| $\overline{Q}_0$, $\overline{Q}_2$, $\overline{Q}_4$ | Data Outputs (NOR) |
| $Q_1$, $Q_3$, $Q_5$ | Data Outputs (OR) |
| $V_{BB}$ | Reference Bias Voltage Output |

## PIN CONFIGURATION

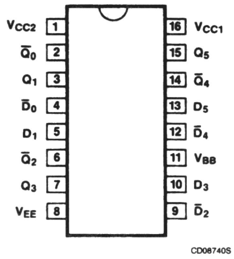

VCC2 1
Q̄0 2
Q1 3
D̄0 4
D1 5
Q̄2 6
Q3 7
VEE 8
16 VCC1
15 Q5
14 Q̄4
13 D5
12 D̄4
11 VBB
10 D3
9 D̄2
CD08740S

Figure 1

## LOGIC SYMBOL

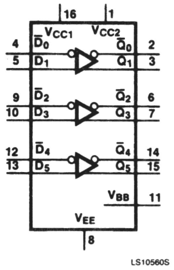

16
1
VCC1
VCC2
4 D̄0
5 D1
Q̄0 2
Q1 3
9 D̄2
10 D3
Q̄2 6
Q3 7
12 D̄4
13 D5
Q̄4 14
Q5 15
VBB 11
VEE
8
LS10560S

Figure 2

## Line Receiver

## 10216

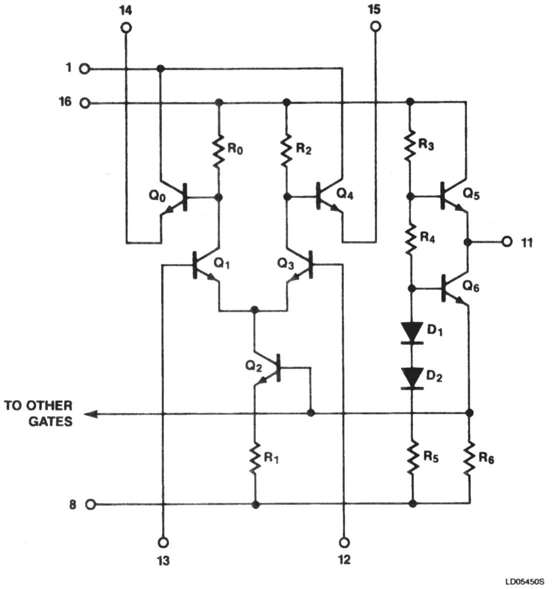
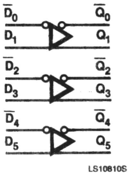

14
15
1
16
R0
R2
R3
Q0
Q4
Q5
R4
11
Q1
Q3
Q6
D1
Q2
D2
TO OTHER GATES
R1
R5
R6
8
13
12
LD05450S

Figure 3. Circuit Diagram (One Amplifier)


$\overline{D}_0$
$\overline{Q}_0$
$D_1$
$Q_1$
$\overline{D}_2$
$\overline{Q}_2$
$D_3$
$Q_3$
$\overline{D}_4$
$\overline{Q}_4$
$D_5$
$Q_5$
LS10810S

$Q_0 = D_0$; $Q_1 = \overline{D}_0$
$Q_2 = D_2$; $Q_3 = \overline{D}_2$
$Q_4 = D_5$; $Q_5 = \overline{D}_4$

**Positive Logic:**
H = HIGH state (the more positive voltage) = 1
L = LOW state (the less positive voltage) = 0

Figure 4. Logic Function

## Line Receiver 10216

**ABSOLUTE MAXIMUM RATINGS** (Operation beyond the limits set forth in this table may impair useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | | 10K ECL | UNIT |
|---|---|---|---|---|
| $V_{EE}$ | Supply voltage | | -8.0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | | 0 to $V_{EE}$ | V |
| $I_O$ | Output current | | -50 | mA |
| $T_S$ | Storage temperature | | -55 to +150 | °C |
| $T_J$ | Maximum junction temperature | Ceramic package | +165 | °C |
| | | Plastic package | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | 10K ECL | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | -5.2 | | V |
| $V_{IH}$ | HIGH level input voltage | $T_A$ = -30°C | | | -890 | mV |
| | | $T_A$ = +25°C | | | -810 | mV |
| | | $T_A$ = +85°C | | | -700 | mV |
| $V_{IHT}$ | HIGH level input threshold voltage | $T_A$ = -30°C | -1205 | | | mV |
| | | $T_A$ = +25°C | -1105 | | | mV |
| | | $T_A$ = +85°C | -1035 | | | mV |
| $V_{ILT}$ | LOW level input threshold voltage | $T_A$ = -30°C | | | -1500 | mV |
| | | $T_A$ = +25°C | | | -1475 | mV |
| | | $T_A$ = +85°C | | | -1440 | mV |
| $V_{IL}$ | LOW level input voltage | $T_A$ = -30°C | -1890 | | | mV |
| | | $T_A$ = +25°C | -1850 | | | mV |
| | | $T_A$ = +85°C | -1825 | | | mV |
| $T_A$ | Operating ambient temperature | | -30 | +25 | +85 | °C |

**NOTE:**
When operating at $V_{EE}$ other than specified voltage (-5.2V), the DC and AC Characteristics will vary slightly from specified values. (See table of DC Characteristics)

## DC OPERATING CONDITIONS FOR COMMON-MODE/REJECTION TEST $V_{CC1} = V_{CC2} = \text{GND}$, $V_{EE} = -5.2\text{V} \pm 0.010\text{V}$

| PARAMETER | | | 10K ECL | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | |
| $V_{IHH}$ | $V_{IHmax}$ + 1.0V | $T_A$ = -30°C | | | +110 | mV |
| | | $T_A$ = +25°C | | | +190 | mV |
| | | $T_A$ = +85°C | | | +300 | mV |
| $V_{IHL}$ | $V_{IHmax}$ - 1.0V | $T_A$ = -30°C | | | -1890 | mV |
| | | $T_A$ = +25°C | | | -1810 | mV |
| | | $T_A$ = +85°C | | | -1700 | mV |
| $V_{ILH}$ | $V_{ILmin}$ + 1.0V | $T_A$ = -30°C | -890 | | | mV |
| | | $T_A$ = +25°C | -850 | | | mV |
| | | $T_A$ = +85°C | -825 | | | mV |
| $V_{ILL}$ | $V_{ILmin}$ - 1.0V | $T_A$ = -30°C | -2890 | | | mV |
| | | $T_A$ = +25°C | -2850 | | | mV |
| | | $T_A$ = +85°C | -2825 | | | mV |

**NOTE:**
When operating at $V_{EE}$ other than specified voltage (-5.2V), the DC and AC Characteristics will vary slightly from specified values. (See table of DC Characteristics)

# Line Receiver 10216

**DC ELECTRICAL CHARACTERISTICS** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$, output loading with 50Ω to −2.0V ±0.010V unless otherwise specified[1,3]

| PARAMETER | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | $T_A = -30°C$ | −1060 | | −890 | mV | For $Q_n$ outputs, apply $V_{ILmin}$ to each inverting input, one at a time, with $V_{BB}$ applied to all non-inverting inputs and with $V_{IHmax}$ applied to all other inverting inputs.<br>For $\overline{Q}_n$ outputs, apply $V_{IHmax}$ to each inverting input one at a time, with $V_{ILmin}$ applied to all other inverting inputs and $V_{BB}$ applied to all non-inverting inputs.<br>(Refer to Fig. 8) |
| | | $T_A = +25°C$ | −960 | | −810 | mV | |
| | | $T_A = +85°C$ | −890 | | −700 | mV | |
| $V_{OHT}$ | HIGH level output threshold voltage | $T_A = -30°C$ | −1080 | | | mV | For $Q_n$ outputs, apply $V_{ILT}$ to each inverting input, one at a time, with $V_{BB}$ applied to all non-inverting inputs and with $V_{IHmax}$ applied to all other inverting inputs.<br>For $\overline{Q}_n$ outputs, apply $V_{IHT}$ to each inverting input, one at a time, with $V_{ILmin}$ applied to all other inverting inputs and $V_{BB}$ applied to all non-inverting inputs.<br>(Refer to Fig. 8) |
| | | $T_A = +25°C$ | −980 | | | mV | |
| | | $T_A = +85°C$ | −910 | | | mV | |
| $V_{OLT}$ | LOW level output threshold voltage | $T_A = -30°C$ | | | −1655 | mV | For $Q_n$ outputs, apply $V_{IHT}$ to each inverting input, one at a time, with $V_{BB}$ applied to all non-inverting inputs and $V_{ILmin}$ applied to all other inverting inputs.<br>For $\overline{Q}_n$ outputs, apply $V_{ILT}$ to each inverting input, one at a time, with $V_{BB}$ applied to all non-inverting inputs and $V_{IHmax}$ applied to all other inverting inputs.<br>(Refer to Fig. 8) |
| | | $T_A = +25°C$ | | | −1630 | mV | |
| | | $T_A = +85°C$ | | | −1595 | mV | |
| $V_{OL}$ | LOW level output voltage | $T_A = -30°C$ | −1890 | | −1675 | mV | For $Q_n$ outputs, apply $V_{IHmax}$ to each inverting input, one at a time, with $V_{BB}$ applied to all non-inverting inputs and $V_{ILmin}$ applied to all other inverting inputs.<br>For $\overline{Q}_n$ outputs, apply $V_{ILmin}$ to each inverting input, one at a time, with $V_{BB}$ applied to all non-inverting and $V_{IHmax}$ applied to all other inverting inputs.<br>(Refer to Fig. 8) |
| | | $T_A = +25°C$ | −1850 | | −1650 | mV | |
| | | $T_A = +85°C$ | −1825 | | −1615 | mV | |
| $I_{IH}$ | HIGH level input current | $T_A = -30°C$ | | | 180 | μA | Apply $V_{IHmax}$ to each inverting input under test one at a time, with $V_{ILmin}$ applied to all other inverting inputs and $V_{BB}$ applied to all non-inverting inputs.<br>Apply $V_{IHmax}$ to each non-inverting input under test, one at a time, with $V_{ILmin}$ applied to all other non-inverting inputs and $V_{BB}$ applied to all inverting inputs.<br>(Refer to Fig. 8) |
| | | $T_A = +25°C$ | | | 115 | μA | |
| | | $T_A = +85°C$ | | | 115 | μA | |
| $-I_{EE}$ | $V_{EE}$ supply current | $T_A = -30°C$ | | | 27 | mA | Apply $V_{ILmin}$ to all inverting inputs.<br>Apply $V_{BB}$ to all non-inverting inputs. |
| | | $T_A = +25°C$ | | 20 | 25 | mA | |
| | | $T_A = +85°C$ | | | 27 | mA | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | $T_A = +25°C$ | | 0.016 | | V/V | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | 0.250 | | V/V | |
| $\frac{\Delta V_{BB}}{\Delta V_{EE}}$ | Reference bias voltage compensation | | | 0.148 | | V/V | |

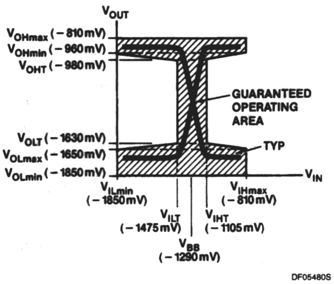
# Line Receiver 10216

## DC ELECTRICAL CHARACTERISTICS (Continued)

| PARAMETER | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] |
|---|---|---|---|---|---|---|---|
| $V_{BB}$ | Reference voltage | $T_A = -30°C$ | −1420 | | −1280 | mV | All inverting or all non-inverting input pins are tied to the $V_{BB}$ pin during measurement. |
| | | $T_A = +25°C$ | −1350 | −1290 | −1230 | mV | |
| | | $T_A = +85°C$ | −1295 | | −1150 | mV | |
| $V_{OH}$ | HIGH level output voltage for common mode rejection test | $T_A = -30°C$ | −1060 | | −890 | mV | For $\overline{Q}_n$ outputs, apply $V_{IHH}$ to inverting inputs and $V_{ILH}$ to non-inverting inputs.<br>For $Q_n$ outputs, apply $V_{ILL}$ to inverting inputs and $V_{IHL}$ to non-inverting inputs. |
| | | $T_A = +25°C$ | −960 | | −810 | mV | |
| | | $T_A = +85°C$ | −890 | | −700 | mV | |
| $V_{OL}$ | LOW level output voltage for common mode rejection test | $T_A = -30°C$ | −1890 | | −1675 | mV | For $\overline{Q}_n$ outputs, apply $V_{ILH}$ to inverting inputs and $V_{IHH}$ to non-inverting inputs.<br>For $Q_n$ outputs, apply $V_{IHL}$ to inverting inputs and $V_{ILL}$ to non-inverting inputs. |
| | | $T_A = +25°C$ | −1850 | | −1650 | mV | |
| | | $T_A = +85°C$ | −1825 | | −1615 | mV | |
| $-I_{CBO}$ | Input leakage current | $T_A = -30°C$ | | | 1.5 | µA | Apply $V_{EE}$ to each inverting input under test, one at a time, with $V_{ILmin}$ applied to all other inverting inputs and $V_{BB}$ applied to all non-inverting inputs. (Refer to Fig. 8) |
| | | $T_A = +25°C$ | | | 1.0 | µA | |
| | | $T_A = +85°C$ | | | 1.0 | µA | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst-case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 5.


$V_{OUT}$
$V_{OHmax}$ (−810mV)
$V_{OHmin}$ (−960mV)
$V_{OHT}$ (−980mV)
GUARANTEED OPERATING AREA
$V_{OLT}$ (−1630mV)
$V_{OLmax}$ (−1650mV)
$V_{OLmin}$ (−1850mV)
TYP
$V_{IN}$
$V_{ILmin}$ (−1850mV)
$V_{IHmax}$ (−810mV)
$V_{ILT}$ (−1475mV)
$V_{IHT}$ (−1105mV)
$V_{BB}$ (−1290mV)
DF05480S

**NOTES:**

$V_{IHmax}$ – Maximum HIGH level input voltage (the most positive $V_{IH}$).
$V_{IHT}$ – HIGH level input threshold voltage.
$V_{ILT}$ – LOW level input threshold voltage.
$V_{ILmin}$ – Minimum LOW level input voltage (the most negative $V_{IL}$).
$V_{OHmax}$ – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition.
$V_{OHmin}$ – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition.
$V_{OHT}$ – HIGH level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLT}$ – LOW level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLmax}$ – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions.
$V_{OLmin}$ – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions.
$V_{BB}$ – Reference bias voltage (the internally generated reference voltage which is used to set the input and output threshold level).

**Figure 5. Transfer Characteristics**

## AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$

| PARAMETER | $T_A = -30°C$ | | $T_A = +25°C$ | | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Typ | Max | Min | Max | | |
| $t_{PLH}$ Propagation delay | 1.0 | 2.6 | 1.0 | 1.5 | 2.5 | 1.0 | 2.8 | ns | Figs. 6, 7, 9 |
| $t_{PHL}$ $D_n$, $\overline{D}_n$ to $Q_n$, $\overline{Q}_n$ | 1.0 | 2.6 | 1.0 | 1.5 | 2.5 | 1.0 | 2.8 | ns | |
| $t_{TLH}$ Transition time | 1.0 | 2.6 | 1.0 | 1.5 | 2.5 | 1.0 | 2.8 | ns | Figs. 6, 7, 9 |
| $t_{THL}$ 20% to 80%, 80% to 20% | 1.0 | 2.6 | 1.0 | 1.5 | 2.5 | 1.0 | 2.8 | ns | |

## AC WAVEFORMS

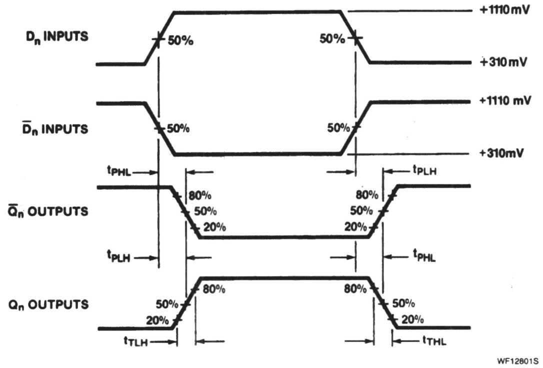

$D_n$ INPUTS
50%
50%
+1110mV
+310mV
$\overline{D}_n$ INPUTS
50%
50%
+1110 mV
+310mV
$t_{PHL}$
$t_{PLH}$
$\overline{Q}_n$ OUTPUTS
80%
50%
20%
80%
50%
20%
$t_{PLH}$
$t_{PHL}$
$Q_n$ OUTPUTS
80%
50%
20%
80%
50%
20%
$t_{TLH}$
$t_{THL}$
WF12801S

**Figure 6. Propagation Delay and Transition Times for Data to Output**

## TEST CIRCUITS AND WAVEFORMS

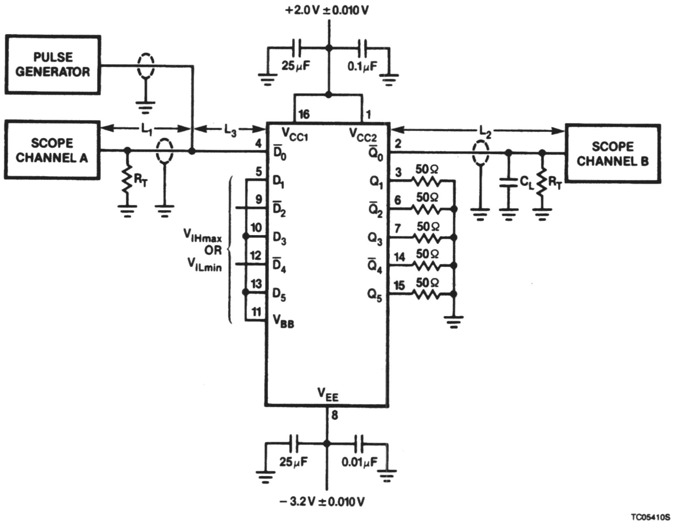

+2.0V ±0.010V
25μF
0.1μF
PULSE GENERATOR
SCOPE CHANNEL A
L1
L3
L2
RT
16
1
VCC1
VCC2
4 D̄0
2 Q̄0
5 D1
Q1
9 D̄2
Q̄2
10 D3
Q3
12 D̄4
Q̄4
13 D5
Q5
11 VBB
3
6
7
14
15
50Ω
VIHmax OR VILmin
CL
SCOPE CHANNEL B
VEE
8
25μF
0.01μF
-3.2V ±0.010V
TC05410S

Figure 7. AC Test Circuit for 10216

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$
2. Decoupling 0.1μF and 25μF from GND to $V_{CC}$, 0.01μF and 25μF from GND to $V_{EE}$. (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance ≤ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ±1% or better.

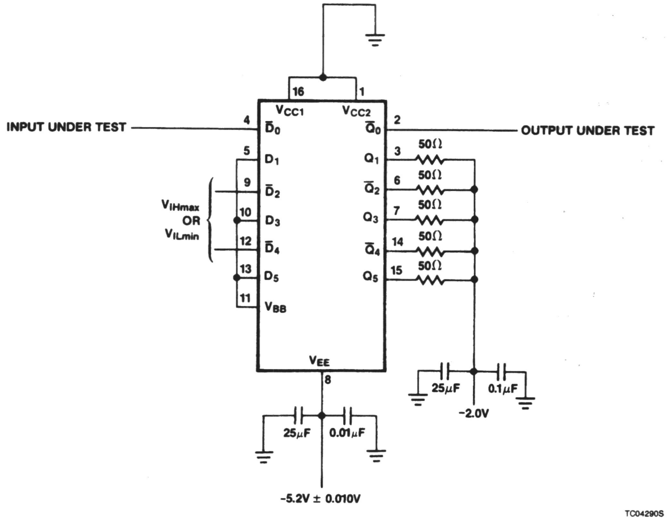
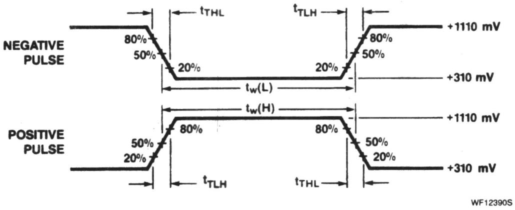

INPUT UNDER TEST
OUTPUT UNDER TEST
16
1
VCC1
VCC2
4 D̄0
2 Q̄0
5 D1
3 Q1
9 D̄2
6 Q̄2
10 D3
7 Q3
12 D̄4
14 Q̄4
13 D5
15 Q5
11 VBB
50Ω
VIHmax OR VILmin
VEE
8
25μF
0.01μF
-5.2V ± 0.010V
25μF
0.1μF
-2.0V
TC04290S

Figure 8. DC Test Circuit for 10216

**NOTES:**

1. $V_{CC1} = V_{CC2}$ = GND (0V), $V_{EE} = -5.2V \pm 0.010V$, $V_T = -2.0V \pm 0.010V$.
2. Decoupling 0.1μF and 25μF from GND to $V_T$, 0.01μF and 25μF from GND to $V_{EE}$ (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than ¼ inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded identically to output under test, substituting a 50Ω termination for the Scope.

# Line Receiver 10216


NEGATIVE PULSE
POSITIVE PULSE
$t_{THL}$
$t_{TLH}$
80%
50%
20%
$t_w(L)$
$t_w(H)$
+1110 mV
+310 mV
WF12390S

| INPUT PULSE REQUIREMENTS<br>$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$, $V_T = GND$ (0V) | | | | | |
|---|---|---|---|---|---|
| **Family** | **Amplitude** | **Rep Rate** | **Pulse Width** | $t_{TLH}$ | $t_{THL}$ |
| 10K ECL | 800mVp-p | 1MHz | 500ns | 2.0 ±0.2ns | 2.0 ±0.2ns |

**Figure 9. Input Pulse Definition**

# 10231
## Flip-Flop

**Dual D-Type Master-Slave Flip-Flop (High-Speed)**
***Product Specification***

## DESCRIPTION

The 10231 is a High-Speed Dual D-type Master-Slave Flip-Flop. It contains Asynchronous Set (S) and Reset (R) which override Clock (CP) and Clock Enable ($\overline{CE}_n$) inputs. Each flip-flop may be clocked separately by using the enable inputs for the clocking function and holding the Clock in the LOW state. For the two flip-flops to be clocked, the Clock must be used with the Clock Enable inputs held in the LOW state.

The outputs of the 10231 change state with the positive transition of the Clock. Due to the master-slave structure of the device, a change in the information present at the data (D) input will not modify the output information at any other time. All unused inputs must be tied to $V_{IL}$ or $V_{EE}$.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 10231 | 2.0ns | 52mA |

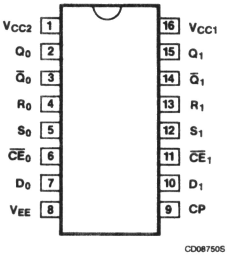
## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} = GND$; $V_{EE} = -5.2V$<br>$T_A = -30°C$ to $+85°C$ |
|---|---|
| Plastic DIP | 10231N |
| Ceramic DIP | 10231F |

## PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_0$, $D_1$ | Data Inputs |
| CP | Clock Input |
| $\overline{CE}_0$, $\overline{CE}_1$ | Clock Enable Inputs |
| $S_0$, $S_1$ | Set Inputs |
| $R_0$, $R_1$ | Reset Inputs |
| $Q_0$, $Q_1$, $\overline{Q}_0$, $\overline{Q}_1$ | Data Outputs |

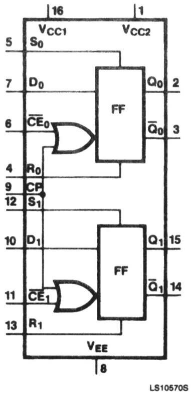
## PIN CONFIGURATION



VCC2 1
Q0 2
Q̄0 3
R0 4
S0 5
C̄Ē0 6
D0 7
VEE 8
16 VCC1
15 Q1
14 Q̄1
13 R1
12 S1
11 C̄Ē1
10 D1
9 CP
CD08750S

Figure 1

## LOGIC SYMBOL

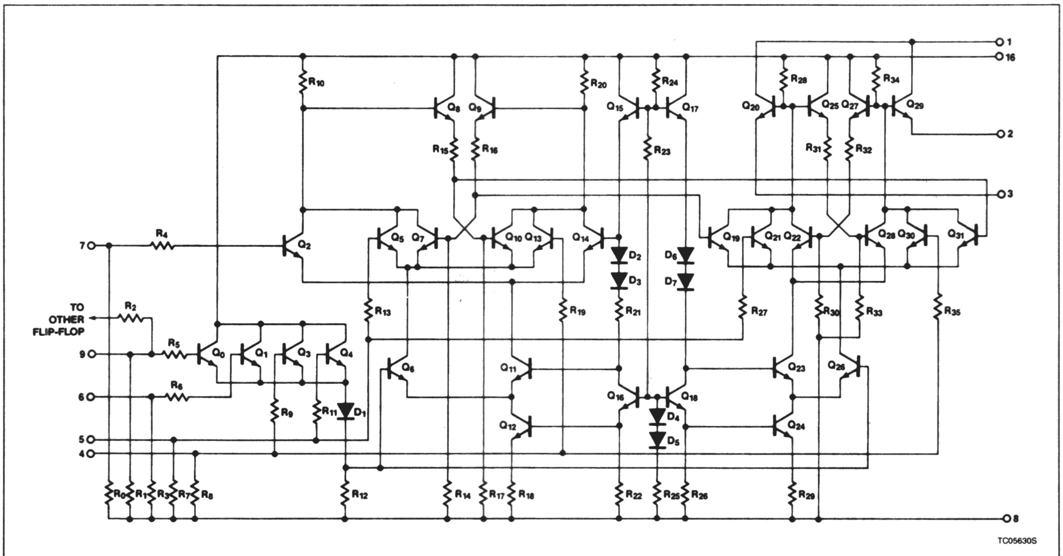


16
1
VCC1
VCC2
5 S0
7 D0
FF
Q0 2
6 C̄Ē0
Q̄0 3
4 R0
9 CP
12 S1
10 D1
FF
Q1 15
11 C̄Ē1
Q̄1 14
13 R1
VEE
8
LS10570S

Figure 2

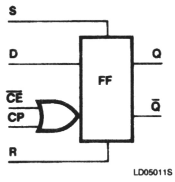
## Flip-Flop

## 10231



1
16
2
3
7
TO OTHER FLIP-FLOP
9
6
5
4
8
R0 R1 R2 R3 R4 R5 R6 R7 R8 R9 R10 R11 R12 R13 R14 R15 R16 R17 R18 R19 R20 R21 R22 R23 R24 R25 R26 R27 R28 R29 R30 R31 R32 R33 R34 R35
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8 Q9 Q10 Q11 Q12 Q13 Q14 Q15 Q16 Q17 Q18 Q19 Q20 Q21 Q22 Q23 Q24 Q25 Q26 Q27 Q28 Q29 Q30 Q31
D1 D2 D3 D4 D5 D6 D7
TC05630S

**Figure 3. Circuit Diagram (One Flip-Flop)**



S
D
CE
CP
R
FF
Q
Q̄
LD05011S

**Figure 4. Logic Function**

### FUNCTION TABLES

### SYNCHRONOUS OPERATION

| $D_n$ | $C_P$ | $\overline{C}_E$* | $Q_{n+1}$** |
|---|---|---|---|
| L | L | L | $Q_n$ |
| L | L | H | $Q_n$ |
| L | H | L | L |
| L | H | H | $Q_n$ |
| H | L | L | $Q_n$ |
| H | L | H | $Q_n$ |
| H | H | L | H |
| H | H | H | $Q_n$ |

*Conditions for CP and $\overline{CE}$ may be interchanged. In this table $\overline{CE}$ is static, while for CP and H represent a transition from LOW to HIGH between $t_n$ and $t_{n+1}$.
**R and S = LOW.

### ASYNCHRONOUS OPERATION

| INPUTS | | OUTPUT |
|---|---|---|
| R | S | $Q_{n+1}$ |
| L | L | $Q_n$ |
| L | H | H |
| H | L | L |
| H | H | N |

Positive Logic:
H = HIGH state = 1
L = LOW state = 0
X = Don't Care
N = Not allowed

# Flip-Flop

# 10231

**ABSOLUTE MAXIMUM RATINGS** (Operation beyond the limits set forth in this table may impair useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | | 10K ECL | UNIT |
|---|---|---|---|---|
| $V_{EE}$ | Supply voltage | | -8.0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | | 0 to $V_{EE}$ | V |
| $I_O$ | Output source current | | -50 | mA |
| $T_S$ | Storage temperature | | -55 to +150 | °C |
| $T_J$ | Maximum junction temperature | Ceramic package | +165 | °C |
| | | Plastic package | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | 10K ECL | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | -5.2 | | V |
| $V_{IH}$ | HIGH level input voltage | $T_A$ = -30°C | | | -890 | mV |
| | | $T_A$ = +25°C | | | -810 | mV |
| | | $T_A$ = +85°C | | | -700 | mV |
| $V_{IHT}$ | HIGH level input threshold voltage | $T_A$ = -30°C | -1205 | | | mV |
| | | $T_A$ = +25°C | -1105 | | | mV |
| | | $T_A$ = +85°C | -1035 | | | mV |
| $V_{ILT}$ | LOW level input threshold voltage | $T_A$ = -30°C | | | -1500 | mV |
| | | $T_A$ = +25°C | | | -1475 | mV |
| | | $T_A$ = +85°C | | | -1440 | mV |
| $V_{IL}$ | LOW level input voltage | $T_A$ = -30°C | -1890 | | | mV |
| | | $T_A$ = +25°C | -1850 | | | mV |
| | | $T_A$ = +85°C | -1825 | | | mV |
| $T_A$ | Operating ambient temperature | | -30 | +25 | +85 | °C |

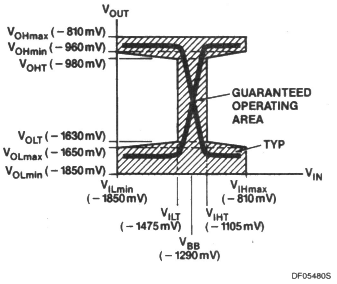
**NOTE:**
When operating at $V_{EE}$ other than specified voltage (-5.2V), the DC and AC Characteristics will vary slightly from specified values. (See table of DC Characteristics)

## DC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$, output loading with 50Ω to −2.0V ±0.010V unless otherwise specified.[1,3]

| PARAMETER | | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | | $T_A = -30°C$ | −1060 | | −890 | mV | For Q outputs, apply $V_{IHmax}$ to $S_n$ inputs with $V_{ILmin}$ applied to all other inputs. For $\overline{Q}$ outputs, apply $V_{IHmax}$ to $R_n$ inputs with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | −960 | | −810 | mV | |
| | | | $T_A = +85°C$ | −890 | | −700 | mV | |
| $V_{OHT}$ | HIGH level output threshold voltage | | $T_A = -30°C$ | −1080 | | | mV | For Q outputs, apply $V_{IHT}$ to $S_n$ inputs, with $V_{ILmin}$ applied to all other inputs. For $\overline{Q}$ outputs, apply $V_{IHT}$ to $R_n$ inputs, with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | −980 | | | mV | |
| | | | $T_A = +85°C$ | −910 | | | mV | |
| $V_{OLT}$ | LOW level output threshold voltage | | $T_A = -30°C$ | | | −1655 | mV | For Q outputs, apply $V_{IHT}$ to $R_n$ inputs, with $V_{ILmin}$ applied to all other inputs. For $\overline{Q}$ outputs, apply $V_{IHT}$ to $S_n$ inputs with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | | | −1630 | mV | |
| | | | $T_A = +85°C$ | | | −1595 | mV | |
| $V_{OL}$ | LOW level output voltage | | $T_A = -30°C$ | −1890 | | −1675 | mV | For Q outputs, apply $V_{IHmax}$ to $R_n$ inputs, with $V_{ILmin}$ applied to all other inputs. For $\overline{Q}$ outputs, apply $V_{IHmax}$ to $S_n$ inputs with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | −1850 | | −1650 | mV | |
| | | | $T_A = +85°C$ | −1825 | | −1615 | mV | |
| $I_{IH}$ | HIGH level input current | $D_n$, $\overline{CE}_n$ inputs | $T_A = -30°C$ | | | 350 | µA | Apply $V_{IHmax}$ to each input under test, one at a time, with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | | | 220 | µA | |
| | | | $T_A = +85°C$ | | | 220 | µA | |
| | | $R_n$, $S_n$ inputs | $T_A = -30°C$ | | | 650 | µA | |
| | | | $T_A = +25°C$ | | | 410 | µA | |
| | | | $T_A = +85°C$ | | | 410 | µA | |
| | | CP input | $T_A = -30°C$ | | | 460 | µA | Apply $V_{IHmax}$ to CP input with $V_{ILmin}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | | | 290 | µA | |
| | | | $T_A = +85°C$ | | | 290 | µA | |
| $I_{IL}$ | LOW level input current | | $T_A = -30°C$ | 0.5 | | | µA | Apply $V_{ILmin}$ to each input under test, one at a time, with $V_{IHmax}$ applied to all other inputs. |
| | | | $T_A = +25°C$ | 0.5 | | | µA | |
| | | | $T_A = +85°C$ | 0.3 | | | µA | |
| $-I_{EE}$ | $V_{EE}$ supply current | | $T_A = -30°C$ | | | 72 | mA | |
| | | | $T_A = +25°C$ | | 52 | 65 | mA | |
| | | | $T_A = +85°C$ | | | 72 | mA | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | | $T_A = +25°C$ | | 0.016 | | V/V | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | | 0.250 | | V/V | |
| $\frac{\Delta V_{BB}}{\Delta V_{EE}}$ | Reference bias voltage compensation | | | | 0.148 | | V/V | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst-case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 5.



**NOTES:**

| | |
|---|---|
| $V_{IHmax}$ | − Maximum HIGH level input voltage (the most positive $V_{IH}$). |
| $V_{IHT}$ | − HIGH level input threshold voltage. |
| $V_{ILT}$ | − LOW level input threshold voltage. |
| $V_{ILmin}$ | − Minimum LOW level input voltage (the most negative $V_{IL}$). |
| $V_{OHmax}$ | − Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition. |
| $V_{OHmin}$ | − Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition. |
| $V_{OHT}$ | − HIGH level output threshold voltage with the inputs set to their respective threshold levels. |
| $V_{OLT}$ | − LOW level output threshold voltage with the inputs set to their respective threshold levels. |
| $V_{OLmax}$ | − Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions. |
| $V_{OLmin}$ | − Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions. |
| $V_{BB}$ | − Reference bias voltage (the internally generated reference voltage which is used to set the input and output threshold level). |

Figure 5. Transfer Characteristics

## AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$

| | PARAMETER | $T_A = -30°C$ | | $T_A = +25°C$ | | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Typ | Max | Min | Max | | |
| $f_{MAX}$ | Maximum clock frequency | 200 | | 200 | 225 | | 200 | | MHz | Figs. 7, 10, 11 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>CP to $Q_n$, $\overline{Q}_n$ | 1.5<br>1.5 | 3.4<br>3.4 | 1.5<br>1.5 | 2.0<br>2.0 | 3.3<br>3.3 | 1.6<br>1.6 | 3.7<br>3.7 | ns<br>ns | Figs. 6, 9, 11 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$S_n$, $R_n$ to $Q_n$, $\overline{Q}_n$ | 1.1<br>1.1 | 3.4<br>3.4 | 1.1<br>1.1 | 2.0<br>2.0 | 3.3<br>3.3 | 1.2<br>1.2 | 3.7<br>3.7 | ns<br>ns | |
| $t_s$ | Setup time $D_n$ to CP | 1.5 | | 1.0 | | | 1.5 | | ns | Figs. 8, 9, 11 |
| $t_h$ | Hold time CP to $D_n$ | 0.9 | | 0.75 | | | 0.9 | | ns | |
| $t_{TLH}$<br>$t_{THL}$ | Transition time<br>20% to 80%, 80% to 20% | 0.9<br>0.9 | 3.3<br>3.3 | 1.0<br>1.0 | 1.3<br>1.3 | 3.1<br>3.1 | 1.0<br>1.0 | 3.6<br>3.6 | ns<br>ns | Figs. 6, 9, 11 |

## AC WAVEFORMS

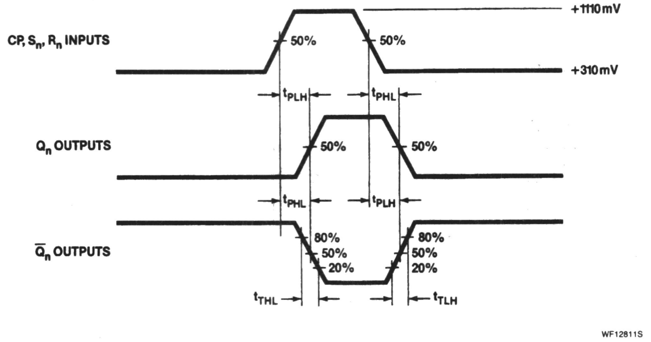

CP, $S_n$, $R_n$ INPUTS
$Q_n$ OUTPUTS
$\overline{Q}_n$ OUTPUTS
+1110mV
+310mV
50%
50%
$t_{PLH}$
$t_{PHL}$
50%
50%
$t_{PHL}$
$t_{PLH}$
80%
50%
20%
80%
50%
20%
$t_{THL}$
$t_{TLH}$
WF12811S

Figure 6. Propagation and Transition Times, CP, $S_n$, $R_n$ Inputs to Outputs

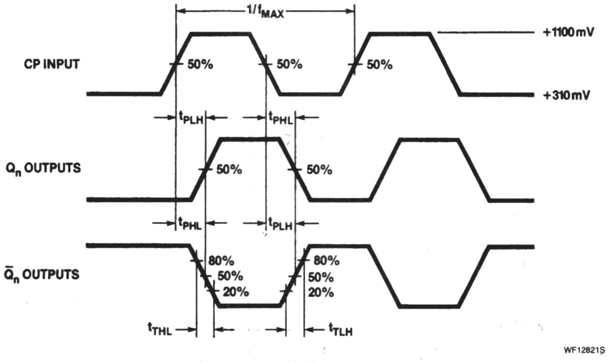

$1/f_{MAX}$
CP INPUT
$Q_n$ OUTPUTS
$\overline{Q}_n$ OUTPUTS
+1100mV
+310mV
50%
50%
50%
$t_{PLH}$
$t_{PHL}$
50%
50%
$t_{PHL}$
$t_{PLH}$
80%
50%
20%
80%
50%
20%
$t_{THL}$
$t_{TLH}$
WF12821S

Figure 7. Maximum Clock Frequency

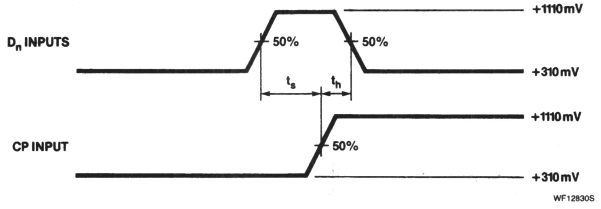
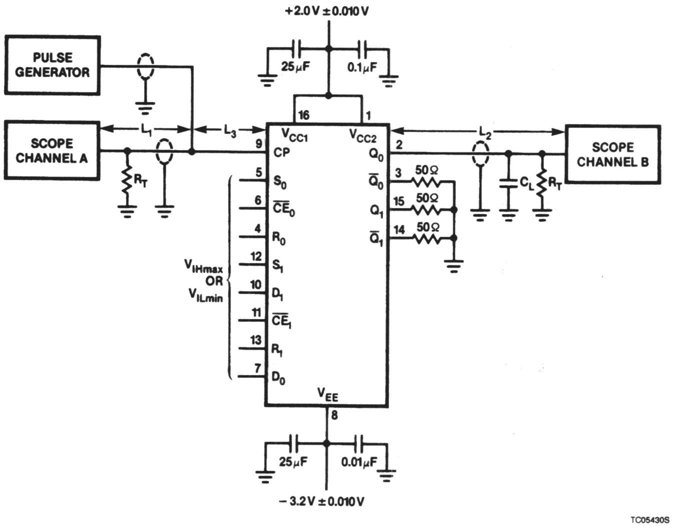

$D_n$ INPUTS
CP INPUT
+1110mV
+310mV
50%
50%
$t_s$
$t_h$
+1110mV
50%
+310mV
WF12830S

Figure 8. Setup and Hold Times for Data to Clock

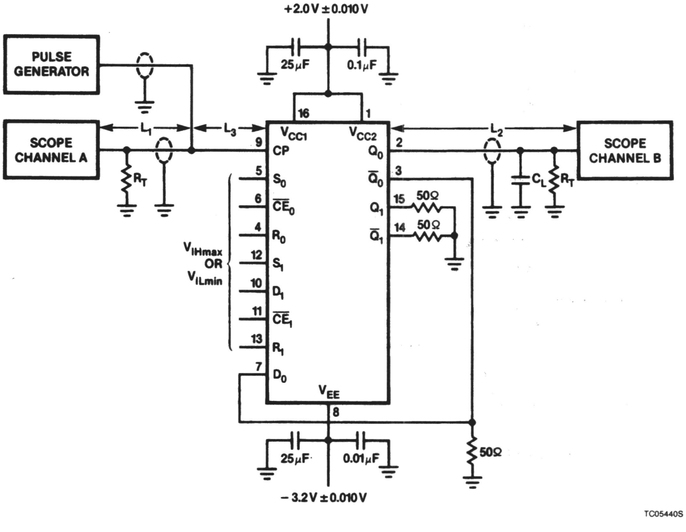
## TEST CIRCUITS AND WAVEFORMS


+2.0V ±0.010V
25μF
0.1μF
PULSE GENERATOR
SCOPE CHANNEL A
L1
L3
L2
RT
16
1
9
VCC1
VCC2
CP
Q0
2
SCOPE CHANNEL B
CL
RT
5 S0
3 50Ω
6 CE0
15 50Ω
Q1
4 R0
14 50Ω
VIHmax OR VILmin
12 S1
10 D1
11 CE1
13 R1
7 D0
VEE
8
25μF
0.01μF
−3.2V ±0.010V
TC05430S

NOTES:

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1μF and 25μF from GND to $V_{CC}$, 0.01μF and 25μF from GND to $V_{EE}$. (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance ≤ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.

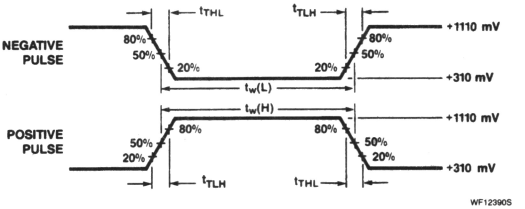
Figure 9. AC Test Circuit for 10231


+2.0V ±0.010V
25μF
0.1μF
PULSE GENERATOR
SCOPE CHANNEL A
L1
L3
L2
RT
16
1
9
VCC1
VCC2
CP
Q0
2
SCOPE CHANNEL B
CL
RT
5 S0
3
6 CE0
15 50Ω
Q1
4 R0
14 50Ω
VIHmax OR VILmin
12 S1
10 D1
11 CE1
13 R1
7 D0
VEE
8
25μF
0.01μF
50Ω
−3.2V ±0.010V
TC05440S

NOTES:

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1μF and 25μF from GND to $V_{CC}$, 0.01μF and 25μF from GND to $V_{EE}$. (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance ≤ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.

Figure 10. AC Test Circuit for 10231 (Clock Frequency)


NEGATIVE PULSE
POSITIVE PULSE
80%
50%
20%
$t_{THL}$
$t_{TLH}$
$t_w(L)$
$t_w(H)$
+1110 mV
+310 mV
WF12390S

| INPUT PULSE REQUIREMENTS<br>$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$, $V_T$ = GND (0V) | | | | | |
|---|---|---|---|---|---|
| **Family** | **Amplitude** | **Rep Rate** | **Pulse Width** | $t_{TLH}$ | $t_{THL}$ |
| 10K ECL | 800mVp-p | 1MHz | 500ns | 2.0 ±0.2ns | 2.0 ±0.2ns |

**Figure 11. Input Pulse Definition**

**Signetics**

# Section 7
# 100K Series Data Sheets

**ECL Products**

## INDEX

| | | |
|---|---|---|
| **100101** | Triple 5-Input OR/NOR Gate | 7-3 |
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| **100112** | Quad Driver | 7-21 |
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| **100141** | 8-Bit Shift Register | 7-105 |
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| **100151** | Hex D-Type Master-Slave Flip-Flop | 7-132 |
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| **100181** | 4-Bit Binary/BCD ALU | 7-230 |
| **100231** | Triple D-Type Master-Slave Flip-Flop (High-Speed Version of 100131) | 7-241 |
| **100255** | Quint Bidirectional 100 K-to-TTL Translator | 7-252 |

7

Signetics

# 100101
## Gate

**Triple 5-Input OR/NOR Gate**
***Product Specification***

**ECL Products**

## DESCRIPTION

100101 is a triple 5-input OR/NOR gate. Each gate has an OR and a NOR output.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT $(-I_{EE})$ |
|---|---|---|
| 100101 | 0.75ns | 27mA |

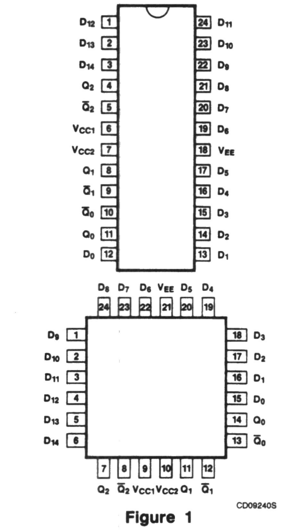
## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} = GND$; $V_{EE} = -4.2V$ to $-4.8V$<br>$T_A = 0°C$ to $+85°C$ |
|---|---|
| Ceramic DIP | 100101F |
| Ceramic Flat Pack | 100101Y |

## PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_0 - D_{14}$ | Data Inputs |
| $Q_0 - Q_2$ | Data Outputs (OR) |
| $\overline{Q}_0 - \overline{Q}_2$ | Data Outputs (NOR) |

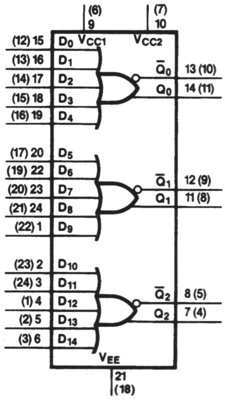
## PIN CONFIGURATION


D12 1
D13 2
D14 3
Q2 4
Q̄2 5
VCC1 6
VCC2 7
Q1 8
Q̄1 9
Q̄0 10
Q0 11
D0 12
24 D11
23 D10
22 D9
21 D8
20 D7
19 D6
18 VEE
17 D5
16 D4
15 D3
14 D2
13 D1
D8 D7 D6 VEE D5 D4
24 23 22 21 20 19
D9 1
D10 2
D11 3
D12 4
D13 5
D14 6
18 D3
17 D2
16 D1
15 D0
14 Q0
13 Q̄0
7 8 9 10 11 12
Q2 Q̄2 VCC1 VCC2 Q1 Q̄1

CD09240S

Figure 1

## LOGIC SYMBOL


(6) 9
(7) 10
VCC1
VCC2
(12) 15 D0
(13) 16 D1
(14) 17 D2
(15) 18 D3
(16) 19 D4
Q̄0 13 (10)
Q0 14 (11)
(17) 20 D5
(19) 22 D6
(20) 23 D7
(21) 24 D8
(22) 1 D9
Q̄1 12 (9)
Q1 11 (8)
(23) 2 D10
(24) 3 D11
(1) 4 D12
(2) 5 D13
(3) 6 D14
Q̄2 8 (5)
Q2 7 (4)
VEE
21 (18)

LS10700S

Figure 2

# Gate 100101

## FUNCTION TABLE (One Gate)

| INPUTS | | | | | OUTPUTS | |
|---|---|---|---|---|---|---|
| $D_0$ | $D_1$ | $D_2$ | $D_3$ | $D_4$ | $\overline{Q}_0$ | $Q_0$ |
| L | L | L | L | L | H | L |
| H | X | X | X | X | L | H |
| X | H | X | X | X | L | H |
| X | X | H | X | X | L | H |
| X | X | X | H | X | L | H |
| X | X | X | X | H | L | H |

Positive Logic:
H = HIGH state (more positive voltage level) = 1
L = LOW state (less positive voltage) = 0
X = Don't Care

## ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | 100K ECL | UNIT |
|---|---|---|---|
| $V_{EE}$ | Supply voltage ($V_{CC1} = V_{CC2} = GND$) | -7.0 to 0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | $V_{EE}$ to +0.5 | V |
| $I_O$ | Output current | -55 | mA |
| $T_S$ | Storage temperature | -65 to +150 | °C |
| $T_J$ | Maximum junction temperature | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | | 100K ECL | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | -4.2 | -4.5 | -4.8 | V |
| $V_{EE}$ | Supply voltage (negative) when operating with 10K ECL family | | | | | -5.7 | V |
| $V_{IH}$ | HIGH level input voltage | $V_{CC1} = V_{CC2} = GND$<br>$T_A = 0°C$ to $+85°C$ | $V_{EE} = -4.2V$ | -1150 | | -880 | mV |
| | | | $V_{EE} = -4.5V$ | -1165 | | | |
| | | | $V_{EE} = -4.8V$ | | | | |
| $V_{IHT}$ | HIGH level input threshold voltage | | $V_{EE} = -4.2V$ | -1150 | | | mV |
| | | | $V_{EE} = -4.5V$ | -1165 | | | mV |
| | | | $V_{EE} = -4.8V$ | | | | |
| $V_{ILT}$ | LOW level input threshold voltage | | $V_{EE} = -4.2V$ | | | -1475 | mV |
| | | | $V_{EE} = -4.5V$ | | | | |
| | | | $V_{EE} = -4.8V$ | | | -1490 | mV |
| $V_{IL}$ | LOW level input voltage | | $V_{EE} = -4.2V$ | -1810 | | -1475 | mV |
| | | | $V_{EE} = -4.5V$ | | | | |
| | | | $V_{EE} = -4.8V$ | | | -1490 | |
| $T_A$ | Operating ambient temperature | | | 0 | +25 | +85 | °C |

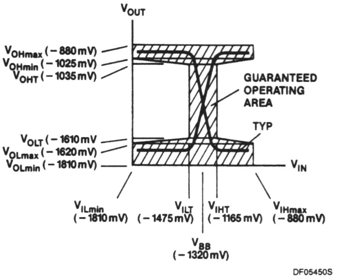
**NOTE:**
When operating at other than specified voltages (-4.2V, -4.5V, -4.8V) DC & AC Characteristics will vary slightly from specified values.

## DC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = \text{GND}$, $V_{EE} = -4.2\text{V} \pm 0.010\text{V}$ to $-4.8\text{V} \pm 0.010\text{V}$, $T_A = 0°\text{C}$ to $+85°\text{C}$ unless otherwise specified[1, 3]

| PARAMETER | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] | |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | $V_{EE} = -4.2\text{V}$ | -1025 | | -870 | mV | $V_{IN} = V_{IHmax}$<br>or<br>$V_{IN} = V_{ILmin}$ | Loading with 50Ω to -2.0V ±0.010V |
| | | $V_{EE} = -4.5\text{V}$ | -1025 | -955 | -880 | mV | | |
| | | $V_{EE} = -4.8\text{V}$ | -1035 | | -880 | mV | | |
| $V_{OHT}$ | HIGH level output threshold voltage | $V_{EE} = -4.2\text{V}$ | -1035 | | | mV | $V_{IN} = V_{IHmin}$<br>or<br>$V_{IN} = V_{ILmax}$ | |
| | | $V_{EE} = -4.5\text{V}$ | -1035 | | | mV | | |
| | | $V_{EE} = -4.8\text{V}$ | -1045 | | | mV | | |
| $V_{OLT}$ | LOW level output threshold voltage | $V_{EE} = -4.2\text{V}$ | | | -1590 | mV | $V_{IN} = V_{IHmin}$<br>or<br>$V_{IN} = V_{ILmax}$ | |
| | | $V_{EE} = -4.5\text{V}$ | | | -1610 | mV | | |
| | | $V_{EE} = -4.8\text{V}$ | | | -1610 | mV | | |
| $V_{OL}$ | LOW level output voltage | $V_{EE} = -4.2\text{V}$ | -1810 | | -1600 | mV | $V_{IN} = V_{IHmax}$<br>or<br>$V_{IN} = V_{ILmin}$ | |
| | | $V_{EE} = -4.5\text{V}$ | -1810 | -1705 | -1620 | mV | | |
| | | $V_{EE} = -4.8\text{V}$ | -1830 | | -1620 | mV | | |
| $I_{IH}$ | HIGH level input current | | | | 350 | μA | $V_{IN} = V_{IHmax}$ | |
| $I_{IL}$ | LOW level input current | | 0.5 | | | μA | $V_{IN} = V_{ILmin}$ | |
| $-I_{EE}$ | $V_{EE}$ supply current | | 18 | 27 | 38 | mA | Inputs open | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | $V_{EE} = -4.2\text{V}$<br>$T_A = +25°\text{C}$ | | | 0.025 | V/V | | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | | 0.05 | V/V | | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to Section 3 Testing, DC testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 3.



**NOTES:**

$V_{IHmax}$ – Maximum HIGH level input voltage (the most positive $V_{IH}$).
$V_{IHT}$ – HIGH level input threshold voltage.
$V_{ILT}$ – LOW level input threshold voltage.
$V_{ILmin}$ – Minimum LOW level input voltage (the most negative $V_{IL}$).
$V_{OHmax}$ – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition.
$V_{OHmin}$ – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition.
$V_{OHT}$ – HIGH level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLT}$ – LOW level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLmax}$ – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions.
$V_{OLmin}$ – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions.
$V_{BB}$ – Reference Bias voltage. The internally generated reference voltage which is used to set the input and output threshold level.

**Figure 3. Transfer Characteristics**

## AC ELECTRICAL CHARACTERISTICS

### Ceramic DIP $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 0.50 | 1.15 | 0.50 | 1.15 | 0.55 | 1.30 | ns | Figs. 4, 5, 6 |
| $t_{PHL}$ | $D_n$ to $Q_n$, $\overline{Q}_n$ | 0.50 | 1.15 | 0.50 | 1.15 | 0.55 | 1.30 | | |
| $t_{TLH}$ | Transition time | 0.45 | 1.20 | 0.45 | 1.10 | 0.45 | 1.10 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.20 | 0.45 | 1.10 | 0.45 | 1.10 | | |

### Ceramic DIP $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V \pm 5\%$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 0.50 | 1.15 | 0.50 | 1.15 | 0.55 | 1.30 | ns | Figs. 4, 5, 6 |
| $t_{PHL}$ | $D_n$ to $Q_n$, $\overline{Q}_n$ | 0.50 | 1.15 | 0.50 | 1.15 | 0.55 | 1.30 | | |
| $t_{TLH}$ | Transition time | 0.45 | 1.20 | 0.45 | 1.10 | 0.45 | 1.10 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.20 | 0.45 | 1.10 | 0.45 | 1.10 | | |

### Flat Pack $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 0.50 | 0.95 | 0.50 | 0.95 | 0.55 | 1.10 | ns | Figs. 4, 5, 6 |
| $t_{PHL}$ | $D_n$ to $Q_n$, $\overline{Q}_n$ | 0.50 | 0.95 | 0.50 | 0.95 | 0.55 | 1.10 | | |
| $t_{TLH}$ | Transition time | 0.45 | 1.20 | 0.45 | 1.10 | 0.45 | 1.10 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.20 | 0.45 | 1.10 | 0.45 | 1.10 | | |

### Flat Pack $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V \pm 5\%$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 0.50 | 0.95 | 0.50 | 0.95 | 0.55 | 1.10 | ns | Figs. 4, 5, 6 |
| $t_{PHL}$ | $D_n$ to $Q_n$, $\overline{Q}_n$ | 0.50 | 0.95 | 0.50 | 0.95 | 0.55 | 1.10 | | |
| $t_{TLH}$ | Transition time | 0.45 | 1.20 | 0.45 | 1.10 | 0.45 | 1.10 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.20 | 0.45 | 1.10 | 0.45 | 1.10 | | |

## AC WAVEFORMS

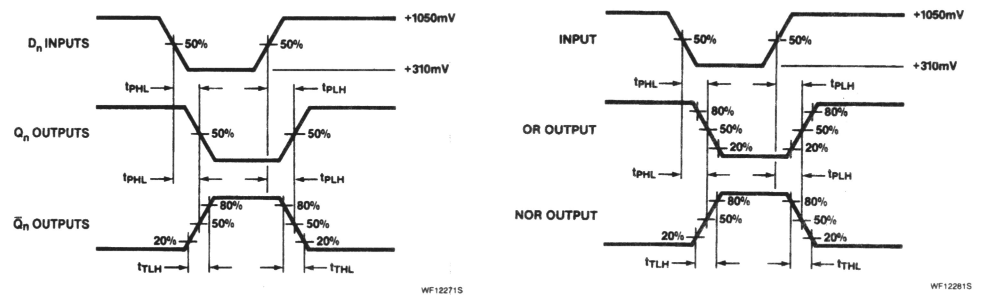
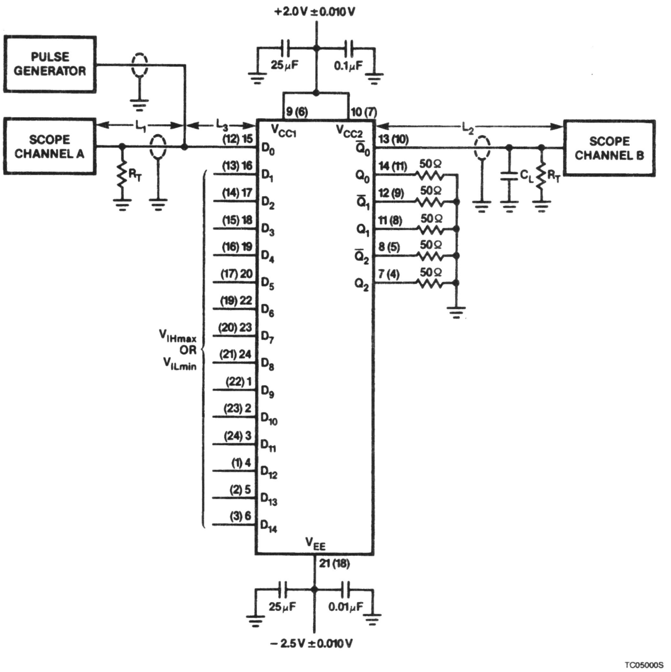

Dn INPUTS
Qn OUTPUTS
$\bar{Q}_n$ OUTPUTS
+1050mV
+310mV
50%
80%
20%
tPHL
tPLH
tTLH
tTHL
WF12271S
INPUT
OR OUTPUT
NOR OUTPUT
WF12281S

Figure 4. Propagation Delay and Transition Times

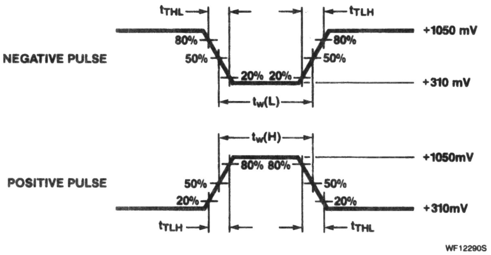
## TEST CIRCUITS AND WAVEFORMS


+2.0V ±0.010V
25μF
0.1μF
PULSE GENERATOR
SCOPE CHANNEL A
SCOPE CHANNEL B
L1
L2
L3
RT
CL
9 (6)
10 (7)
VCC1
VCC2
(12) 15 D0
(13) 16 D1
(14) 17 D2
(15) 18 D3
(16) 19 D4
(17) 20 D5
(19) 22 D6
(20) 23 D7
(21) 24 D8
(22) 1 D9
(23) 2 D10
(24) 3 D11
(1) 4 D12
(2) 5 D13
(3) 6 D14
13 (10) $\bar{Q}_0$
14 (11) Q0
12 (9) $\bar{Q}_1$
11 (8) Q1
8 (5) $\bar{Q}_2$
7 (4) Q2
50Ω
VIHmax OR VILmin
VEE
21 (18)
0.01μF
−2.5V ±0.010V
TC05000S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1μF and 25μF from GND to $V_{CC}$, 0.01μF and 25μF from GND to $V_{EE}$ (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance ≤ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ±1% or better.
11. Pin connections are for Flat Pack and in parentheses for Ceramic DIP package.

Figure 5. Test Circuit


NEGATIVE PULSE
$t_{THL}$
$t_{TLH}$
80%
50%
20% 20%
80%
50%
+1050 mV
+310 mV
$t_w(L)$
$t_w(H)$
POSITIVE PULSE
80% 80%
50%
20%
50%
20%
+1050mV
+310mV
$t_{TLH}$
$t_{THL}$
WF12290S

| INPUT PULSE REQUIREMENTS<br>$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -2.5V \pm 0.010V$, $V_T = GND$ (0V) | | | | | |
|---|---|---|---|---|---|
| **Family** | **Amplitude** | **Rep Rate** | **Pulse Width** | $t_{TLH}$ | $t_{THL}$ |
| 100K ECL | 740mVp-p | 1MHz | 500ns | 0.7 ±0.1ns | 0.7 ±0.1ns |

**Figure 6. Input Pulse Definition**

Signetics

# 100102
## Gate

**Quint 2-Input OR-NOR Gate With Common Enable**
***Product Specification***

**ECL Products**

### DESCRIPTION

The 100102 has five 3-input gates. One input is a common enable to all five gates.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 100102 | 0.75ns | 55mA |

### ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} = GND$; $V_{EE} = -4.2V$ to $-4.8V$<br>$T_A = 0°C$ to $+85°C$ |
|---|---|
| Ceramic DIP | 100102F |
| Ceramic Flat Pack | 100102Y |

### PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_0 - D_9$ | Data Inputs |
| $\overline{E}$ | Enable Input |
| $Q_0 - Q_4$ | Data Outputs (OR) |
| $\overline{Q}_0 - \overline{Q}_4$ | Data Outputs (NOR) |

### PIN CONFIGURATION

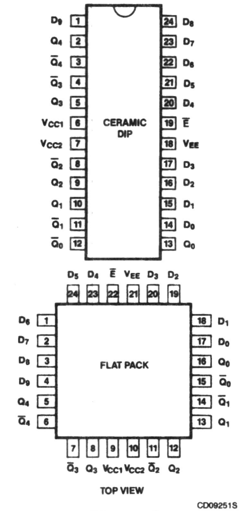

$D_9$ 1
$Q_4$ 2
$\overline{Q}_4$ 3
$\overline{Q}_3$ 4
$Q_3$ 5
$V_{CC1}$ 6
$V_{CC2}$ 7
$\overline{Q}_2$ 8
$Q_2$ 9
$Q_1$ 10
$\overline{Q}_1$ 11
$\overline{Q}_0$ 12
24 $D_8$
23 $D_7$
22 $D_6$
21 $D_5$
20 $D_4$
19 $\overline{E}$
18 $V_{EE}$
17 $D_3$
16 $D_2$
15 $D_1$
14 $D_0$
13 $Q_0$
CERAMIC DIP
$D_5$ $D_4$ $\overline{E}$ $V_{EE}$ $D_3$ $D_2$
24 23 22 21 20 19
$D_6$ 1
$D_7$ 2
$D_8$ 3
$D_9$ 4
$Q_4$ 5
$\overline{Q}_4$ 6
18 $D_1$
17 $D_0$
16 $Q_0$
15 $\overline{Q}_0$
14 $\overline{Q}_1$
13 $Q_1$
FLAT PACK
7 8 9 10 11 12
$\overline{Q}_3$ $Q_3$ $V_{CC1}$ $V_{CC2}$ $\overline{Q}_2$ $Q_2$
TOP VIEW
CD09251S

Figure 1

### LOGIC SYMBOL

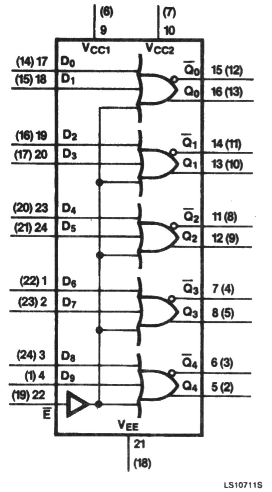

(6) 9
(7) 10
$V_{CC1}$
$V_{CC2}$
(14) 17 $D_0$
(15) 18 $D_1$
(16) 19 $D_2$
(17) 20 $D_3$
(20) 23 $D_4$
(21) 24 $D_5$
(22) 1 $D_6$
(23) 2 $D_7$
(24) 3 $D_8$
(1) 4 $D_9$
(19) 22 $\overline{E}$
$\overline{Q}_0$ 15 (12)
$Q_0$ 16 (13)
$\overline{Q}_1$ 14 (11)
$Q_1$ 13 (10)
$\overline{Q}_2$ 11 (8)
$Q_2$ 12 (9)
$\overline{Q}_3$ 7 (4)
$Q_3$ 8 (5)
$\overline{Q}_4$ 6 (3)
$Q_4$ 5 (2)
$V_{EE}$
21
(18)
LS10711S

Figure 2

## FUNCTION TABLE (One Gate)

| INPUTS | | | OUTPUTS | |
|---|---|---|---|---|
| $D_0$ | $D_1$ | $\overline{E}$ | $Q_0$ | $\overline{Q}_0$ |
| X | X | H | H | L |
| X | H | X | H | L |
| H | X | X | H | L |
| L | L | L | L | H |

Positive Logic:
H = HIGH state (more positive voltage) = 1
L = LOW state (less positive voltage) = 0
X = Don't Care

## ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| | PARAMETER | 100K ECL | UNIT |
|---|---|---|---|
| $V_{EE}$ | Supply voltage ($V_{CC1} = V_{CC2} = GND$) | −7.0 to 0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | $V_{EE}$ to +0.5 | V |
| $I_O$ | Output current | −55 | mA |
| $T_S$ | Storage temperature | −65 to +150 | °C |
| $T_J$ | Maximum junction temperature | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | | 100K ECL | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | −4.2 | −4.5 | −4.8 | V |
| $V_{EE}$ | Supply voltage (negative) when operating with 10K ECL family | | | | | −5.7 | V |
| $V_{IH}$ | HIGH level input voltage | $V_{CC1} = V_{CC2} = GND$<br>$T_A = 0°C$ to $+85°C$ | $V_{EE} = -4.2V$ | −1150 | | −880 | mV |
| | | | $V_{EE} = -4.5V$ | −1165 | | | |
| | | | $V_{EE} = -4.8V$ | | | | |
| $V_{IHT}$ | HIGH level input threshold voltage | | $V_{EE} = -4.2V$ | −1150 | | | mV |
| | | | $V_{EE} = -4.5V$ | −1165 | | | mV |
| | | | $V_{EE} = -4.8V$ | | | | |
| $V_{ILT}$ | LOW level input threshold voltage | | $V_{EE} = -4.2V$ | | | −1475 | mV |
| | | | $V_{EE} = -4.5V$ | | | | |
| | | | $V_{EE} = -4.8V$ | | | −1490 | mV |
| $V_{IL}$ | LOW level input voltage | | $V_{EE} = -4.2V$ | −1810 | | −1475 | mV |
| | | | $V_{EE} = -4.5V$ | | | | |
| | | | $V_{EE} = -4.8V$ | | | −1490 | |
| $T_A$ | Operating ambient temperature | | | 0 | +25 | +85 | °C |

**NOTE:**
When operating at other than specified voltages (−4.2V, −4.5V, −4.8V) DC & AC Characteristics will vary slightly from specified values.

## Gate

## 100102

**DC ELECTRICAL CHARACTERISTICS** $V_{CC1} = V_{CC2}$ = GND, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$, $T_A = 0°C$ to $+85°C$ unless otherwise specified[1, 3]

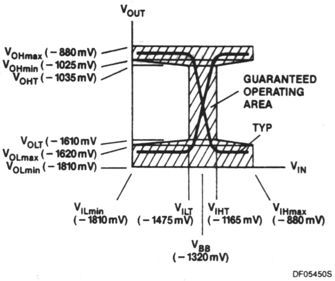
| PARAMETER | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] | |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | $V_{EE} = -4.2V$ | −1025 | | −870 | mV | $V_{IN} = V_{IHmax}$<br>or<br>$V_{IN} = V_{ILmin}$ | Loading with 50Ω to −2.0V ±0.010V |
| | | $V_{EE} = -4.5V$ | −1025 | −955 | −880 | mV | | |
| | | $V_{EE} = -4.8V$ | −1035 | | −880 | mV | | |
| $V_{OHT}$ | HIGH level output threshold voltage | $V_{EE} = -4.2V$ | −1035 | | | mV | $V_{IN} = V_{IHmin}$<br>or<br>$V_{IN} = V_{ILmax}$ | |
| | | $V_{EE} = -4.5V$ | −1035 | | | mV | | |
| | | $V_{EE} = -4.8V$ | −1045 | | | mV | | |
| $V_{OLT}$ | LOW level output threshold voltage | $V_{EE} = -4.2V$ | | | −1590 | mV | $V_{IN} = V_{IHmin}$<br>or<br>$V_{IN} = V_{ILmax}$ | |
| | | $V_{EE} = -4.5V$ | | | −1610 | mV | | |
| | | $V_{EE} = -4.8V$ | | | −1610 | mV | | |
| $V_{OL}$ | LOW level output voltage | $V_{EE} = -4.2V$ | −1810 | | −1600 | mV | $V_{IN} = V_{IHmax}$<br>or<br>$V_{IN} = V_{ILmin}$ | |
| | | $V_{EE} = -4.5V$ | −1810 | −1705 | −1620 | mV | | |
| | | $V_{EE} = -4.8V$ | −1830 | | −1620 | mV | | |
| $I_{IH}$ | HIGH level input current | $D_n$ inputs | | | 350 | μA | $V_{IN} = V_{IHmax}$ | |
| | | E input | | | 300 | μA | | |
| $I_{IL}$ | LOW level input current | | 0.5 | | | μA | $V_{IN} = V_{ILmin}$ | |
| $-I_{EE}$ | $V_{EE}$ supply current | | 38 | 55 | 80 | mA | Inputs open | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | $V_{EE} = -4.2V$<br>$T_A = +25°C$ | | | 0.025 | V/V | | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | | 0.05 | V/V | | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to Section 3 Testing, DC testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 3.

## Gate

## 100102



**NOTES:**

$V_{IHmax}$ – Maximum HIGH level input voltage (the most positive $V_{IH}$).
$V_{IHT}$ – HIGH level input threshold voltage.
$V_{ILT}$ – LOW level input threshold voltage.
$V_{ILmin}$ – Minimum LOW level input voltage (the most negative $V_{IL}$).
$V_{OHmax}$ – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition.
$V_{OHmin}$ – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition.
$V_{OHT}$ – HIGH level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLT}$ – LOW level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLmax}$ – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions.
$V_{OLmin}$ – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions.
$V_{BB}$ – Reference Bias voltage. The internally generated reference voltage which is used to set the input and output threshold level.

**Figure 3. Transfer Characteristics**

## AC ELECTRICAL CHARACTERISTICS

**Ceramic DIP** $V_{CC1} = V_{CC2} =$ GND, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$D_n$ to $Q_n$ | 0.45<br>0.45 | 1.35<br>1.35 | 0.45<br>0.45 | 1.15<br>1.15 | 0.45<br>0.45 | 1.40<br>1.40 | ns<br>ns | Figs. 4, 5, 6 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>E to $Q_n$ | 0.90<br>0.90 | 2.15<br>2.15 | 0.95<br>0.95 | 2.15<br>2.15 | 0.95<br>0.95 | 2.20<br>2.20 | ns<br>ns | |
| $t_{TLH}$<br>$t_{THL}$ | Transition time<br>20% to 80%, 80% to 20% | 0.45<br>0.45 | 1.20<br>1.20 | 0.45<br>0.45 | 1.10<br>1.10 | 0.45<br>0.45 | 1.10<br>1.10 | ns<br>ns | |

**Ceramic DIP** $V_{CC1} = V_{CC2} =$ GND, $V_{EE} = -5.2V \pm 5\%$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$D_n$ to $Q_n$ | 0.45<br>0.45 | 1.35<br>1.35 | 0.45<br>0.45 | 1.15<br>1.15 | 0.45<br>0.45 | 1.40<br>1.40 | ns<br>ns | Figs. 4, 5, 6 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>E to $Q_n$ | 0.90<br>0.90 | 2.15<br>2.15 | 0.95<br>0.95 | 2.15<br>2.15 | 0.95<br>0.95 | 2.20<br>2.20 | ns<br>ns | |
| $t_{TLH}$<br>$t_{THL}$ | Transition time<br>20% to 80%, 80% to 20% | 0.45<br>0.45 | 1.20<br>1.20 | 0.45<br>0.45 | 1.10<br>1.10 | 0.45<br>0.45 | 1.10<br>1.10 | ns<br>ns | |

**Flat Pack** $V_{CC1} = V_{CC2} =$ GND, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$D_n$ to $Q_n$ | 0.45<br>0.45 | 1.15<br>1.15 | 0.45<br>0.45 | 0.95<br>0.95 | 0.45<br>0.45 | 1.20<br>1.20 | ns<br>ns | Figs. 4, 5, 6 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay | 0.90<br>0.90 | 1.95<br>1.95 | 0.95<br>0.95 | 1.95<br>1.95 | 0.95<br>0.95 | 2.00<br>2.00 | ns<br>ns | |
| $t_{TLH}$<br>$t_{THL}$ | Transition time<br>20% to 80%, 80% to 20% | 0.45<br>0.45 | 1.20<br>1.20 | 0.45<br>0.45 | 1.10<br>1.10 | 0.45<br>0.45 | 1.10<br>1.10 | ns<br>ns | |

## Gate 100102

### AC ELECTRICAL CHARACTERISTICS

**Flat Pack** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V \pm 5\%$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 0.45 | 1.15 | 0.45 | 0.95 | 0.45 | 1.20 | ns | Figs. 4, 5, 6 |
| $t_{PHL}$ | $D_n$ to $Q_n$ | 0.45 | 1.15 | 0.45 | 0.95 | 0.45 | 1.20 | ns | |
| $t_{PLH}$ | Propagation delay | 0.90 | 1.95 | 0.95 | 1.95 | 0.95 | 2.00 | ns | |
| $t_{PHL}$ | | 0.90 | 1.95 | 0.95 | 1.95 | 0.95 | 2.00 | ns | |
| $t_{TLH}$ | Transition time | 0.45 | 1.20 | 0.45 | 1.10 | 0.45 | 1.10 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.20 | 0.45 | 1.10 | 0.45 | 1.10 | ns | |

### AC WAVEFORMS

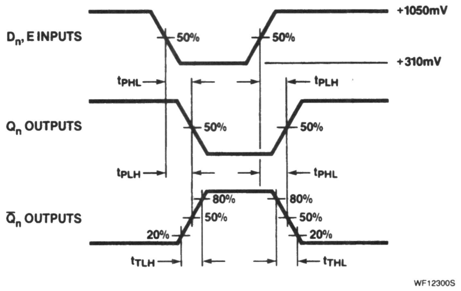
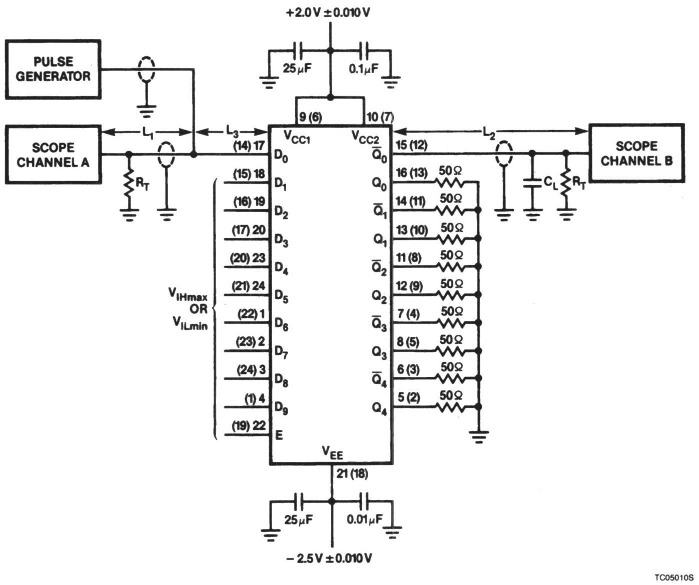

D_n, E INPUTS
50%
50%
+1050mV
+310mV
tPHL
tPLH
Q_n OUTPUTS
50%
50%
tPLH
tPHL
Q̄_n OUTPUTS
80%
80%
50%
50%
20%
20%
tTLH
tTHL
WF12300S

Figure 4. Propagation Delay and Transition Times

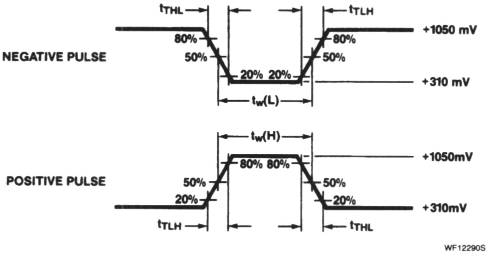
## TEST CIRCUITS AND WAVEFORMS


+2.0V ±0.010V
25µF
0.1µF
PULSE GENERATOR
SCOPE CHANNEL A
SCOPE CHANNEL B
L1
L2
L3
RT
CL
9 (6)
10 (7)
VCC1
VCC2
(14) 17 D0
(15) 18 D1
(16) 19 D2
(17) 20 D3
(20) 23 D4
(21) 24 D5
(22) 1 D6
(23) 2 D7
(24) 3 D8
(1) 4 D9
(19) 22 E
VIHmax OR VILmin
15 (12) Q̄0
16 (13) Q0
14 (11) Q̄1
13 (10) Q1
11 (8) Q̄2
12 (9) Q2
7 (4) Q̄3
8 (5) Q3
6 (3) Q̄4
5 (2) Q4
50Ω
VEE
21 (18)
25µF
0.01µF
−2.5V ±0.010V
TC05010S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1µF and 25µF from GND to $V_{CC}$, 0.01µF and 25µF from GND to $V_{EE}$. (0.01 and 0.1µF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance ≤ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.
11. Pin connections are for Flat Pack and in parentheses for Ceramic DIP package.

Figure 5. Test Circuit


NEGATIVE PULSE
tTHL
tTLH
80%
50%
20% 20%
tw(L)
+1050 mV
+310 mV
POSITIVE PULSE
tw(H)
80% 80%
50%
20%
tTLH
tTHL
+1050mV
+310mV
WF12290S

| INPUT PULSE REQUIREMENTS<br>$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -2.5V \pm 0.010V$, $V_T$ = GND (0V) | | | | | |
|---|---|---|---|---|---|
| Family | Amplitude | Rep Rate | Pulse Width | $t_{TLH}$ | $t_{THL}$ |
| 100K ECL | 740mVp-p | 1MHz | 500ns | 0.7 ±0.1ns | 0.7 ±0.1ns |

Figure 6. Input Pulse Definition

**Signetics**

# 100107
## Gate

**Quint Exclusive-OR/Exclusive-NOR Gate With Compare Output**
***Product Specification***

**ECL Products**

### DESCRIPTION

The 100107 has five 2-input, 2-output Exclusive-OR/NOR gates with a compare output.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 100107 | 0.95ns | 68mA |

### ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} = GND$; $V_{EE} = -4.2V$ to $-4.8V$<br>$T_A = 0°C$ to $+85°C$ |
|---|---|
| Ceramic DIP | 100107F |
| Ceramic Flat Pack | 100107Y |

### PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_0 - D_9$ | Data Inputs |
| $Q_0 - Q_4$ | Data Outputs (OR) |
| $\overline{Q}_0 - \overline{Q}_4$ | Data Outputs (NOR) |
| $Q_5$ | Compare Output |

### PIN CONFIGURATION

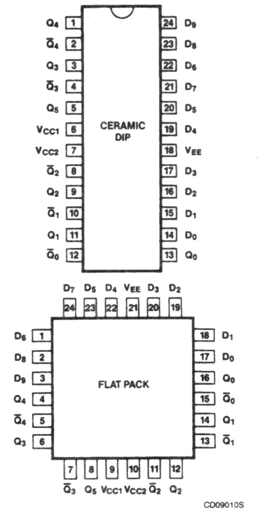
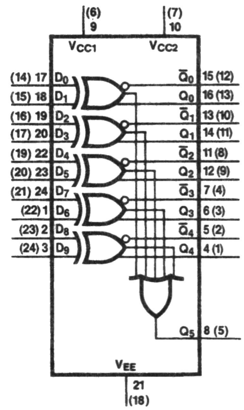

$Q_4$ 1
$\overline{Q}_4$ 2
$Q_3$ 3
$\overline{Q}_3$ 4
$Q_5$ 5
$V_{CC1}$ 6
$V_{CC2}$ 7
$\overline{Q}_2$ 8
$Q_2$ 9
$\overline{Q}_1$ 10
$Q_1$ 11
$\overline{Q}_0$ 12
24 $D_9$
23 $D_8$
22 $D_6$
21 $D_7$
20 $D_5$
19 $D_4$
18 $V_{EE}$
17 $D_3$
16 $D_2$
15 $D_1$
14 $D_0$
13 $Q_0$
CERAMIC DIP
$D_7$ $D_5$ $D_4$ $V_{EE}$ $D_3$ $D_2$
24 23 22 21 20 19
$D_6$ 1
$D_8$ 2
$D_9$ 3
$Q_4$ 4
$\overline{Q}_4$ 5
$Q_3$ 6
18 $D_1$
17 $D_0$
16 $Q_0$
15 $\overline{Q}_0$
14 $Q_1$
13 $\overline{Q}_1$
FLAT PACK
7 8 9 10 11 12
$\overline{Q}_3$ $Q_5$ $V_{CC1}$ $V_{CC2}$ $\overline{Q}_2$ $Q_2$
CD09010S

Figure 1

### LOGIC SYMBOL


(6) 9
(7) 10
$V_{CC1}$
$V_{CC2}$
(14) 17 $D_0$
(15) 18 $D_1$
(16) 19 $D_2$
(17) 20 $D_3$
(19) 22 $D_4$
(20) 23 $D_5$
(21) 24 $D_7$
(22) 1 $D_6$
(23) 2 $D_8$
(24) 3 $D_9$
$\overline{Q}_0$ 15 (12)
$Q_0$ 16 (13)
$\overline{Q}_1$ 13 (10)
$Q_1$ 14 (11)
$\overline{Q}_2$ 11 (8)
$Q_2$ 12 (9)
$\overline{Q}_3$ 7 (4)
$Q_3$ 6 (3)
$\overline{Q}_4$ 5 (2)
$Q_4$ 4 (1)
$Q_5$ 8 (5)
$V_{EE}$
21
(18)

Pin connections for Flat Pack and in ( ) for Ceramic DIP package

LD05110S

Figure 2

## TRUTH TABLE

| INPUTS | | | | | OUTPUT |
|---|---|---|---|---|---|
| $D_0 \oplus D_1$ | $D_2 \oplus D_3$ | $D_4 \oplus D_5$ | $D_6 \oplus D_7$ | $D_8 \oplus D_9$ | $Q_5$ |
| L | L | L | L | L | L |
| H | X | X | X | X | H |
| X | H | X | X | X | H |
| X | X | H | X | X | H |
| X | X | X | H | X | H |
| X | X | X | X | H | H |

⊕ = Exclusive OR
Positive Logic:
H = HIGH state (more positive voltage) = 1
L = LOW state (less positive voltage) = 0
X = Don't Care

## FUNCTION TABLE (One Gate)

| INPUTS | | OUTPUTS | |
|---|---|---|---|
| $D_0$ | $D_1$ | $Q_0$ | $\overline{Q}_0$ |
| L | L | L | H |
| L | H | H | L |
| H | L | H | L |
| H | H | L | H |

## ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | 100K ECL | UNIT |
|---|---|---|---|
| $V_{EE}$ | Supply voltage $V_{CC1} = V_{CC2} = GND$ | -7.0 to 0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | $V_{EE}$ to +0.5 | V |
| $I_O$ | Output source current | -55 | mA |
| $T_S$ | Storage temperature | -65 to +150 | °C |
| $T_J$ | Maximum junction temperature | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | | 100K ECL | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | -4.2 | -4.5 | -4.8 | V |
| $V_{EE}$ | Supply voltage (negative) when operating with 10K ECL family | | | | | -5.7 | V |
| $V_{IH}$ | HIGH level input voltage | $V_{CC1} = V_{CC2} = GND$<br>$T_A = 0°C$ to $+85°C$ | $V_{EE} = -4.2V$ | -1150 | | -880 | mV |
| | | | $V_{EE} = -4.5V$ | -1165 | | | |
| | | | $V_{EE} = -4.8V$ | | | | |
| $V_{IHT}$ | HIGH level input threshold voltage | | $V_{EE} = -4.2V$ | -1150 | | | mV |
| | | | $V_{EE} = -4.5V$ | -1165 | | | mV |
| | | | $V_{EE} = -4.8V$ | | | | |
| $V_{ILT}$ | LOW level input threshold voltage | | $V_{EE} = -4.2V$ | | | -1475 | mV |
| | | | $V_{EE} = -4.5V$ | | | | |
| | | | $V_{EE} = -4.8V$ | | | -1490 | mV |
| $V_{IL}$ | LOW level input voltage | | $V_{EE} = -4.2V$ | -1810 | | -1475 | mV |
| | | | $V_{EE} = -4.5V$ | | | | |
| | | | $V_{EE} = -4.8V$ | | | -1490 | |
| $T_A$ | Operating ambient temperature | | | 0 | +25 | +85 | °C |

**NOTE:**
When operating at other than specified voltages (-4.2V, -4.5V, -4.8V) DC & AC Characteristics will vary slightly from specified values.

**DC ELECTRICAL CHARACTERISTICS** $V_{CC1} = V_{CC2}$ = GND, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$, $T_A = 0°C$ to $+85°C$ 10V unless otherwise specified[1, 3]

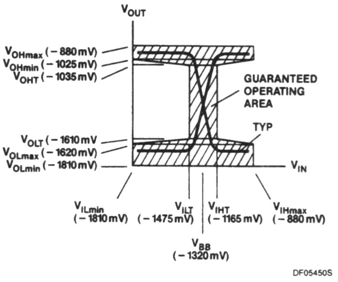
| PARAMETER | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] | |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | $V_{EE} = -4.2V$ | −1025 | | −870 | mV | $V_{IN} = V_{IHmax}$ or $V_{IN} = V_{ILmin}$ | Loading with 50Ω to −2.0V |
| | | $V_{EE} = -4.5V$ | −1025 | −955 | −880 | mV | | |
| | | $V_{EE} = -4.8V$ | −1035 | | −880 | mV | | |
| $V_{OHT}$ | HIGH level output threshold voltage | $V_{EE} = -4.2V$ | −1035 | | | mV | $V_{IN} = V_{IHmin}$ or $V_{IN} = V_{ILmax}$ | |
| | | $V_{EE} = -4.5V$ | −1035 | | | mV | | |
| | | $V_{EE} = -4.8V$ | −1045 | | | mV | | |
| $V_{OLT}$ | LOW level output threshold voltage | $V_{EE} = -4.2V$ | | | −1590 | mV | $V_{IN} = V_{IHmin}$ or $V_{IN} = V_{ILmax}$ | |
| | | $V_{EE} = -4.5V$ | | | −1610 | mV | | |
| | | $V_{EE} = -4.8V$ | | | −1610 | mV | | |
| $V_{OL}$ | LOW level output voltage | $V_{EE} = -4.2V$ | −1810 | | −1605 | mV | $V_{IN} = V_{IHmax}$ or $V_{IN} = V_{ILmin}$ | |
| | | $V_{EE} = -4.5V$ | −1810 | −1705 | −1620 | mV | | |
| | | $V_{EE} = -4.8V$ | −1830 | | −1620 | mV | | |
| $I_{IH}$ | HIGH level input current | $D_1$, $D_3$, $D_5$ $D_7$, $D_9$ | | | 250 | μA | $V_{IN} = V_{IHmax}$ | |
| | | $D_0$, $D_2$, $D_4$ $D_6$, $D_8$ | | | 350 | μA | | |
| $I_{IL}$ | LOW level input current | | 0.5 | | | μA | $V_{IN} = V_{ILmin}$ | |
| $-I_{EE}$ | $V_{EE}$ supply current | | 46 | 68 | 96 | mA | Inputs open | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | $V_{EE} = -4.2V$ $T_A = +25°C$ | | | 0.025 | V/V | | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | | 0.05 | V/V | | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to Section 3 Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 3.

# Gate

# 100107



**NOTES:**

| | |
|---|---|
| $V_{IHmax}$ | – Maximum HIGH level input voltage (the most positive $V_{IH}$). |
| $V_{IHT}$ | – HIGH level input threshold voltage. |
| $V_{ILT}$ | – LOW level input threshold voltage. |
| $V_{ILmin}$ | – Minimum LOW level input voltage (the most negative $V_{IL}$). |
| $V_{OHmax}$ | – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition. |
| $V_{OHmin}$ | – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition. |
| $V_{OHT}$ | – HIGH level output threshold voltage with the inputs set to their respective threshold levels. |
| $V_{OLT}$ | – LOW level output threshold voltage with the inputs set to their respective threshold levels. |
| $V_{OLmax}$ | – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions. |
| $V_{OLmin}$ | – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions. |
| $V_{BB}$ | – Reference Bias voltage. The internally generated reference voltage which is used to set the input and output threshold level. |

**Figure 3. Transfer Characteristics**

## AC ELECTRICAL CHARACTERISTICS

**Ceramic DIP** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 0.55 | 1.90 | 0.55 | 1.80 | 0.55 | 1.90 | ns | Figs. 4, 5, 6 |
| $t_{PHL}$ | $D_0, D_2, D_4, D_6, D_8$ to $Q_0 - Q_4, \overline{Q}_n$ | 0.55 | 1.90 | 0.55 | 1.80 | 0.55 | 1.90 | ns | |
| $t_{PLH}$ | Propagation delay | 0.55 | 1.70 | 0.55 | 1.60 | 0.55 | 1.70 | ns | |
| $t_{PHL}$ | $D_1, D_3, D_5, D_7, D_9$ to $Q_0 - Q_4, \overline{Q}_n$ | 0.55 | 1.70 | 0.55 | 1.60 | 0.55 | 1.70 | ns | |
| $t_{PLH}$ | Propagation delay | 1.15 | 2.75 | 1.15 | 2.75 | 1.15 | 3.00 | ns | |
| $t_{PHL}$ | $D_n$ to $Q_5$ | 1.15 | 2.75 | 1.15 | 2.75 | 1.15 | 3.00 | ns | |
| $t_{TLH}$ | Transition time | 0.45 | 1.70 | 0.45 | 1.55 | 0.45 | 1.70 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.70 | 0.45 | 1.55 | 0.45 | 1.70 | ns | |

**Ceramic DIP** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V \pm 5\%$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 0.55 | 1.90 | 0.55 | 1.80 | 0.55 | 1.90 | ns | Figs. 4, 5, 6 |
| $t_{PHL}$ | $D_0, D_2, D_4, D_6, D_8$ to $Q_0 - Q_4, \overline{Q}_n$ | 0.55 | 1.90 | 0.55 | 1.80 | 0.55 | 1.90 | ns | |
| $t_{PLH}$ | Propagation delay | 0.55 | 1.70 | 0.55 | 1.60 | 0.55 | 1.70 | ns | |
| $t_{PHL}$ | $D_1, D_3, D_5, D_7, D_9$ to $Q_0 - Q_4, \overline{Q}_n$ | 0.55 | 1.70 | 0.55 | 1.60 | 0.55 | 1.70 | ns | |
| $t_{PLH}$ | Propagation delay | 1.15 | 2.75 | 1.15 | 2.75 | 1.15 | 3.00 | ns | |
| $t_{PHL}$ | $D_n$ to $Q_5$ | 1.15 | 2.75 | 1.15 | 2.75 | 1.15 | 3.00 | ns | |
| $t_{TLH}$ | Transition time | 0.45 | 1.70 | 0.45 | 1.55 | 0.45 | 1.70 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.70 | 0.45 | 1.55 | 0.45 | 1.70 | ns | |

**Flat Pack** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 0.55 | 1.70 | 0.55 | 1.60 | 0.55 | 1.70 | ns | Figs. 4, 5, 6 |
| $t_{PHL}$ | $D_0, D_2, D_4, D_6, D_8$ to $Q_0 - Q_4, \overline{Q}_n$ | 0.55 | 1.70 | 0.55 | 1.60 | 0.55 | 1.70 | ns | |
| $t_{PLH}$ | Propagation delay | 0.55 | 1.50 | 0.55 | 1.40 | 0.55 | 1.50 | ns | |
| $t_{PHL}$ | $D_1, D_3, D_5, D_7, D_9$ to $Q_0 - Q_4, \overline{Q}_n$ | 0.55 | 1.50 | 0.55 | 1.40 | 0.55 | 1.50 | ns | |
| $t_{PLH}$ | Propagation delay | 1.15 | 2.55 | 1.15 | 2.55 | 1.15 | 2.80 | ns | |
| $t_{PHL}$ | $D_n$ to $Q_5$ | 1.15 | 2.55 | 1.15 | 2.55 | 1.15 | 2.80 | ns | |
| $t_{TLH}$ | Transition time | 0.45 | 1.70 | 0.45 | 1.55 | 0.45 | 1.70 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.70 | 0.45 | 1.55 | 0.45 | 1.70 | ns | |

## AC ELECTRICAL CHARACTERISTICS

**Flat Pack** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V \pm 5\%$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$D_0, D_2, D_4, D_6, D_8$ to $Q_0 - Q_4, \overline{Q}_n$ | 0.55<br>0.55 | 1.70<br>1.70 | 0.55<br>0.55 | 1.60<br>1.60 | 0.55<br>0.55 | 1.70<br>1.70 | ns<br>ns | Figs. 4, 5, 6 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$D_1, D_3, D_5, D_7, D_9$ to $Q_0 - Q_4, \overline{Q}_n$ | 0.55<br>0.55 | 1.50<br>1.50 | 0.55<br>0.55 | 1.40<br>1.40 | 0.55<br>0.55 | 1.50<br>1.50 | ns<br>ns | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$D_n$ to $Q_5$ | 1.15<br>1.15 | 2.55<br>2.55 | 1.15<br>1.15 | 2.55<br>2.55 | 1.15<br>1.15 | 2.80<br>2.80 | ns<br>ns | |
| $t_{TLH}$<br>$t_{THL}$ | Transition time<br>20% to 80%, 80% to 20% | 0.45<br>0.45 | 1.70<br>1.70 | 0.45<br>0.45 | 1.55<br>1.55 | 0.45<br>0.45 | 1.70<br>1.70 | ns<br>ns | |

## AC WAVEFORMS

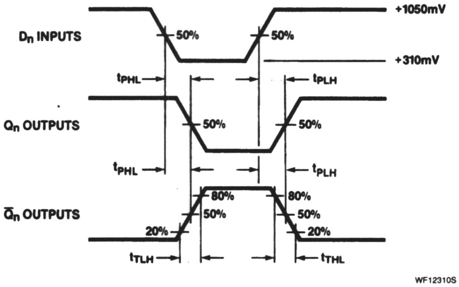
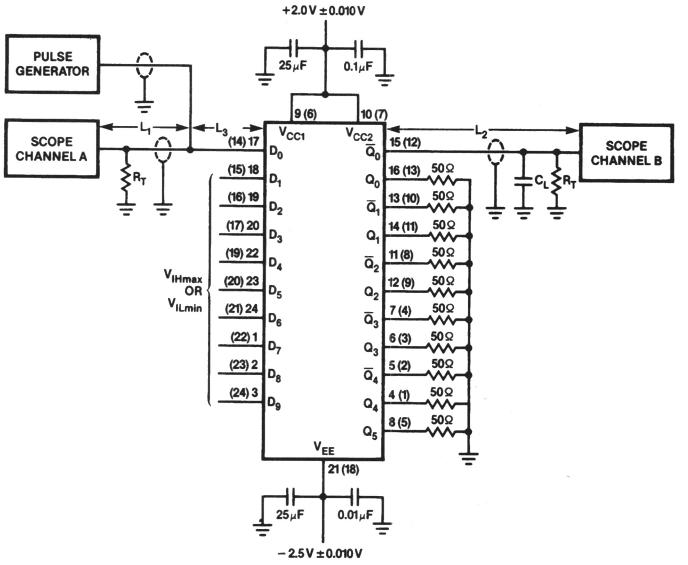

$D_n$ INPUTS
50%
50%
+1050mV
+310mV
$t_{PHL}$
$t_{PLH}$
$Q_n$ OUTPUTS
50%
50%
$t_{PHL}$
$t_{PLH}$
$\overline{Q}_n$ OUTPUTS
80%
50%
20%
80%
50%
20%
$t_{TLH}$
$t_{THL}$
WF12310S

Figure 4. Propagation Delay and Transition Times

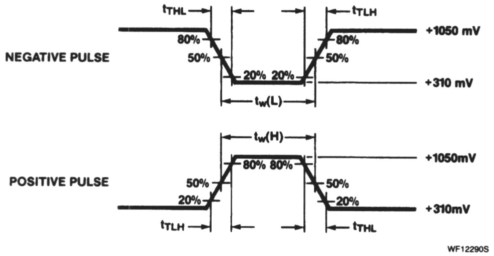
## TEST CIRCUITS AND WAVEFORMS


+2.0V ±0.010V
25μF
0.1μF
PULSE GENERATOR
SCOPE CHANNEL A
$R_T$
$L_1$
$L_3$
9 (6)
10 (7)
$V_{CC1}$
$V_{CC2}$
(14) 17 $D_0$
(15) 18 $D_1$
(16) 19 $D_2$
(17) 20 $D_3$
(19) 22 $D_4$
(20) 23 $D_5$
(21) 24 $D_6$
(22) 1 $D_7$
(23) 2 $D_8$
(24) 3 $D_9$
$V_{IHmax}$ OR $V_{ILmin}$
$L_2$
15 (12) $\overline{Q}_0$
16 (13) $Q_0$
13 (10) $\overline{Q}_1$
14 (11) $Q_1$
11 (8) $\overline{Q}_2$
12 (9) $Q_2$
7 (4) $\overline{Q}_3$
6 (3) $Q_3$
5 (2) $\overline{Q}_4$
4 (1) $Q_4$
8 (5) $Q_5$
50Ω
$C_L$
$R_T$
SCOPE CHANNEL B
$V_{EE}$
21 (18)
25μF
0.01μF
−2.5V ±0.010V
TC05060S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1μF and 25μF from GND to $V_{CC}$, 0.01μF and 25μF from GND to $V_{EE}$. (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines . $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T = 50\Omega$ terminator internal to Scope
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance $\leqslant$ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.
11. Pin connections are for Flat Pack and in parentheses for Ceramic DIP package.

Figure 5. Test Circuit


$t_{THL}$
$t_{TLH}$
NEGATIVE PULSE
80%
50%
20% 20%
80%
50%
+1050 mV
+310 mV
$t_w(L)$
$t_w(H)$
POSITIVE PULSE
80% 80%
50%
20%
50%
20%
+1050mV
+310mV
$t_{TLH}$
$t_{THL}$
WF12290S

| INPUT PULSE REQUIREMENTS<br>$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -2.5V \pm 0.010V$, $V_T$ = GND (0V) | | | | | |
|---|---|---|---|---|---|
| **Family** | **Amplitude** | **Rep Rate** | **Pulse Width** | **$t_{TLH}$** | **$t_{THL}$** |
| 100K ECL | 740mVp-p | 1MHz | 500ns | 0.7 ±0.1ns | 0.7 ±0.1ns |

Figure 6. Input Pulse Definition

**Signetics**

# 100112
## Driver

**Quad Driver**
***Product Specification***

**ECL Products**

### DESCRIPTION

The 100112 has four 2-input OR-NOR gates, with one common enable input. Each gate has two OR outputs and two NOR outputs.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 100112 | 0.85ns | 73mA |
|  | Enable input 1.4ns |  |

### ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} = \text{GND}$; $V_{EE} = -4.2\text{V}$ to $-4.8\text{V}$<br>$T_A = 0°\text{C}$ to $+85°\text{C}$ |
|---|---|
| Ceramic DIP | 100112F |
| Ceramic Flat Pack | 100112Y |

### PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_0 - D_3$ | Data Inputs |
| $\overline{E}$ | Enable Input |
| $Q_0 - Q_7$ | Data Outputs (OR) |
| $\overline{Q}_0 - \overline{Q}_7$ | Data Outputs (NOR) |

### PIN CONFIGURATION

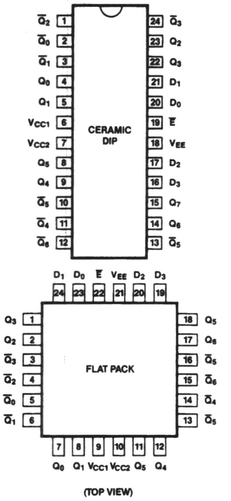
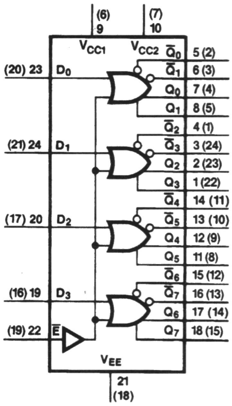

$\overline{Q}_2$ 1
$\overline{Q}_0$ 2
$\overline{Q}_1$ 3
$Q_0$ 4
$Q_1$ 5
$V_{CC1}$ 6
$V_{CC2}$ 7
$Q_5$ 8
$Q_4$ 9
$\overline{Q}_5$ 10
$\overline{Q}_4$ 11
$\overline{Q}_6$ 12
13 $\overline{Q}_5$
14 $Q_6$
15 $Q_7$
16 $D_3$
17 $D_2$
18 $V_{EE}$
19 $\overline{E}$
20 $D_0$
21 $D_1$
22 $Q_3$
23 $Q_2$
24 $\overline{Q}_3$
CERAMIC DIP
$D_1$ 24, $D_0$ 23, $\overline{E}$ 22, $V_{EE}$ 21, $D_2$ 20, $D_3$ 19
$Q_3$ 1
$Q_2$ 2
$\overline{Q}_3$ 3
$\overline{Q}_2$ 4
$\overline{Q}_0$ 5
$\overline{Q}_1$ 6
18 $Q_5$
17 $Q_6$
16 $\overline{Q}_5$
15 $\overline{Q}_6$
14 $\overline{Q}_4$
13 $\overline{Q}_5$
FLAT PACK
7 $Q_0$, 8 $Q_1$, 9 $V_{CC1}$, 10 $V_{CC2}$, 11 $Q_5$, 12 $Q_4$
(TOP VIEW)
CD09031S

**Figure 1**

### LOGIC SYMBOL


(6) 9
(7) 10
$V_{CC1}$
$V_{CC2}$
(20) 23 $D_0$
(21) 24 $D_1$
(17) 20 $D_2$
(16) 19 $D_3$
(19) 22 $\overline{E}$
$\overline{Q}_0$ 5 (2)
$\overline{Q}_1$ 6 (3)
$Q_0$ 7 (4)
$Q_1$ 8 (5)
$\overline{Q}_2$ 4 (1)
$\overline{Q}_3$ 3 (24)
$Q_2$ 2 (23)
$Q_3$ 1 (22)
$\overline{Q}_4$ 14 (11)
$\overline{Q}_5$ 13 (10)
$Q_4$ 12 (9)
$Q_5$ 11 (8)
$\overline{Q}_6$ 15 (12)
$\overline{Q}_7$ 16 (13)
$Q_6$ 17 (14)
$Q_7$ 18 (15)
$V_{EE}$
21 (18)

Pin connections for Flat Pack and in ( ) for Ceramic DIP package

LD05121S

**Figure 2**

## FUNCTION TABLE (One Gate)

| INPUTS | | OUTPUTS | | | |
|---|---|---|---|---|---|
| $D_0$ | E | $\overline{Q}_0$ | $\overline{Q}_1$ | $Q_0$ | $Q_1$ |
| H | X | L | L | H | H |
| X | H | L | L | H | H |
| L | L | H | H | L | L |

Positive Logic:
H = HIGH state (more positive voltage) = 1
L = LOW state (less positive voltage) = 0
X = Don't Care

## ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | 100K ECL | UNIT |
|---|---|---|---|
| $V_{EE}$ | Supply voltage $V_{CC1} = V_{CC2}$ = GND | −7.0 to 0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | $V_{EE}$ to +0.5 | V |
| $I_O$ | Output source current | −55 | mA |
| $T_S$ | Storage temperature | −65 to +150 | °C |
| $T_J$ | Maximum junction temperature | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | | 100K ECL | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | −4.2 | −4.5 | −4.8 | V |
| $V_{EE}$ | Supply voltage (negative) when operating with 10K ECL family | | | | | −5.7 | V |
| $V_{IH}$ | HIGH level input voltage | $V_{CC1} = V_{CC2}$ = GND<br>$T_A$ = 0°C to +85°C | $V_{EE}$ = −4.2V | −1150 | | −880 | mV |
| | | | $V_{EE}$ = −4.5V | −1165 | | | |
| | | | $V_{EE}$ = −4.8V | | | | |
| $V_{IHT}$ | HIGH level input threshold voltage | | $V_{EE}$ = −4.2V | −1150 | | | mV |
| | | | $V_{EE}$ = −4.5V | −1165 | | | mV |
| | | | $V_{EE}$ = −4.8V | | | | |
| $V_{ILT}$ | LOW level input threshold voltage | | $V_{EE}$ = −4.2V | | | −1475 | mV |
| | | | $V_{EE}$ = −4.5V | | | | |
| | | | $V_{EE}$ = −4.8V | | | −1490 | mV |
| $V_{IL}$ | LOW level input voltage | | $V_{EE}$ = −4.2V | −1810 | | −1475 | mV |
| | | | $V_{EE}$ = −4.5V | | | | |
| | | | $V_{EE}$ = −4.8V | | | −1490 | |
| $T_A$ | Operating ambient temperature | | | 0 | +25 | +85 | °C |

**NOTE:**
When operating at other than specified voltages (−4.2V, −4.5V, −4.8V) DC & AC Characteristics will vary slightly from specified values.

## DC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$, $T_A = 0°C$ to $+85°C$ unless otherwise specified[1, 3]

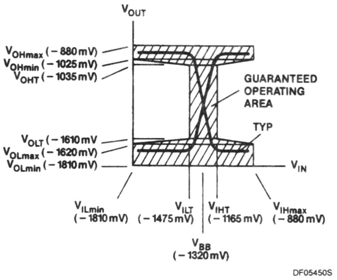
| PARAMETER | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] | |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | $V_{EE} = -4.2V$ | −1025 | | −870 | mV | $V_{IN} = V_{IHmax}$<br>or<br>$V_{IN} = V_{ILmin}$ | Loading with<br>50Ω to −2.0V ±0.010V |
| | | $V_{EE} = -4.5V$ | −1025 | −955 | −880 | mV | | |
| | | $V_{EE} = -4.8V$ | −1035 | | −880 | mV | | |
| $V_{OHT}$ | HIGH level output threshold voltage | $V_{EE} = -4.2V$ | −1035 | | | mV | $V_{IN} = V_{IHmin}$<br>or<br>$V_{IN} = V_{ILmax}$ | |
| | | $V_{EE} = -4.5V$ | −1035 | | | mV | | |
| | | $V_{EE} = -4.8V$ | −1045 | | | mV | | |
| $V_{OLT}$ | LOW level output threshold voltage | $V_{EE} = -4.2V$ | | | −1590 | mV | $V_{IN} = V_{IHmin}$<br>or<br>$V_{IN} = V_{ILmax}$ | |
| | | $V_{EE} = -4.5V$ | | | −1610 | mV | | |
| | | $V_{EE} = -4.8V$ | | | −1610 | mV | | |
| $V_{OL}$ | LOW level output voltage | $V_{EE} = -4.2V$ | −1810 | | −1600 | mV | $V_{IN} = V_{IHmax}$<br>or<br>$V_{IN} = V_{ILmin}$ | |
| | | $V_{EE} = -4.5V$ | −1810 | −1705 | −1620 | mV | | |
| | | $V_{EE} = -4.8V$ | −1830 | | −1620 | mV | | |
| $I_{IH}$ | HIGH level input current | $D_n$ inputs | | | 550 | µA | $V_{IN} = V_{IHmax}$ | |
| | | E input | | | 450 | µA | | |
| $I_{IL}$ | LOW level input current | | 0.5 | | | µA | $V_{IN} = V_{ILmin}$ | |
| $-I_{EE}$ | $V_{EE}$ supply current | | 51 | 73 | 106 | mA | Inputs open | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | $V_{EE} = -4.2V$<br>$T_A = +25°C$ | | | 0.025 | V/V | | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | | 0.05 | V/V | | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 3.

## Driver

## 100112



**NOTES:**

$V_{IHmax}$ – Maximum HIGH level input voltage (the most positive $V_{IH}$).

$V_{IHT}$ – HIGH level input threshold voltage.

$V_{ILT}$ – LOW level input threshold voltage.

$V_{ILmin}$ – Minimum LOW level input voltage (the most negative $V_{IL}$).

$V_{OHmax}$ – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition.

$V_{OHmin}$ – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition.

$V_{OHT}$ – HIGH level output threshold voltage with the inputs set to their respective threshold levels.

$V_{OLT}$ – LOW level output threshold voltage with the inputs set to their respective threshold levels.

$V_{OLmax}$ – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions.

$V_{OLmin}$ – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions.

$V_{BB}$ – Reference Bias voltage. The internally generated reference voltage which is used to set the input and output threshold level.

**Figure 3. Transfer Characteristics**

## AC ELECTRICAL CHARACTERISTICS

### Ceramic DIP $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 0.45 | 1.40 | 0.45 | 1.35 | 0.45 | 1.40 | ns | Figs. 4, 5, 6 |
| $t_{PHL}$ | $D_n$ to $Q_n$, $\overline{Q}_n$ | 0.45 | 1.40 | 0.45 | 1.35 | 0.45 | 1.40 | ns | |
| $t_{PLH}$ | Propagation delay | 0.55 | 1.90 | 0.55 | 1.90 | 0.55 | 1.90 | ns | |
| $t_{PHL}$ | E to $Q_n$, $\overline{Q}_n$ | 0.55 | 1.90 | 0.55 | 1.90 | 0.55 | 1.90 | ns | |
| $t_{TLH}$ | Transition time | 0.45 | 1.50 | 0.45 | 1.40 | 0.45 | 1.50 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.50 | 0.45 | 1.40 | 0.45 | 1.50 | ns | |

### Ceramic DIP $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V \pm 5\%$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 0.45 | 1.40 | 0.45 | 1.35 | 0.45 | 1.40 | ns | Figs. 4, 5, 6 |
| $t_{PHL}$ | $D_n$ to $Q_n$, $\overline{Q}_n$ | 0.45 | 1.40 | 0.45 | 1.35 | 0.45 | 1.40 | ns | |
| $t_{PLH}$ | Propagation delay | 0.55 | 1.90 | 0.55 | 1.90 | 0.55 | 1.90 | ns | |
| $t_{PHL}$ | E to $Q_n$, $\overline{Q}_n$ | 0.55 | 1.90 | 0.55 | 1.90 | 0.55 | 1.90 | ns | |
| $t_{TLH}$ | Transition time | 0.45 | 1.50 | 0.45 | 1.40 | 0.45 | 1.50 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.50 | 0.45 | 1.40 | 0.45 | 1.50 | ns | |

### Flat Pack $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 0.45 | 1.20 | 0.45 | 1.15 | 0.45 | 1.20 | ns | Figs. 4, 5, 6 |
| $t_{PHL}$ | $D_n$ to $Q_n$ | 0.45 | 1.20 | 0.45 | 1.15 | 0.45 | 1.20 | ns | |
| $t_{PLH}$ | Propagation delay | 0.55 | 1.70 | 0.55 | 1.70 | 0.55 | 1.70 | ns | |
| $t_{PHL}$ | E to $Q_n$, $\overline{Q}_n$ | 0.55 | 1.70 | 0.55 | 1.70 | 0.55 | 1.70 | ns | |
| $t_{TLH}$ | Transition time | 0.45 | 1.50 | 0.45 | 1.40 | 0.45 | 1.50 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.50 | 0.45 | 1.40 | 0.45 | 1.50 | ns | |

## AC ELECTRICAL CHARACTERISTICS

**Flat Pack** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V \pm 5\%$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 0.45 | 1.20 | 0.45 | 1.15 | 0.45 | 1.20 | ns | Figs. 4, 5, 6 |
| $t_{PHL}$ | $D_n$ to $Q_n$ | 0.45 | 1.20 | 0.45 | 1.15 | 0.45 | 1.20 | ns | |
| $t_{PLH}$ | Propagation delay | 0.55 | 1.70 | 0.55 | 1.70 | 0.55 | 1.70 | ns | |
| $t_{PHL}$ | E to $Q_n$, $\overline{Q}_n$ | 0.55 | 1.70 | 0.55 | 1.70 | 0.55 | 1.70 | ns | |
| $t_{TLH}$ | Transition time | 0.45 | 1.50 | 0.45 | 1.40 | 0.45 | 1.50 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.50 | 0.45 | 1.40 | 0.45 | 1.50 | ns | |

## AC WAVEFORMS

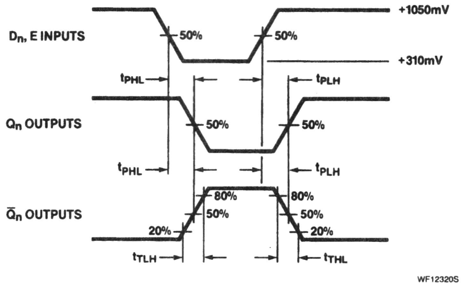
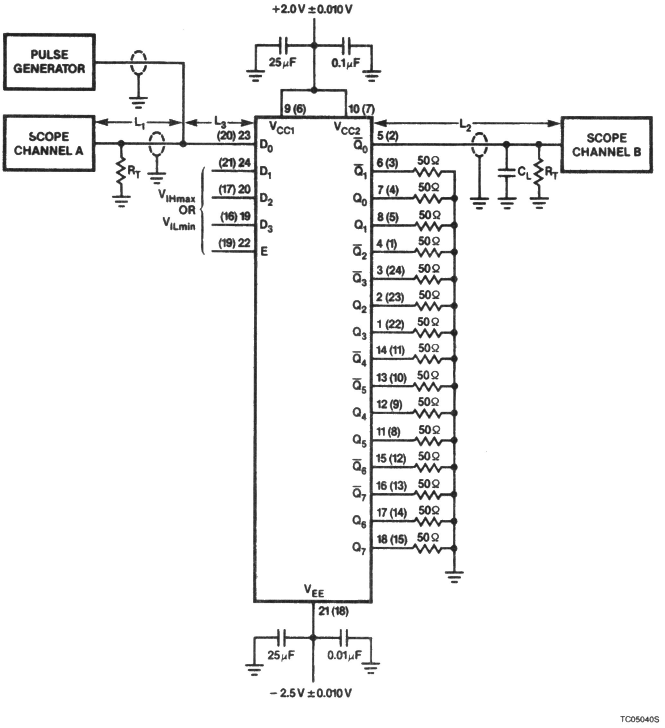

+1050mV
$D_n$, E INPUTS
50%
50%
+310mV
$t_{PHL}$
$t_{PLH}$
$Q_n$ OUTPUTS
50%
50%
$t_{PHL}$
$t_{PLH}$
80%
80%
$\overline{Q}_n$ OUTPUTS
50%
50%
20%
20%
$t_{TLH}$
$t_{THL}$
WF12320S

Figure 4. Propagation Delay and Transition Times

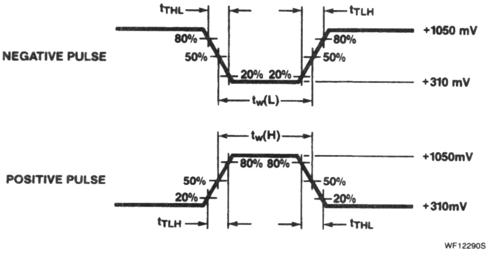
## TEST CIRCUITS AND WAVEFORMS


+2.0V ±0.010V
25μF
0.1μF
PULSE GENERATOR
SCOPE CHANNEL A
SCOPE CHANNEL B
L1
L2
L3
$R_T$
$C_L$
$V_{IHmax}$ OR $V_{ILmin}$
9 (6)
10 (7)
(20) 23
(21) 24
(17) 20
(16) 19
(19) 22
$V_{CC1}$
$V_{CC2}$
$D_0$
$D_1$
$D_2$
$D_3$
E
$\bar{Q}_0$ 5 (2)
$\bar{Q}_1$ 6 (3)
$Q_0$ 7 (4)
$Q_1$ 8 (5)
$\bar{Q}_2$ 4 (1)
$\bar{Q}_3$ 3 (24)
$Q_2$ 2 (23)
$Q_3$ 1 (22)
$\bar{Q}_4$ 14 (11)
$\bar{Q}_5$ 13 (10)
$Q_4$ 12 (9)
$Q_5$ 11 (8)
$\bar{Q}_6$ 15 (12)
$\bar{Q}_7$ 16 (13)
$Q_6$ 17 (14)
$Q_7$ 18 (15)
50Ω
$V_{EE}$
21 (18)
25μF
0.01μF
−2.5V ±0.010V
TC05040S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1μF and 25μF from GND to $V_{CC}$, 0.01μF and 25μF from GND to $V_{EE}$. (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance ≤ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ±1% or better.
11. Pin connections are for Flat Pack and in parentheses for Ceramic DIP package.

Figure 5. Test Circuit


NEGATIVE PULSE
POSITIVE PULSE
$t_{THL}$
$t_{TLH}$
80%
50%
20%
$t_w(L)$
$t_w(H)$
+1050 mV
+310 mV
+1050mV
+310mV
WF12290S

| INPUT PULSE REQUIREMENTS<br>$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -2.5V \pm 0.010V$, $V_T$ = GND (0V) | | | | | |
|---|---|---|---|---|---|
| Family | Amplitude | Rep Rate | Pulse Width | $t_{TLH}$ | $t_{THL}$ |
| 100K ECL | 740mVp-p | 1MHz | 500ns | 0.7 ±0.1ns | 0.7 ±0.1ns |

Figure 6. Input Pulse Definition

**Signetics**

# 100113
## Driver

**Quad Driver (High-Speed)**
***Product Specification***

**ECL Products**

### DESCRIPTION

The 100113 has four 2-input OR-NOR Gates, with one enable input. Each gate has two OR outputs and two NOR outputs.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 100113 | 0.80ns | 75mA |
| | Enable input 1.4ns | |

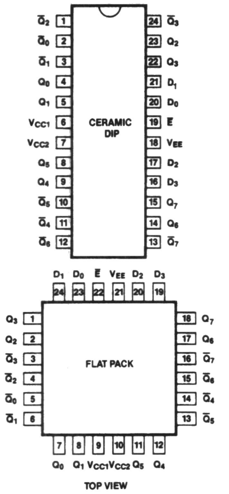
### ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} = \text{GND}$; $V_{EE} = -4.2\text{V}$ to $-4.8\text{V}$<br>$T_A = 0°\text{C}$ to $+85°\text{C}$ |
|---|---|
| Ceramic DIP | 100113F |
| Ceramic Flat Pack | 100113Y |

### PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_0 - D_3$ | Data Inputs |
| $\overline{E}$ | Enable Input |
| $Q_0 - Q_7$ | Data Outputs (OR) |
| $\overline{Q}_0 - \overline{Q}_7$ | Data Outputs (NOR) |

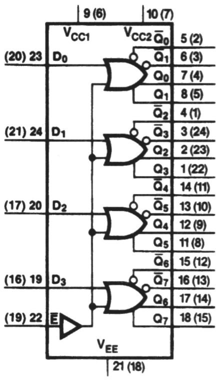
### PIN CONFIGURATION



CERAMIC DIP
Q̄2 1
Q̄0 2
Q̄1 3
Q0 4
Q1 5
VCC1 6
VCC2 7
Q5 8
Q4 9
Q̄5 10
Q̄4 11
Q̄6 12
13 Q̄7
14 Q6
15 Q7
16 D3
17 D2
18 VEE
19 E
20 D0
21 D1
22 Q3
23 Q2
24 Q̄3
FLAT PACK
D1 24
D0 23
Ē 22
VEE 21
D2 20
D3 19
Q3 1
Q2 2
Q̄3 3
Q̄2 4
Q̄0 5
Q̄1 6
7 Q0
8 Q1
9 VCC1
10 VCC2
11 Q5
12 Q4
18 Q7
17 Q6
16 Q̄7
15 Q̄6
14 Q̄4
13 Q̄5
TOP VIEW
CD09051S

Figure 1

### LOGIC SYMBOL



9 (6)
10 (7)
VCC1
VCC2
(20) 23 D0
(21) 24 D1
(17) 20 D2
(16) 19 D3
(19) 22 Ē
Q̄0 5 (2)
Q̄1 6 (3)
Q0 7 (4)
Q1 8 (5)
Q̄2 4 (1)
Q̄3 3 (24)
Q2 2 (23)
Q3 1 (22)
Q̄4 14 (11)
Q̄5 13 (10)
Q4 12 (9)
Q5 11 (8)
Q̄6 15 (12)
Q̄7 16 (13)
Q6 17 (14)
Q7 18 (15)
VEE
21 (18)

Pin connections for Flat Pack and in ( ) for Ceramic Dip package

LD05131S

Figure 2

## TRUTH TABLE (One Gate)

| INPUTS | | OUTPUTS | | | |
|---|---|---|---|---|---|
| $D_0$ | E | $\overline{Q}_0$ | $\overline{Q}_1$ | $Q_0$ | $Q_1$ |
| H | X | L | L | H | H |
| X | H | L | L | H | H |
| L | L | H | H | L | L |

Positive Logic:
H = HIGH state (more positive voltage) = 1
L = LOW state (less positive voltage) = 0
X = Don't Care

## ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| | PARAMETER | 100K ECL | UNIT |
|---|---|---|---|
| $V_{EE}$ | Supply voltage ($V_{CC1} = V_{CC2}$ = GND) | −7.0 to 0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | $V_{EE}$ to +0.5 | V |
| $I_O$ | Output source current | −55 | mA |
| $T_S$ | Storage temperature | −65 to +150 | °C |
| $T_J$ | Maximum junction temperature | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | | 100K ECL | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | −4.2 | −4.5 | −4.8 | V |
| $V_{EE}$ | Supply voltage (negative) when operating with 10K ECL family | | | | | −5.7 | V |
| $V_{IH}$ | HIGH level input voltage | $V_{CC1} = V_{CC2}$ = GND<br>$T_A$ = 0°C to +85°C | $V_{EE}$ = −4.2V | −1150 | | −880 | mV |
| | | | $V_{EE}$ = −4.5V | −1165 | | | |
| | | | $V_{EE}$ = −4.8V | | | | |
| $V_{IHT}$ | HIGH level input threshold voltage | | $V_{EE}$ = −4.2V | −1150 | | | mV |
| | | | $V_{EE}$ = −4.5V | −1165 | | | mV |
| | | | $V_{EE}$ = −4.8V | | | | |
| $V_{ILT}$ | LOW level input threshold voltage | | $V_{EE}$ = −4.2V | | | −1475 | mV |
| | | | $V_{EE}$ = −4.5V | | | | |
| | | | $V_{EE}$ = −4.8V | | | −1490 | mV |
| $V_{IL}$ | LOW level input voltage | | $V_{EE}$ = −4.2V | −1810 | | −1475 | mV |
| | | | $V_{EE}$ = −4.5V | | | | |
| | | | $V_{EE}$ = −4.8V | | | −1490 | |
| $T_A$ | Operating ambient temperature | | | 0 | +25 | +85 | °C |

**NOTE:**
When operating at other than specified voltages (−4.2V, −4.5V, −4.8V) DC & AC Characteristics will vary slightly from specified values.

## Driver

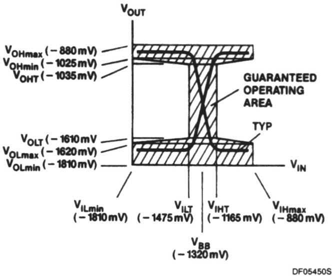
## 100113

**DC ELECTRICAL CHARACTERISTICS** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$, $T_A = 0°C$ to $+85°C$ unless otherwise specified[1,3]

| PARAMETER | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] | |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | $V_{EE} = -4.2V$ | −1025 | | −870 | mV | $V_{IN} = V_{IHmax}$<br>or<br>$V_{IN} = V_{ILmin}$ | Loading with $50\Omega$ to $-2.0V \pm 0.010V$ |
| | | $V_{EE} = -4.5V$ | −1025 | −955 | −880 | mV | | |
| | | $V_{EE} = -4.8V$ | −1035 | | −880 | mV | | |
| $V_{OHT}$ | HIGH level output threshold voltage | $V_{EE} = -4.2V$ | −1035 | | | mV | $V_{IN} = V_{IHmin}$<br>or<br>$V_{IN} = V_{ILmax}$ | |
| | | $V_{EE} = -4.5V$ | −1035 | | | mV | | |
| | | $V_{EE} = -4.8V$ | −1045 | | | mV | | |
| $V_{OLT}$ | LOW level output threshold voltage | $V_{EE} = -4.2V$ | | | −1590 | mV | $V_{IN} = V_{IHmin}$<br>or<br>$V_{IN} = V_{ILmax}$ | |
| | | $V_{EE} = -4.5V$ | | | −1610 | mV | | |
| | | $V_{EE} = -4.8V$ | | | −1610 | mV | | |
| $V_{OL}$ | LOW level output voltage | $V_{EE} = -4.2V$ | −1810 | | −1600 | mV | $V_{IN} = V_{IHmax}$<br>or<br>$V_{IN} = V_{ILmin}$ | |
| | | $V_{EE} = -4.5V$ | −1810 | −1705 | −1620 | mV | | |
| | | $V_{EE} = -4.8V$ | −1830 | | −1620 | mV | | |
| $I_{IH}$ | HIGH level input current | $D_n$ input | | | 550 | μA | $V_{IN} = V_{IHmax}$ | |
| | | E input | | | 450 | μA | | |
| $I_{IL}$ | LOW level input current | | 0.5 | | | μA | $V_{IN} = V_{ILmin}$ | |
| $-I_{EE}$ | $V_{EE}$ supply current | | 54 | 75 | 116 | mA | Inputs open | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | $V_{EE} = -4.2V$<br>$T_A = +25°C$ | | | 0.025 | V/V | | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | | 0.05 | V/V | | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 3.



**NOTES:**

$V_{IHmax}$ – Maximum HIGH level input voltage (the most positive $V_{IH}$).
$V_{IHT}$ – HIGH level input threshold voltage.
$V_{ILT}$ – LOW level input threshold voltage.
$V_{ILmin}$ – Minimum LOW level input voltage (the most negative $V_{IL}$).
$V_{OHmax}$ – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition.
$V_{OHmin}$ – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition.
$V_{OHT}$ – HIGH level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLT}$ – LOW level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLmax}$ – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions.
$V_{OLmin}$ – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions.
$V_{BB}$ – Reference Bias voltage. The internally generated reference voltage which is used to set the input and output threshold level.

Figure 3. Transfer Characteristics

## AC ELECTRICAL CHARACTERISTICS

### Ceramic DIP $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 0.45 | 1.40 | 0.45 | 1.35 | 0.45 | 1.40 | ns | Figs. 4, 5, 6 |
| $t_{PHL}$ | $D_n$ to $Q_n$, $\overline{Q}_n$ | 0.45 | 1.40 | 0.45 | 1.35 | 0.45 | 1.40 | ns | |
| $t_{PLH}$ | Propagation delay | 0.55 | 1.90 | 0.55 | 1.90 | 0.55 | 1.90 | ns | |
| $t_{PHL}$ | E to $Q_n$, $\overline{Q}_n$ | 0.55 | 1.90 | 0.55 | 1.90 | 0.55 | 1.90 | ns | |
| $t_{TLH}$ | Transition time | 0.45 | 1.50 | 0.45 | 1.40 | 0.45 | 1.50 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.50 | 0.45 | 1.40 | 0.45 | 1.50 | ns | |

### Ceramic DIP $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V \pm 5\%$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 0.45 | 1.40 | 0.45 | 1.35 | 0.45 | 1.40 | ns | Figs. 4, 5, 6 |
| $t_{PHL}$ | $D_n$ to $Q_n$, $\overline{Q}_n$ | 0.45 | 1.40 | 0.45 | 1.35 | 0.45 | 1.40 | ns | |
| $t_{PLH}$ | Propagation delay | 0.55 | 1.90 | 0.55 | 1.90 | 0.55 | 1.90 | ns | |
| $t_{PHL}$ | E to $Q_n$, $\overline{Q}_n$ | 0.55 | 1.90 | 0.55 | 1.90 | 0.55 | 1.90 | ns | |
| $t_{TLH}$ | Transition time | 0.45 | 1.50 | 0.45 | 1.40 | 0.45 | 1.50 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.50 | 0.45 | 1.40 | 0.45 | 1.50 | ns | |

### Flat Pack $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 0.45 | 1.20 | 0.45 | 1.15 | 0.45 | 1.20 | ns | Figs. 4, 5, 6 |
| $t_{PHL}$ | $D_n$ to $Q_n$, $\overline{Q}_n$ | 0.45 | 1.20 | 0.45 | 1.15 | 0.45 | 1.20 | ns | |
| $t_{PLH}$ | Propagation delay | 0.55 | 1.70 | 0.55 | 1.70 | 0.55 | 1.70 | ns | |
| $t_{PHL}$ | E to $Q_n$, $\overline{Q}_n$ | 0.55 | 1.70 | 0.55 | 1.70 | 0.55 | 1.70 | ns | |
| $t_{TLH}$ | Transition time | 0.45 | 1.50 | 0.45 | 1.40 | 0.45 | 1.50 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.50 | 0.45 | 1.40 | 0.45 | 1.50 | ns | |

# Driver

# 100113

## AC ELECTRICAL CHARACTERISTICS

**Flat Pack** $V_{CC1} = V_{CC2} = \text{GND}$, $V_{EE} = -5.2V \pm 5\%$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 0.45 | 1.20 | 0.45 | 1.15 | 0.45 | 1.20 | ns | Figs. 4, 5, 6 |
| $t_{PHL}$ | $D_n$ to $Q_n$, $\overline{Q}_n$ | 0.45 | 1.20 | 0.45 | 1.15 | 0.45 | 1.20 | ns | |
| $t_{PLH}$ | Propagation delay | 0.55 | 1.70 | 0.55 | 1.70 | 0.55 | 1.70 | ns | |
| $t_{PHL}$ | E to $Q_n$, $\overline{Q}_n$ | 0.55 | 1.70 | 0.55 | 1.70 | 0.55 | 1.70 | ns | |
| $t_{TLH}$ | Transition time | 0.45 | 1.50 | 0.45 | 1.40 | 0.45 | 1.50 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.50 | 0.45 | 1.40 | 0.45 | 1.50 | ns | |

## AC WAVEFORMS

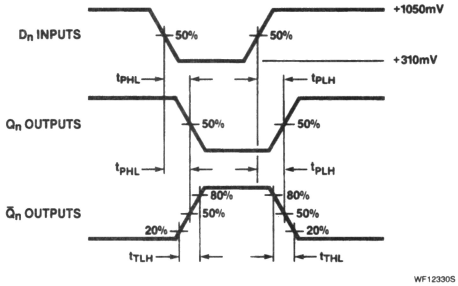
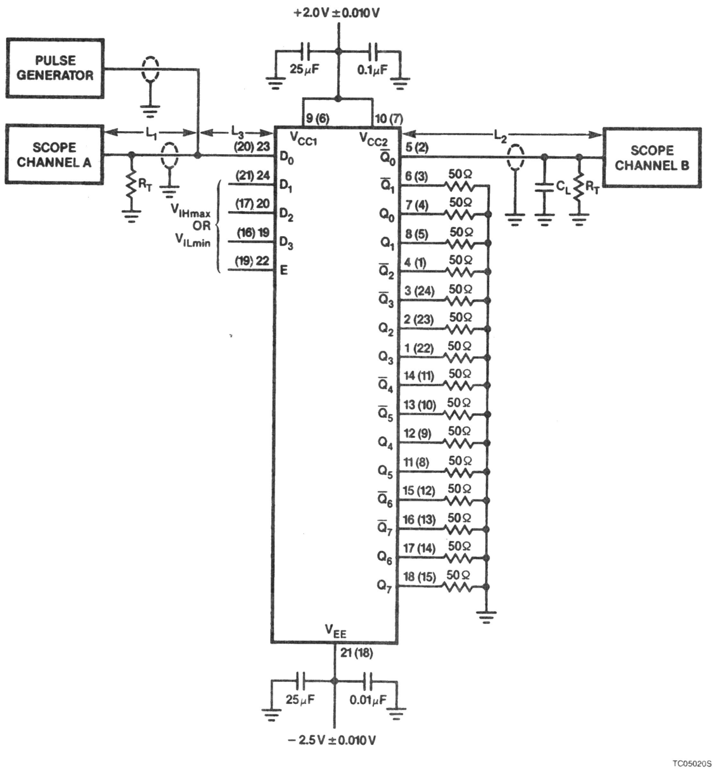

D_n INPUTS
Q_n OUTPUTS
Q̄_n OUTPUTS
+1050mV
+310mV
50%
50%
t_PHL
t_PLH
50%
50%
t_PHL
t_PLH
80%
50%
20%
80%
50%
20%
t_TLH
t_THL
WF12330S

Figure 4. Propagation Delay and Transition Times

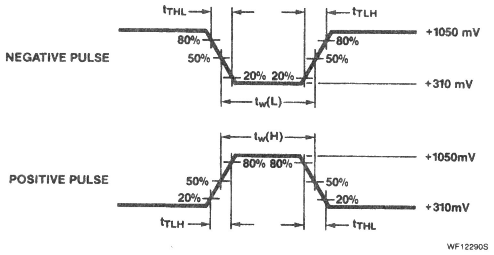
## TEST CIRCUITS AND WAVEFORMS


+2.0V ±0.010V
25µF
0.1µF
PULSE GENERATOR
SCOPE CHANNEL A
SCOPE CHANNEL B
L1
L2
L3
R_T
C_L
V_IHmax OR V_ILmin
9 (6)
10 (7)
V_CC1
V_CC2
(20) 23 D0
(21) 24 D1
(17) 20 D2
(16) 19 D3
(19) 22 E
5 (2) Q̄0
6 (3) Q̄1
7 (4) Q0
8 (5) Q1
4 (1) Q̄2
3 (24) Q̄3
2 (23) Q2
1 (22) Q3
14 (11) Q̄4
13 (10) Q̄5
12 (9) Q4
11 (8) Q5
15 (12) Q̄6
16 (13) Q̄7
17 (14) Q6
18 (15) Q7
50Ω
V_EE
21 (18)
25µF
0.01µF
−2.5V ±0.010V
TC05020S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1µF and 25µF from GND to $V_{CC}$, 0.01µF and 25µF from GND to $V_{EE}$. (0.01 and 0.1µF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance ⩽ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.
11. Pin connections are for Flat Pack and in parentheses for Ceramic DIP package.

Figure 5. Test Circuit


NEGATIVE PULSE
$t_{THL}$
$t_{TLH}$
80%
50%
20%
20%
80%
50%
+1050 mV
+310 mV
$t_w(L)$
POSITIVE PULSE
$t_w(H)$
80%
80%
50%
20%
50%
20%
+1050mV
+310mV
$t_{TLH}$
$t_{THL}$
WF12290S

| INPUT PULSE REQUIREMENTS<br>$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -2.5V \pm 0.010V$, $V_T$ = GND (0V) | | | | | |
|---|---|---|---|---|---|
| Family | Amplitude | Rep Rate | Pulse Width | $t_{TLH}$ | $t_{THL}$ |
| 100K ECL | 740mVp-p | 1MHz | 500ns | 0.7 ±0.1ns | 0.7 ±0.1ns |

Figure 6. Input Pulse Definition

# 100114
## Line Receiver

**Quint Differential Line Receiver**
***Product Specification***

**ECL Products**

### DESCRIPTION

The 100114 contains five gates with differential inputs and complementary outputs. An internal reference bias is available ($V_{BB}$), which enables, when connected to a gate input, the other to operate as a standard 100K ECL input. The direct output of a gate goes LOW, and the complementary one goes HIGH when both inputs are either open, or at $V_{CC}$, or have equal voltage applied.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 100114 | 1.40ns | 73mA |

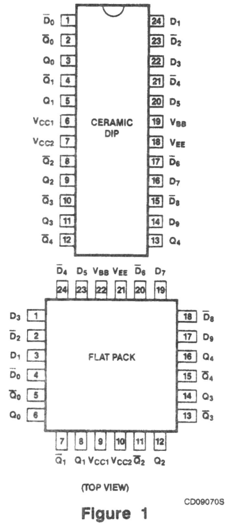
### ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} = GND$; $V_{EE} = -4.2V$ to $-4.8V$<br>$T_A = 0°C$ to $+85°C$ |
|---|---|
| Ceramic DIP | 100114F |
| Ceramic Flat Pack | 100114Y |

### PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_1$, $D_3$, $D_5$, $D_7$, $D_9$ | Data Inputs |
| $\overline{D}_0$, $\overline{D}_2$, $\overline{D}_4$, $\overline{D}_6$, $\overline{D}_8$ | Inverting Data Inputs |
| $Q_0 - Q_4$, $\overline{Q}_0 - \overline{Q}_4$ | Data Outputs |

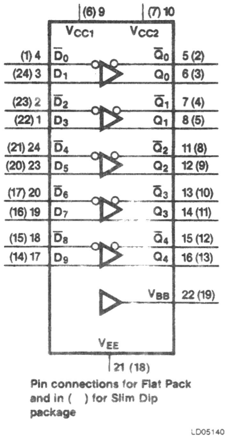
### PIN CONFIGURATION



$\overline{D}_0$ 1
$\overline{Q}_0$ 2
$Q_0$ 3
$\overline{Q}_1$ 4
$Q_1$ 5
$V_{CC1}$ 6
$V_{CC2}$ 7
$\overline{Q}_2$ 8
$Q_2$ 9
$\overline{Q}_3$ 10
$Q_3$ 11
$\overline{Q}_4$ 12
24 $D_1$
23 $\overline{D}_2$
22 $D_3$
21 $\overline{D}_4$
20 $D_5$
19 $V_{BB}$
18 $V_{EE}$
17 $\overline{D}_6$
16 $D_7$
15 $\overline{D}_8$
14 $D_9$
13 $Q_4$
CERAMIC DIP
$\overline{D}_4$ 24, $D_5$ 23, $V_{BB}$ 22, $V_{EE}$ 21, $\overline{D}_6$ 20, $D_7$ 19
$D_3$ 1
$\overline{D}_2$ 2
$D_1$ 3
$\overline{D}_0$ 4
$\overline{Q}_0$ 5
$Q_0$ 6
18 $\overline{D}_8$
17 $D_9$
16 $Q_4$
15 $\overline{Q}_4$
14 $Q_3$
13 $\overline{Q}_3$
FLAT PACK
7 $\overline{Q}_1$, 8 $Q_1$, 9 $V_{CC1}$, 10 $V_{CC2}$, 11 $\overline{Q}_2$, 12 $Q_2$
(TOP VIEW)
CD09070S

Figure 1

### LOGIC SYMBOL



(6) 9
(7) 10
$V_{CC1}$
$V_{CC2}$
(1) 4 $\overline{D}_0$
(24) 3 $D_1$
(23) 2 $\overline{D}_2$
(22) 1 $D_3$
(21) 24 $\overline{D}_4$
(20) 23 $D_5$
(17) 20 $\overline{D}_6$
(16) 19 $D_7$
(15) 18 $\overline{D}_8$
(14) 17 $D_9$
$\overline{Q}_0$ 5 (2)
$Q_0$ 6 (3)
$\overline{Q}_1$ 7 (4)
$Q_1$ 8 (5)
$\overline{Q}_2$ 11 (8)
$Q_2$ 12 (9)
$\overline{Q}_3$ 13 (10)
$Q_3$ 14 (11)
$\overline{Q}_4$ 15 (12)
$Q_4$ 16 (13)
$V_{BB}$ 22 (19)
$V_{EE}$
21 (18)
LD05140S

Pin connections for Flat Pack and in ( ) for Slim Dip package

Figure 2

## FUNCTION TABLE (One Gate)

| INPUTS | | OUTPUTS | |
|---|---|---|---|
| $\overline{D}_0$ | $D_1$ | $\overline{Q}_0$ | $Q_1$ |
| H | $V_{BB}$ | H | L |
| L | $V_{BB}$ | L | H |
| $V_{BB}$ | H | L | H |
| $V_{BB}$ | L | H | L |
| $V_{ID} \geqslant 0V$ | $V_{ID} \geqslant 0V$ | H | L |
| $V_{ID} \leqslant -0.150V$ | $V_{ID} \leqslant -0.150V$ | L | H |
| $-0.150V < V_{ID} < 0V$ | $-0.150V < V_{ID} < 0V$ | * | * |
| open | open | H | L |
| $V_{CC}$ | $V_{CC}$ | H | L |

Positive Logic:
H = HIGH state (more positive voltage) = 1
L = LOW state (less positive voltage) = 0
* = Indeterminate state
$V_{BB}$ = Internal reference pin 22 (18)
$V_{ID}$ = Complement to direct input voltage difference.

## ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| | PARAMETER | 100K ECL | UNIT |
|---|---|---|---|
| $V_{EE}$ | Supply voltage ($V_{CC1} = V_{CC2}$ = GND) | -7.0 to 0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | $V_{EE}$ to +0.5 | V |
| $I_O$ | Output source current | -55 | mA |
| $T_S$ | Storage temperature | -65 to +150 | °C |
| $T_J$ | Maximum junction temperature | +150 | °C |

# Line Receiver

# 100114

## DC OPERATING CONDITIONS

| PARAMETER | | | | 100K ECL | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | −4.2 | −4.5 | −4.8 | V |
| $V_{EE}$ | Supply voltage (negative) when operating with 10K ECL family | | | | | −5.7 | V |
| $V_{IH}$ | HIGH level input voltage | $V_{CC1} = V_{CC2} = GND$<br>$T_A = 0°C$ to $+85°C$ | $V_{EE} = -4.2V$ | −1150 | | −880 | mV |
| | | | $V_{EE} = -4.5V$ | −1165 | | | |
| | | | $V_{EE} = -4.8V$ | | | | |
| $V_{IHT}$ | HIGH level input threshold voltage | | $V_{EE} = -4.2V$ | −1150 | | | mV |
| | | | $V_{EE} = -4.5V$ | −1165 | | | mV |
| | | | $V_{EE} = -4.8V$ | | | | |
| $V_{ILT}$ | LOW level input threshold voltage | | $V_{EE} = -4.2V$ | | | −1475 | mV |
| | | | $V_{EE} = -4.5V$ | | | | |
| | | | $V_{EE} = -4.8V$ | | | −1490 | mV |
| $V_{IL}$ | LOW level input voltage | | $V_{EE} = -4.2V$ | −1810 | | −1475 | mV |
| | | | $V_{EE} = -4.5V$ | | | | |
| | | | $V_{EE} = -4.8V$ | | | −1490 | |
| $V_{IHmax}$ | Minimum permissable HIGH level input voltage | | $V_{EE} = -4.2V$ | | | −230 | mV |
| | | | $V_{EE} = -4.5V$ | | | | |
| | | | $V_{EE} = -4.8V$ | | | | |
| $V_{REFmin}$ | Minimum permissable extended input reference voltage | | $V_{EE} = -4.2V$ | −2300 | | | mV |
| | | | $V_{EE} = -4.5V$ | | | | |
| | | | $V_{EE} = -4.8V$ | | | | |
| $V_{CM}$ | Common mode voltage | $V_{CC1} = V_{CC2} = GND$<br>$T_A = 0°C$ to $+85°C$<br>permissable $\pm V_{CM}$<br>with respect to $V_{BB}$ | $V_{EE} = -4.2V$ | | | 1.0 | V |
| | | | $V_{EE} = -4.5V$ | | | | |
| | | | $V_{EE} = -4.8V$ | | | | |
| $V_{DIFF}$ | Differential input voltage | $V_{CC1} = V_{CC2} = GND$<br>$T_A = 0°C$ to $+85°C$<br>required for full swing output | $V_{EE} = -4.2V$ | 150 | | | mV |
| | | | $V_{EE} = -4.5V$ | | | | |
| | | | $V_{EE} = -4.8V$ | | | | |
| $T_A$ | Operating ambient temperature | | | 0 | +25 | +85 | °C |

**NOTE:**
When operating at other than specified voltages (−4.2V, −4.5V, −4.8V) DC & AC Characteristics will vary slightly from specified values.

## Line Receiver 100114

### DC ELECTRICAL CHARACTERISTICS

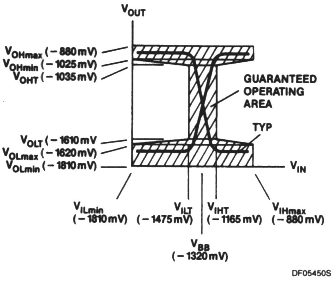
$V_{CC1} = V_{CC2} = GND$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$, $T_A = 0°C$ to $+85°C$ unless otherwise specified[1, 3]

| PARAMETER | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] | |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | $V_{EE} = -4.2V$ | -1025 | | -870 | mV | $V_{IN} = V_{IHmax}$<br>or<br>$V_{IN} = V_{ILmin}$ | Loading with 50Ω to -2.0V ±0.010V |
| | | $V_{EE} = -4.5V$ | -1025 | -955 | -880 | mV | | |
| | | $V_{EE} = -4.8V$ | -1035 | | -880 | mV | | |
| $V_{OHT}$ | HIGH level output threshold voltage | $V_{EE} = -4.2V$ | -1035 | | | mV | $V_{IN} = V_{IHmin}$<br>or<br>$V_{IN} = V_{ILmax}$ | |
| | | $V_{EE} = -4.5V$ | -1035 | | | mV | | |
| | | $V_{EE} = -4.8V$ | -1045 | | | mV | | |
| $V_{OLT}$ | LOW level output threshold voltage | $V_{EE} = -4.2V$ | | | -1590 | mV | $V_{IN} = V_{IHmin}$<br>or<br>$V_{IN} = V_{ILmax}$ | |
| | | $V_{EE} = -4.5V$ | | | -1610 | mV | | |
| | | $V_{EE} = -4.8V$ | | | -1610 | mV | | |
| $V_{OL}$ | LOW level output voltage | $V_{EE} = -4.2V$ | -1810 | | -1600 | mV | $V_{IN} = V_{IHmax}$<br>or<br>$V_{IN} = V_{ILmin}$ | |
| | | $V_{EE} = -4.5V$ | -1810 | -1705 | -1620 | mV | | |
| | | $V_{EE} = -4.8V$ | -1830 | | -1620 | mV | | |
| $V_{BB}$ | Output reference voltage | $V_{EE} = -4.5V$ | -1380 | -1320 | -1260 | mV | $I_{BB} = 0$ to $475\mu A$ | |
| | | $V_{EE} = -4.2V$ to $-4.8V$ | -1396 | -1320 | -1244 | mV | | |
| $I_{IH}$ | HIGH level input current | | | | 65 | μA | $V_{IN} = V_{IHmax}$, second input to $V_{BB}$ | |
| $I_{CBO}$ | Input leakage current | | -10 | | | μA | $V_{IN} = V_{EE}$, second input to $V_{BB}$ | |
| $-I_{EE}$ | $V_{EE}$ supply current | | 51 | 73 | 106 | mA | Inputs open | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | $V_{EE} = -4.2V$<br>$T_A = +25°C$ | | | 0.035 | V/V | | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | | 0.07 | V/V | | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 3.

## Line Receiver 100114



**NOTES:**

| | |
|---|---|
| $V_{IHmax}$ | – Maximum HIGH level input voltage (the most positive $V_{IH}$). |
| $V_{IHT}$ | – HIGH level input threshold voltage. |
| $V_{ILT}$ | – LOW level input threshold voltage. |
| $V_{ILmin}$ | – Minimum LOW level input voltage (the most negative $V_{IL}$). |
| $V_{OHmax}$ | – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition. |
| $V_{OHmin}$ | – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition. |
| $V_{OHT}$ | – HIGH level output threshold voltage with the inputs set to their respective threshold levels. |
| $V_{OLT}$ | – LOW level output threshold voltage with the inputs set to their respective threshold levels. |
| $V_{OLmax}$ | – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions. |
| $V_{OLmin}$ | – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions. |
| $V_{BB}$ | – Reference Bias voltage. The internally generated reference voltage which is used to set the input and output threshold level. |

**Figure 3. Transfer Characteristics**

## AC ELECTRICAL CHARACTERISTICS

**Ceramic DIP** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 0.55 | 2.20 | 0.60 | 2.20 | 0.70 | 2.40 | ns | Figs. 4, 5, 6 |
| $t_{PHL}$ | $D_n$, $\overline{D}_n$ to $Q_n$, $\overline{Q}_n$ | 0.55 | 2.20 | 0.60 | 2.20 | 0.70 | 2.40 | ns | |
| $t_{TLH}$ | Transition time | 0.45 | 1.30 | 0.45 | 1.20 | 0.45 | 1.30 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.30 | 0.45 | 1.20 | 0.45 | 1.30 | ns | |

**Ceramic DIP** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V \pm 5\%$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 0.55 | 2.20 | 0.60 | 2.20 | 0.70 | 2.40 | ns | Figs. 4, 5, 6 |
| $t_{PHL}$ | $D_n$, $\overline{D}_n$ to $Q_n$, $\overline{Q}_n$ | 0.55 | 2.20 | 0.60 | 2.20 | 0.70 | 2.40 | ns | |
| $t_{TLH}$ | Transition time | 0.45 | 1.30 | 0.45 | 1.20 | 0.45 | 1.30 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.30 | 0.45 | 1.20 | 0.45 | 1.30 | ns | |

**Flat Pack** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 0.55 | 2.00 | 0.60 | 2.00 | 0.70 | 2.20 | ns | Figs. 4, 5, 6 |
| $t_{PHL}$ | $D_n$, $\overline{D}_n$ to $Q_n$, $\overline{Q}_n$ | 0.55 | 2.00 | 0.60 | 2.00 | 0.70 | 2.20 | ns | |
| $t_{TLH}$ | Transition time | 0.45 | 1.30 | 0.45 | 1.20 | 0.45 | 1.30 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.30 | 0.45 | 1.20 | 0.45 | 1.30 | ns | |

**Flat Pack** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V \pm 5\%$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 0.55 | 2.00 | 0.60 | 2.00 | 0.70 | 2.20 | ns | Figs. 4, 5, 6 |
| $t_{PHL}$ | $D_n$, $\overline{D}_n$ to $Q_n$, $\overline{Q}_n$ | 0.55 | 2.00 | 0.60 | 2.00 | 0.70 | 2.20 | ns | |
| $t_{TLH}$ | Transition time | 0.45 | 1.30 | 0.45 | 1.20 | 0.45 | 1.30 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.30 | 0.45 | 1.20 | 0.45 | 1.30 | ns | |

## AC WAVEFORMS

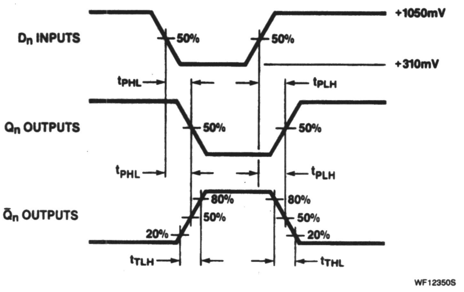
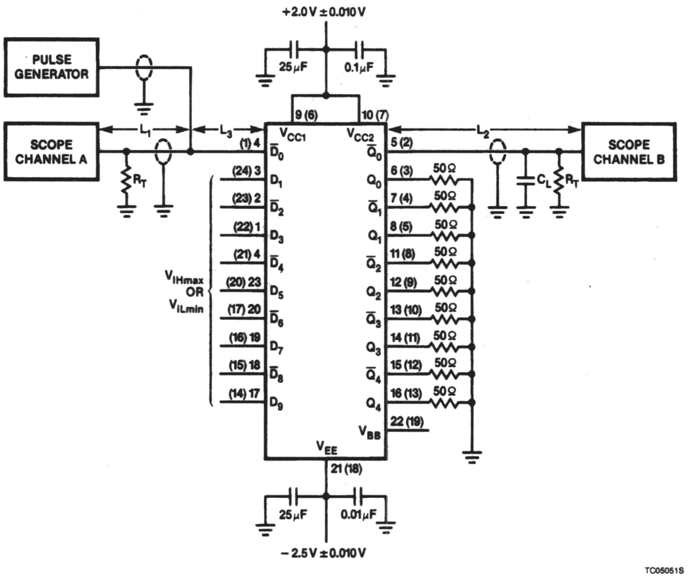

Dn INPUTS
+1050mV
+310mV
50%
50%
tPHL
tPLH
Qn OUTPUTS
50%
50%
tPHL
tPLH
Q̄n OUTPUTS
80%
50%
20%
80%
50%
20%
tTLH
tTHL
WF12350S

Figure 4. Propagation Delay and Transition Times

## TEST CIRCUITS AND WAVEFORMS


+2.0V ±0.010V
25μF
0.1μF
PULSE GENERATOR
SCOPE CHANNEL A
RT
L1
L3
L2
9 (6)
10 (7)
VCC1
VCC2
(1) 4
D̄0
Q̄0
5 (2)
(24) 3
D1
Q0
6 (3)
(23) 2
D̄2
Q̄1
7 (4)
(22) 1
D3
Q1
8 (5)
(21) 4
D̄4
Q̄2
11 (8)
(20) 23
D5
Q2
12 (9)
(17) 20
D̄6
Q̄3
13 (10)
(16) 19
D7
Q3
14 (11)
(15) 18
D̄8
Q̄4
15 (12)
(14) 17
D9
Q4
16 (13)
VBB
22 (19)
VEE
21 (18)
50Ω
VIHmax OR VILmin
SCOPE CHANNEL B
CL
RT
25μF
0.01μF
−2.5V ±0.010V
TC05051S

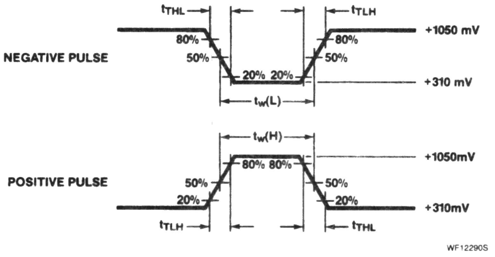
**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1μF and 25μF from GND to $V_{CC}$, 0.01μF and 25μF from GND to $V_{EE}$. (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance ≤ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ±1% or better.
11. Pin connections are for Flat Pack and in parentheses for Ceramic DIP.

Figure 5. Test Circuit

# Line Receiver

# 100114


tTHL
tTLH
NEGATIVE PULSE
80%
50%
20% 20%
80%
50%
+1050 mV
+310 mV
tw(L)
tw(H)
POSITIVE PULSE
50%
20%
80% 80%
50%
20%
+1050mV
+310mV
tTLH
tTHL
WF12290S

| INPUT PULSE REQUIREMENTS<br>$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -2.5V \pm 0.010V$, $V_T$ = GND (0V) | | | | | |
|---|---|---|---|---|---|
| **Family** | **Amplitude** | **Rep Rate** | **Pulse Width** | $t_{TLH}$ | $t_{THL}$ |
| 100K ECL | 740mVp-p | 1MHz | 500ns | 0.7 ±0.1ns | 0.7 ±0.1ns |

Figure 6. Input Pulse Definition

Signetics

# 100117
## Gate

**Triple 1-2-2 Input OR-AND/OR-AND-INVERT Gate**
***Product Specification***

**ECL Products**

### DESCRIPTION

The 100117 has three 1-2-2 input OR/NAND gates with true and complementary outputs.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 100117 | $E_n$ to $Q_n$, $\overline{Q}_n$ 0.75ns | 57mA |
| | $D_n$ to $Q_n$, $\overline{Q}_n$ 1.40ns | |

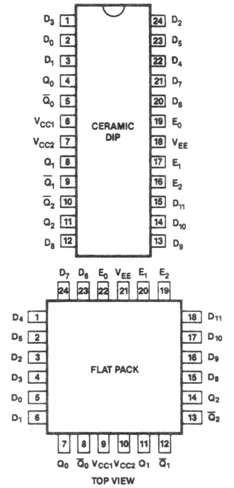
### ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} = \text{GND}$; $V_{EE} = -4.2\text{V}$ to $-4.8\text{V}$<br>$T_A = 0°\text{C}$ to $+85°\text{C}$ |
|---|---|
| Ceramic DIP | 100117F |
| Ceramic Flat Pack | 100117Y |

### PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_0 - D_{11}$ | Data Inputs |
| $E_0 - E_2$ | Enable Inputs |
| $Q_0 - Q_2$, $\overline{Q}_0 - \overline{Q}_2$ | Data Outputs |

### PIN CONFIGURATION

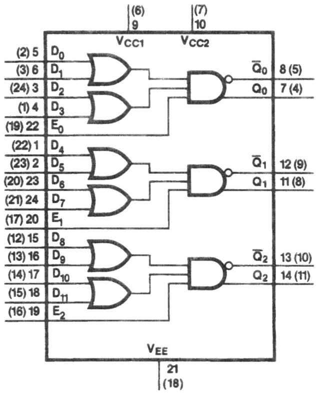


D3 1
D0 2
D1 3
Q0 4
Q̄0 5
VCC1 6
VCC2 7
Q1 8
Q̄1 9
Q̄2 10
Q2 11
D8 12
24 D2
23 D5
22 D4
21 D7
20 D6
19 E0
18 VEE
17 E1
16 E2
15 D11
14 D10
13 D9
CERAMIC DIP
D7 D6 E0 VEE E1 E2
24 23 22 21 20 19
D4 1
D5 2
D2 3
D3 4
D0 5
D1 6
18 D11
17 D10
16 D9
15 D8
14 Q2
13 Q̄2
FLAT PACK
7 8 9 10 11 12
Q0 Q̄0 VCC1 VCC2 Q1 Q̄1
TOP VIEW

CD09090S

Figure 1

### LOGIC SYMBOL



(6) 9
(7) 10
VCC1
VCC2
(2) 5 D0
(3) 6 D1
(24) 3 D2
(1) 4 D3
(19) 22 E0
(22) 1 D4
(23) 2 D5
(20) 23 D6
(21) 24 D7
(17) 20 E1
(12) 15 D8
(13) 16 D9
(14) 17 D10
(15) 18 D11
(16) 19 E2
Q̄0 8 (5)
Q0 7 (4)
Q̄1 12 (9)
Q1 11 (8)
Q̄2 13 (10)
Q2 14 (11)
VEE
21 (18)

Pin connections for Flat Pack and in ( ) for Ceramic DIP package

LD05150S

Figure 2

# Gate 100117

## FUNCTION TABLE (One Gate)

| INPUTS | | | | | OUTPUTS | |
|---|---|---|---|---|---|---|
| $D_4$ | $D_2$ | $D_3$ | $D_0$ | $D_1$ | $\overline{Q}_0$ | $Q_0$ |
| L | X | X | X | X | H | L |
| X | L | L | X | X | H | L |
| X | X | X | L | L | H | L |
| H | H | X | H | X | L | H |
| H | X | H | X | H | L | H |
| H | H | X | X | H | L | H |
| H | X | H | H | X | L | H |

Positive Logic:
H = HIGH state (more positive voltage) = 1
L = LOW state (less positive voltage) = 0
X = Don't Care

## ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | 100K ECL | UNIT |
|---|---|---|---|
| $V_{EE}$ | Supply voltage ($V_{CC1} = V_{CC2} =$ GND) | -7.0 to 0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | $V_{EE}$ to +0.5 | V |
| $I_O$ | Output source current | -55 | mA |
| $T_S$ | Storage temperature | -65 to +150 | °C |
| $T_J$ | Maximum junction temperature | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | | 100K ECL | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | -4.2 | -4.5 | -4.8 | V |
| $V_{EE}$ | Supply voltage (negative) when operating with 10K ECL family | | | | | -5.7 | V |
| $V_{IH}$ | HIGH level input voltage | $V_{CC1} = V_{CC2} =$ GND<br>$T_A$ = 0°C to +85°C | $V_{EE} = -4.2V$ | -1150 | | -880 | mV |
| | | | $V_{EE} = -4.5V$ | -1165 | | | |
| | | | $V_{EE} = -4.8V$ | | | | |
| $V_{IHT}$ | HIGH level input threshold voltage | | $V_{EE} = -4.2V$ | -1150 | | | mV |
| | | | $V_{EE} = -4.5V$ | -1165 | | | mV |
| | | | $V_{EE} = -4.8V$ | | | | |
| $V_{ILT}$ | LOW level input threshold voltage | | $V_{EE} = -4.2V$ | | | -1475 | mV |
| | | | $V_{EE} = -4.5V$ | | | | |
| | | | $V_{EE} = -4.8V$ | | | -1490 | mV |
| $V_{IL}$ | LOW level input voltage | | $V_{EE} = -4.2V$ | -1810 | | -1475 | mV |
| | | | $V_{EE} = -4.5V$ | | | | |
| | | | $V_{EE} = -4.8V$ | | | -1490 | |
| $T_A$ | Operating ambient temperature | | | 0 | +25 | +85 | °C |

**NOTE:**
When operating at other than specified voltages (-4.2V, -4.5V, -4.8V) DC & AC Characteristics will vary slightly from specified values.

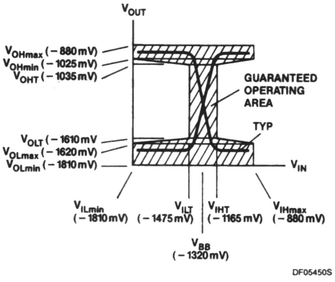
## DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2} = GND$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$, $T_A = 0°C$ to $+85°C$ unless otherwise specified[1, 3]

| PARAMETER | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] | |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | $V_{EE} = -4.2V$ | −1025 | | −870 | mV | $V_{IN} = V_{IHmax}$<br>or<br>$V_{IN} = V_{ILmin}$ | Loading with 50Ω to −2.0V ±0.010V |
| | | $V_{EE} = -4.5V$ | −1025 | −955 | −880 | mV | | |
| | | $V_{EE} = -4.8V$ | −1035 | | −880 | mV | | |
| $V_{OHT}$ | HIGH level output threshold voltage | $V_{EE} = -4.2V$ | −1035 | | | mV | $V_{IN} = V_{IHmin}$<br>or<br>$V_{IN} = V_{ILmax}$ | |
| | | $V_{EE} = -4.5V$ | −1035 | | | mV | | |
| | | $V_{EE} = -4.8V$ | −1045 | | | mV | | |
| $V_{OLT}$ | LOW level output threshold voltage | $V_{EE} = -4.2V$ | | | −1590 | mV | $V_{IN} = V_{IHmin}$<br>or<br>$V_{IN} = V_{ILmax}$ | |
| | | $V_{EE} = -4.5V$ | | | −1610 | mV | | |
| | | $V_{EE} = -4.8V$ | | | −1610 | mV | | |
| $V_{OL}$ | LOW level output voltage | $V_{EE} = -4.2V$ | −1810 | | −1600 | mV | $V_{IN} = V_{IHmax}$<br>or<br>$V_{IN} = V_{ILmin}$ | |
| | | $V_{EE} = -4.5V$ | −1810 | −1705 | −1620 | mV | | |
| | | $V_{EE} = -4.8V$ | −1830 | | −1620 | mV | | |
| $I_{IH}$ | HIGH level input current | $D_4$, $D_9$, $D_{14}$ | | | 350 | μA | $V_{IN} = V_{IHmax}$ | |
| | | Other inputs | | | 220 | μA | | |
| $I_{IL}$ | LOW level input current | | 0.5 | | | μA | $V_{IN} = V_{ILmin}$ | |
| $-I_{EE}$ | $V_{EE}$ supply current | | 37 | 57 | 79 | mA | Inputs open | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | $V_{EE} = -4.2V$<br>$T_A = +25°C$ | | | 0.025 | V/V | | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | | 0.050 | V/V | | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 3.



**NOTES:**

| | |
|---|---|
| $V_{IHmax}$ | – Maximum HIGH level input voltage (the most positive $V_{IH}$). |
| $V_{IHT}$ | – HIGH level input threshold voltage. |
| $V_{ILT}$ | – LOW level input threshold voltage. |
| $V_{ILmin}$ | – Minimum LOW level input voltage (the most negative $V_{IL}$). |
| $V_{OHmax}$ | – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition. |
| $V_{OHmin}$ | – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition. |
| $V_{OHT}$ | – HIGH level output threshold voltage with the inputs set to their respective threshold levels. |
| $V_{OLT}$ | – LOW level output threshold voltage with the inputs set to their respective threshold levels. |
| $V_{OLmax}$ | – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions. |
| $V_{OLmin}$ | – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions. |
| $V_{BB}$ | – Reference bias voltage (the internally generated reference voltage which is used to set the input and output threshold level). |

**Figure 3. Transfer Characteristics**

## AC ELECTRICAL CHARACTERISTICS

### Ceramic DIP $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 0.90 | 2.60 | 0.90 | 2.50 | 0.90 | 2.60 | ns | Figs. 4, 5, 6 |
| $t_{PHL}$ | $D_n$ to $Q_n$, $\overline{Q}_n$ | 0.90 | 2.60 | 0.90 | 2.50 | 0.90 | 2.60 | ns | |
| $t_{PLH}$ | Propagation delay | 0.45 | 1.40 | 0.45 | 1.30 | 0.45 | 1.40 | ns | |
| $t_{PHL}$ | $E_n$ to $Q_n$, $\overline{Q}_n$ | 0.45 | 1.40 | 0.45 | 1.30 | 0.45 | 1.40 | ns | |
| $t_{TLH}$ | Transition time | 0.45 | 1.20 | 0.45 | 1.10 | 0.45 | 1.20 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.20 | 0.45 | 1.10 | 0.45 | 1.20 | ns | |

### Ceramic DIP $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V \pm 5\%$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 0.90 | 2.60 | 0.90 | 2.50 | 0.90 | 2.60 | ns | Figs. 4, 5, 6 |
| $t_{PHL}$ | $D_n$ to $Q_n$, $\overline{Q}_n$ | 0.90 | 2.60 | 0.90 | 2.50 | 0.90 | 2.60 | ns | |
| $t_{PLH}$ | Propagation delay | 0.45 | 1.40 | 0.45 | 1.30 | 0.45 | 1.40 | ns | |
| $t_{PHL}$ | $E_n$ to $Q_n$, $\overline{Q}_n$ | 0.45 | 1.40 | 0.45 | 1.30 | 0.45 | 1.40 | ns | |
| $t_{TLH}$ | Transition time | 0.45 | 1.20 | 0.45 | 1.10 | 0.45 | 1.20 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.20 | 0.45 | 1.10 | 0.45 | 1.20 | ns | |

### Flat Pack $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 0.90 | 2.40 | 0.90 | 2.30 | 0.90 | 2.40 | ns | Figs. 4, 5, 6 |
| $t_{PHL}$ | $D_n$ to $Q_n$, $\overline{Q}_n$ | 0.90 | 2.40 | 0.90 | 2.30 | 0.90 | 2.40 | ns | |
| $t_{PLH}$ | Propagation delay | 0.45 | 1.20 | 0.45 | 1.10 | 0.45 | 1.20 | ns | |
| $t_{PHL}$ | $E_n$ to $Q_n$, $\overline{Q}_n$ | 0.45 | 1.20 | 0.45 | 1.10 | 0.45 | 1.20 | ns | |
| $t_{TLH}$ | Transition time | 0.45 | 1.20 | 0.45 | 1.10 | 0.45 | 1.20 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.20 | 0.45 | 1.10 | 0.45 | 1.20 | ns | |

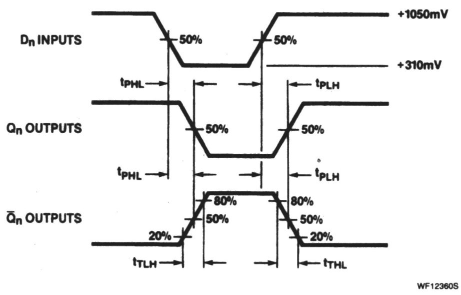
# Gate | 100117

## AC ELECTRICAL CHARACTERISTICS

**Flat Pack** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V \pm 5\%$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$D_n$ to $Q_n$, $\overline{Q}_n$ | 0.90<br>0.90 | 2.40<br>2.40 | 0.90<br>0.90 | 2.30<br>2.30 | 0.90<br>0.90 | 2.40<br>2.40 | ns<br>ns | Figs. 4, 5, 6 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$E_n$ to $Q_n$, $\overline{Q}_n$ | 0.45<br>0.45 | 1.20<br>1.20 | 0.45<br>0.45 | 1.10<br>1.10 | 0.45<br>0.45 | 1.20<br>1.20 | ns<br>ns | |
| $t_{TLH}$<br>$t_{THL}$ | Transition time<br>20% to 80%, 80% to 20% | 0.45<br>0.45 | 1.20<br>1.20 | 0.45<br>0.45 | 1.10<br>1.10 | 0.45<br>0.45 | 1.20<br>1.20 | ns<br>ns | |

## AC WAVEFORMS



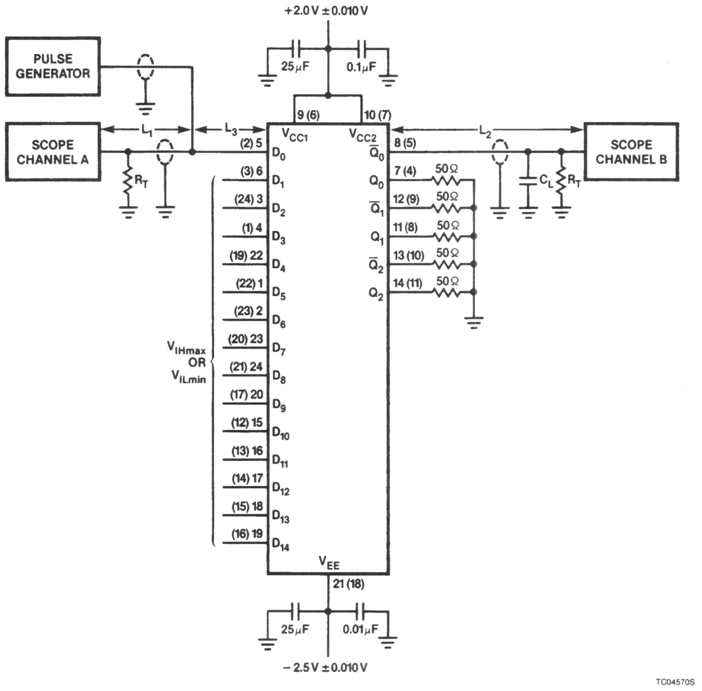
$D_n$ INPUTS
+1050mV
+310mV
50%
50%
$t_{PHL}$
$t_{PLH}$
$Q_n$ OUTPUTS
50%
50%
$t_{PHL}$
$t_{PLH}$
$\overline{Q}_n$ OUTPUTS
80%
80%
50%
50%
20%
20%
$t_{TLH}$
$t_{THL}$
WF12360S

Figure 4. Propagation Delay and Transition Times

# Gate

# 100117

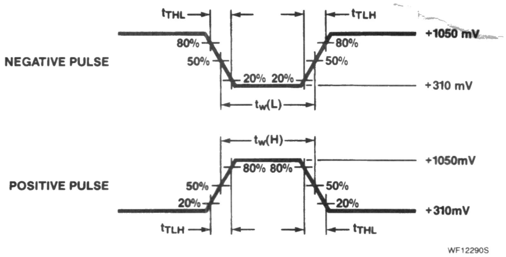
## TEST CIRCUITS AND WAVEFORMS


+2.0V ±0.010V
25μF
0.1μF
PULSE GENERATOR
SCOPE CHANNEL A
SCOPE CHANNEL B
L1
L2
L3
RT
CL
9 (6)
10 (7)
VCC1
VCC2
(2) 5 D0
(3) 6 D1
(24) 3 D2
(1) 4 D3
(19) 22 D4
(22) 1 D5
(23) 2 D6
(20) 23 D7
(21) 24 D8
(17) 20 D9
(12) 15 D10
(13) 16 D11
(14) 17 D12
(15) 18 D13
(16) 19 D14
VIHmax OR VILmin
8 (5) Q̄0
7 (4) Q0
12 (9) Q̄1
11 (8) Q1
13 (10) Q̄2
14 (11) Q2
50Ω
VEE
21 (18)
25μF
0.01μF
−2.5V ±0.010V
TC04570S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1μF and 25μF from GND to $V_{CC}$, 0.01μF and 25μF from GND to $V_{EE}$. (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance $\leq$ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.
11. Pin connections are for Flat Pack and in parentheses for Ceramic DIP.

Figure 5. Test Circuit


NEGATIVE PULSE
tTHL
tTLH
80%
50%
20% 20%
tw(L)
+1050 mV
+310 mV
POSITIVE PULSE
tw(H)
80% 80%
50%
20%
tTLH
tTHL
+1050mV
+310mV
WF12290S

| INPUT PULSE REQUIREMENTS<br>$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -2.5V \pm 0.010V$, $V_T$ = GND (0V) | | | | | |
|---|---|---|---|---|---|
| **Family** | **Amplitude** | **Rep Rate** | **Pulse Width** | **$t_{TLH}$** | **$t_{THL}$** |
| 100K ECL | 740mVp-p | 1MHz | 500ns | 0.7 ±0.1ns | 0.7 ±0.1ns |

Figure 6. Input Pulse Definition

**Signetics**

# 100118
## Gate

**Quint 2-4-4-4-5-Input OR-AND Gate**
***Product Specification***

**ECL Products**

### DESCRIPTION

The 100118 is a 5-wide OR-AND 2-4-4-4-5 input Gate with true and complementary outputs.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 100118 | 1.15ns | 43mA |

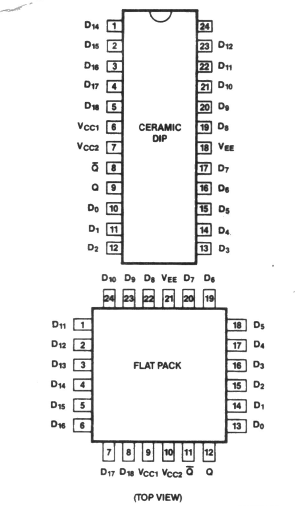
### ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} = GND$; $V_{EE} = -4.2V$ to $-4.8V$<br>$T_A = 0°C$ to $+85°C$ |
|---|---|
| Ceramic DIP | 100118F |
| Ceramic Flat Pack | 100118Y |

### PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_0 - D_{18}$ | Data Inputs |
| Q, $\overline{Q}$ | Data Outputs |

### PIN CONFIGURATION

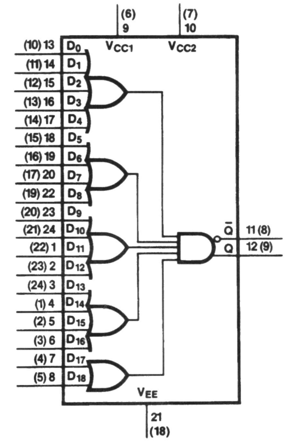

CERAMIC DIP
1 $D_{14}$
2 $D_{15}$
3 $D_{16}$
4 $D_{17}$
5 $D_{18}$
6 $V_{CC1}$
7 $V_{CC2}$
8 $\overline{Q}$
9 Q
10 $D_0$
11 $D_1$
12 $D_2$
13 $D_3$
14 $D_4$
15 $D_5$
16 $D_6$
17 $D_7$
18 $V_{EE}$
19 $D_8$
20 $D_9$
21 $D_{10}$
22 $D_{11}$
23 $D_{12}$
24
FLAT PACK
1 $D_{11}$
2 $D_{12}$
3 $D_{13}$
4 $D_{14}$
5 $D_{15}$
6 $D_{16}$
7 $D_{17}$
8 $D_{18}$
9 $V_{CC1}$
10 $V_{CC2}$
11 $\overline{Q}$
12 Q
13 $D_0$
14 $D_1$
15 $D_2$
16 $D_3$
17 $D_4$
18 $D_5$
19 $D_6$
20 $D_7$
21 $V_{EE}$
22 $D_8$
23 $D_9$
24 $D_{10}$

(TOP VIEW)

CD09110S

Figure 1

### LOGIC SYMBOL


(6) 9 $V_{CC1}$
(7) 10 $V_{CC2}$
(10) 13 $D_0$
(11) 14 $D_1$
(12) 15 $D_2$
(13) 16 $D_3$
(14) 17 $D_4$
(15) 18 $D_5$
(16) 19 $D_6$
(17) 20 $D_7$
(19) 22 $D_8$
(20) 23 $D_9$
(21) 24 $D_{10}$
(22) 1 $D_{11}$
(23) 2 $D_{12}$
(24) 3 $D_{13}$
(1) 4 $D_{14}$
(2) 5 $D_{15}$
(3) 6 $D_{16}$
(4) 7 $D_{17}$
(5) 8 $D_{18}$
$\overline{Q}$ 11 (8)
Q 12 (9)
$V_{EE}$ 21 (18)

Pin connections for Flat Pack and in ( ) for Ceramic DIP package

LD05160S

Figure 2

## FUNCTION TABLE

| INPUTS | | | | | | | | | | | | | | | | | | | OUTPUTS | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $D_0$ | $D_1$ | $D_2$ | $D_3$ | $D_4$ | $D_5$ | $D_6$ | $D_7$ | $D_8$ | $D_9$ | $D_{10}$ | $D_{11}$ | $D_{12}$ | $D_{13}$ | $D_{14}$ | $D_{15}$ | $D_{16}$ | $D_{17}$ | $D_{18}$ | $\overline{Q}$ | Q |
| L | L | L | L | L | X | X | X | X | X | X | X | X | X | X | X | X | X | X | H | L |
| X | X | X | X | X | L | L | L | L | X | X | X | X | X | X | X | X | X | X | H | L |
| X | X | X | X | X | X | X | X | X | L | L | L | L | X | X | X | X | X | X | H | L |
| X | X | X | X | X | X | X | X | X | X | X | X | X | L | L | L | L | X | X | H | L |
| X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | L | L | H | L |
| all other combinations | | | | | | | | | | | | | | | | | | | L | H |

Positive Logic:
H = HIGH state (more positive voltage) = 1
L = LOW state (less positive voltage) = 0
X = Don't Care

## ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | 100K ECL | UNIT |
|---|---|---|---|
| $V_{EE}$ | Supply voltage ($V_{CC1} = V_{CC2}$ = GND) | -7.0 to 0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | $V_{EE}$ to +0.5 | V |
| $I_O$ | Output source current | -55 | mA |
| $T_S$ | Storage temperature | -65 to +150 | °C |
| $T_J$ | Maximum junction temperature | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | | 100K ECL | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | -4.2 | -4.5 | -4.8 | V |
| $V_{EE}$ | Supply voltage (negative) when operating with 10K ECL family | | | | | -5.7 | V |
| $V_{IH}$ | HIGH level input voltage | $V_{CC1} = V_{CC2}$ = GND<br>$T_A$ = 0°C to +85°C | $V_{EE}$ = -4.2V | -1150 | | -880 | mV |
| | | | $V_{EE}$ = -4.5V | -1165 | | | |
| | | | $V_{EE}$ = -4.8V | | | | |
| $V_{IHT}$ | HIGH level input threshold voltage | | $V_{EE}$ = -4.2V | -1150 | | | mV |
| | | | $V_{EE}$ = -4.5V | -1165 | | | mV |
| | | | $V_{EE}$ = -4.8V | | | | |
| $V_{ILT}$ | LOW level input threshold voltage | | $V_{EE}$ = -4.2V | | | -1475 | mV |
| | | | $V_{EE}$ = -4.5V | | | | |
| | | | $V_{EE}$ = -4.8V | | | -1490 | mV |
| $V_{IL}$ | LOW level input voltage | | $V_{EE}$ = -4.2V | -1810 | | -1475 | mV |
| | | | $V_{EE}$ = -4.5V | | | | |
| | | | $V_{EE}$ = -4.8V | | | -1490 | |
| $T_A$ | Operating ambient temperature | | | 0 | +25 | +85 | °C |

**NOTE:**
When operating at other than specified voltages (-4.2V, -4.5V, -4.8V) DC & AC Characteristics will vary slightly from specified values.

# Gate

# 100118

**DC ELECTRICAL CHARACTERISTICS** $V_{CC1} = V_{CC2} =$ GND, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$, $T_A = 0°C$ to $+85°C$ unless otherwise specified[1, 3]

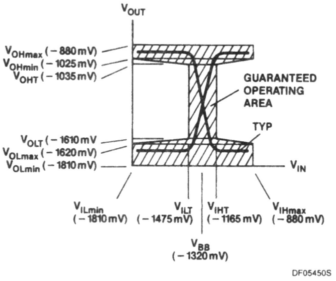
| PARAMETER | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] | |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | $V_{EE} = -4.2V$ | -1025 | | -870 | mV | $V_{IN} = V_{IHmax}$ or $V_{IN} = V_{ILmin}$ | Loading with 50Ω to -2.0V ±0.010V |
| | | $V_{EE} = -4.5V$ | -1025 | -955 | -880 | mV | | |
| | | $V_{EE} = -4.8V$ | -1035 | | -880 | mV | | |
| $V_{OHT}$ | HIGH level output threshold voltage | $V_{EE} = -4.2V$ | -1035 | | | mV | $V_{IN} = V_{IHmin}$ or $V_{IN} = V_{ILmax}$ | |
| | | $V_{EE} = -4.5V$ | -1035 | | | mV | | |
| | | $V_{EE} = -4.8V$ | -1045 | | | mV | | |
| $V_{OLT}$ | LOW level output threshold voltage | $V_{EE} = -4.2V$ | | | -1590 | mV | $V_{IN} = V_{IHmin}$ or $V_{IN} = V_{ILmax}$ | |
| | | $V_{EE} = -4.5V$ | | | -1610 | mV | | |
| | | $V_{EE} = -4.8V$ | | | -1610 | mV | | |
| $V_{OL}$ | LOW level output voltage | $V_{EE} = -4.2V$ | -1810 | | -1600 | mV | $V_{IN} = V_{IHmax}$ or $V_{IN} = V_{ILmin}$ | |
| | | $V_{EE} = -4.5V$ | -1810 | -1705 | -1620 | mV | | |
| | | $V_{EE} = -4.8V$ | -1830 | | -1620 | mV | | |
| $I_{IH}$ | HIGH level input current | | | | 350 | μA | $V_{IN} = V_{IHmax}$ | |
| $I_{IL}$ | LOW level input current | | 0.5 | | | μA | $V_{IN} = V_{ILmin}$ | |
| $-I_{EE}$ | $V_{EE}$ supply current | | 32 | 43 | 92 | mA | Inputs open | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | $V_{EE} = -4.2V$<br>$T_A = +25°C$ | | | 0.025 | V/V | | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | | 0.05 | V/V | | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to Section 3, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 3.

## Gate

## 100118



**NOTES:**

| | |
|---|---|
| $V_{IHmax}$ | – Maximum HIGH level input voltage (the most positive $V_{IH}$). |
| $V_{IHT}$ | – HIGH level input threshold voltage. |
| $V_{ILT}$ | – LOW level input threshold voltage. |
| $V_{ILmin}$ | – Minimum LOW level input voltage (the most negative $V_{IL}$). |
| $V_{OHmax}$ | – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition. |
| $V_{OHmin}$ | – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition. |
| $V_{OHT}$ | – HIGH level output threshold voltage with the inputs set to their respective threshold levels. |
| $V_{OLT}$ | – LOW level output threshold voltage with the inputs set to their respective threshold levels. |
| $V_{OLmax}$ | – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions. |
| $V_{OLmin}$ | – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions. |
| $V_{BB}$ | – Reference bias voltage (the internally generated reference voltage which is used to set the input and output threshold level). |

**Figure 3. Transfer Characteristics**

## AC ELECTRICAL CHARACTERISTICS

### Ceramic DIP $V_{CC1} = V_{CC2} = \text{GND}$, $V_{EE} = -4.2\text{V} \pm 0.010\text{V}$ to $-4.8\text{V} \pm 0.010\text{V}$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 0.85 | 3.20 | 0.85 | 3.20 | 0.85 | 3.40 | ns | Figs. 4, 5, 6 |
| $t_{PHL}$ | $D_n$ to Q, $\overline{Q}$ | 0.85 | 3.20 | 0.85 | 3.20 | 0.85 | 3.40 | ns | |
| $t_{TLH}$ | Transition time | 0.45 | 1.50 | 0.45 | 1.40 | 0.45 | 1.50 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.50 | 0.45 | 1.40 | 0.45 | 1.50 | ns | |

### Ceramic DIP $V_{CC1} = V_{CC2} = \text{GND}$, $V_{EE} = -5.2\text{V} \pm 5\%$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 0.85 | 3.20 | 0.85 | 3.20 | 0.85 | 3.40 | ns | Figs. 4, 5, 6 |
| $t_{PHL}$ | $D_n$ to Q, $\overline{Q}$ | 0.85 | 3.20 | 0.85 | 3.20 | 0.85 | 3.40 | ns | |
| $t_{TLH}$ | Transition time | 0.45 | 1.50 | 0.45 | 1.40 | 0.45 | 1.50 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.50 | 0.45 | 1.40 | 0.45 | 1.50 | ns | |

### Flat Pack $V_{CC1} = V_{CC2} = \text{GND}$, $V_{EE} = -4.2\text{V} \pm 0.010\text{V}$ to $-4.8\text{V} \pm 0.010\text{V}$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 0.85 | 3.00 | 0.85 | 3.00 | 0.85 | 3.20 | ns | Figs. 4, 5, 6 |
| $t_{PHL}$ | $D_n$ to Q, $\overline{Q}$ | 0.85 | 3.00 | 0.85 | 3.00 | 0.85 | 3.20 | ns | |
| $t_{TLH}$ | Transition time | 0.45 | 1.50 | 0.45 | 1.40 | 0.45 | 1.50 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.50 | 0.45 | 1.40 | 0.45 | 1.50 | ns | |

### Flat Pack $V_{CC1} = V_{CC2} = \text{GND}$, $V_{EE} = -5.2\text{V} \pm 5\%$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 0.85 | 3.00 | 0.85 | 3.00 | 0.85 | 3.20 | ns | Figs. 4, 5, 6 |
| $t_{PHL}$ | $D_n$ to Q, $\overline{Q}$ | 0.85 | 3.00 | 0.85 | 3.00 | 0.85 | 3.20 | ns | |
| $t_{TLH}$ | Transition time | 0.45 | 1.50 | 0.45 | 1.40 | 0.45 | 1.50 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.50 | 0.45 | 1.40 | 0.45 | 1.50 | ns | |

## AC WAVEFORMS

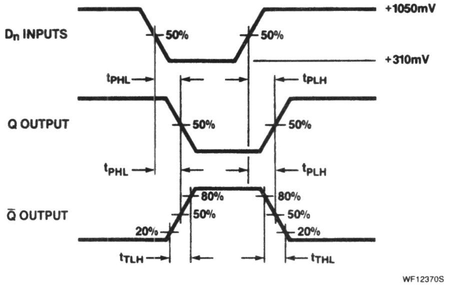
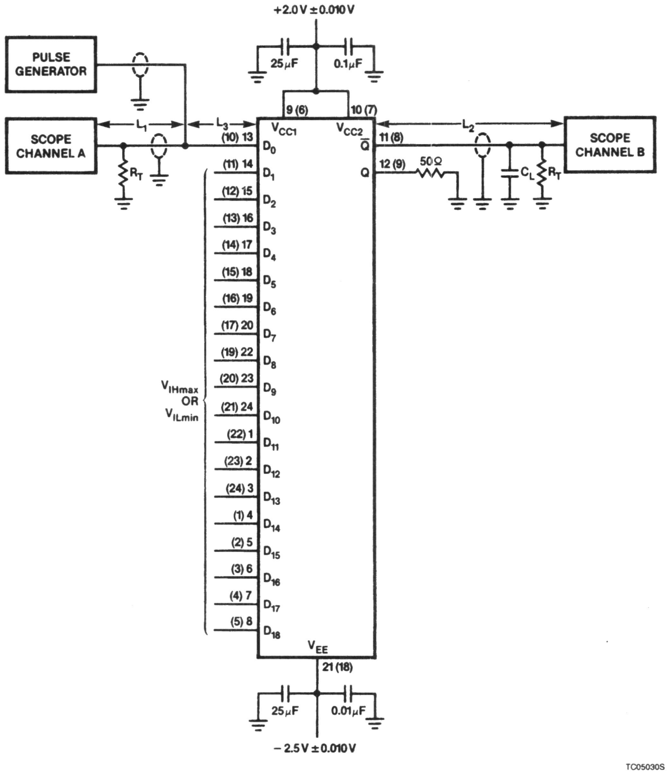

Dn INPUTS
50%
50%
+1050mV
+310mV
tPHL
tPLH
Q OUTPUT
50%
50%
tPHL
tPLH
Q̄ OUTPUT
80%
50%
20%
80%
50%
20%
tTLH
tTHL
WF12370S

Figure 4. Propagation Delay and Transition Times

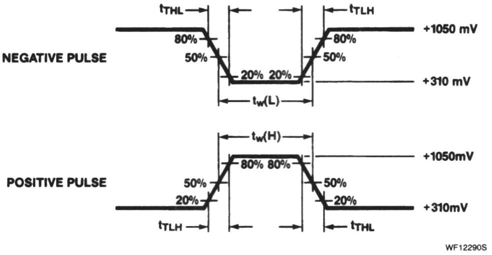
## TEST CIRCUITS AND WAVEFORMS


+2.0V ±0.010V
25μF
0.1μF
PULSE GENERATOR
SCOPE CHANNEL A
L1
L3
RT
9 (6)
10 (7)
VCC1
VCC2
(10) 13
D0
(11) 14
D1
(12) 15
D2
(13) 16
D3
(14) 17
D4
(15) 18
D5
(16) 19
D6
(17) 20
D7
(19) 22
D8
(20) 23
D9
(21) 24
D10
(22) 1
D11
(23) 2
D12
(24) 3
D13
(1) 4
D14
(2) 5
D15
(3) 6
D16
(4) 7
D17
(5) 8
D18
VIHmax OR VILmin
11 (8)
Q̄
12 (9)
Q
50Ω
L2
CL
RT
SCOPE CHANNEL B
VEE
21 (18)
25μF
0.01μF
−2.5V ±0.010V
TC05030S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1μF and 25μF from GND to $V_{CC}$, 0.01μF and 25μF from GND to $V_{EE}$. (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance $\leqslant$ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.
11. Pin connections are for Flat Pack and in parentheses for Ceramic DIP.

Figure 5. Test Circuit


NEGATIVE PULSE
tTHL
tTLH
80%
50%
20% 20%
80%
50%
+1050 mV
+310 mV
tw(L)
POSITIVE PULSE
tw(H)
80% 80%
50%
20%
50%
20%
+1050mV
+310mV
tTLH
tTHL
WF12290S

**INPUT PULSE REQUIREMENTS**

**$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -2.5V \pm 0.010V$, $V_T = GND\ (0V)$**

| Family | Amplitude | Rep Rate | Pulse Width | $t_{TLH}$ | $t_{THL}$ |
|---|---|---|---|---|---|
| 100K ECL | 740mVp-p | 1MHz | 500ns | 0.7 ±0.1ns | 0.7 ±0.1ns |

Figure 6. Input Pulse Definition

**Signetics**

# 100122
## Buffer

**9-Gate Buffer**
***Product Specification***

**ECL Products**

### DESCRIPTION

The 100122 contains 9 Buffer Gates with single input and output.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 100122 | 0.75ns | 78mA |

### ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} = GND$; $V_{EE} = -4.2V$ to $-4.8V$<br>$T_A = 0°C$ to $+85°C$ |
|---|---|
| Ceramic DIP | 100122F |
| Ceramic Flat Pack | 100122Y |

### PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_0 - D_8$ | Data Inputs |
| $Q_0 - Q_8$ | Data Outputs |

### PIN CONFIGURATION

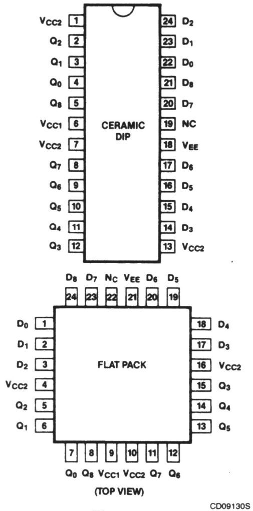
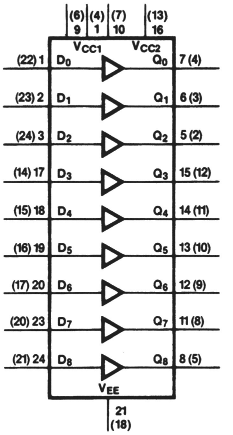

V_CC2 1
Q2 2
Q1 3
Q0 4
Q8 5
V_CC1 6
V_CC2 7
Q7 8
Q6 9
Q5 10
Q4 11
Q3 12
24 D2
23 D1
22 D0
21 D8
20 D7
19 NC
18 V_EE
17 D6
16 D5
15 D4
14 D3
13 V_CC2
CERAMIC DIP
D8 D7 NC V_EE D6 D5
24 23 22 21 20 19
D0 1
D1 2
D2 3
V_CC2 4
Q2 5
Q1 6
FLAT PACK
18 D4
17 D3
16 V_CC2
15 Q3
14 Q4
13 Q5
7 8 9 10 11 12
Q0 Q8 V_CC1 V_CC2 Q7 Q6
(TOP VIEW)
CD09130S

Figure 1

### LOGIC SYMBOL


(6) 9
(4) 1
(7) 10
(13) 16
V_CC1
V_CC2
(22) 1 D0
Q0 7 (4)
(23) 2 D1
Q1 6 (3)
(24) 3 D2
Q2 5 (2)
(14) 17 D3
Q3 15 (12)
(15) 18 D4
Q4 14 (11)
(16) 19 D5
Q5 13 (10)
(17) 20 D6
Q6 12 (9)
(20) 23 D7
Q7 11 (8)
(21) 24 D8
Q8 8 (5)
V_EE
21
(18)
LD05170S

Pin connections for Flat Pack and in ( ) for Ceramic DIP package

Figure 2

# Buffer 100122

**ABSOLUTE MAXIMUM RATINGS** (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | 100K ECL | UNIT |
|---|---|---|---|
| $V_{EE}$ | Supply voltage ($V_{CC1} = V_{CC2}$ = GND) | -7.0 to 0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | $V_{EE}$ to +0.5V | |
| $I_O$ | Output source current | -55 | mA |
| $T_S$ | Storage temperature | -65 to +150 | °C |
| $T_J$ | Maximum junction temperature | +150 | °C |

## RECOMMENDED OPERATING CONDITIONS

| PARAMETER | | | | 100K ECL | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | -4.2 | -4.5 | -4.8 | V |
| $V_{EE}$ | Supply voltage (negative) when operating with 10K ECL family | | | | | -5.7 | V |
| $V_{IH}$ | HIGH level input voltage | $V_{CC1} = V_{CC2}$ = GND<br>$T_A$ = 0°C to +85°C | $V_{EE}$ = -4.2V | -1150 | | -880 | mV |
| | | | $V_{EE}$ = -4.5V | -1165 | | | |
| | | | $V_{EE}$ = -4.8V | | | | |
| $V_{IHT}$ | HIGH level input threshold voltage | | $V_{EE}$ = -4.2V | -1150 | | | mV |
| | | | $V_{EE}$ = -4.5V | -1165 | | | mV |
| | | | $V_{EE}$ = -4.8V | | | | |
| $V_{ILT}$ | LOW level input threshold voltage | | $V_{EE}$ = -4.2V | | | -1475 | mV |
| | | | $V_{EE}$ = -4.5V | | | | |
| | | | $V_{EE}$ = -4.8V | | | -1490 | mV |
| $V_{IL}$ | LOW level input voltage | | $V_{EE}$ = -4.2V | -1810 | | -1475 | mV |
| | | | $V_{EE}$ = -4.5V | | | | |
| | | | $V_{EE}$ = -4.8V | | | -1490 | |
| $T_A$ | Operating ambient temperature | | | 0 | +25 | +85 | °C |

**NOTE:**
When operating at other than specified voltages (-4.2V, -4.5V, -4.8V) DC & AC Characteristics will vary slightly from specified values.

# Buffer

# 100122

## DC ELECTRICAL CHARACTERISTICS

$V_{CG1} = V_{CC2}$ = GND, $V_{EE}$ = −4.2V ±0.010V to −4.8V ±0.010V, $T_A$ = 0°C to +85°C unless otherwise specified[1,3]

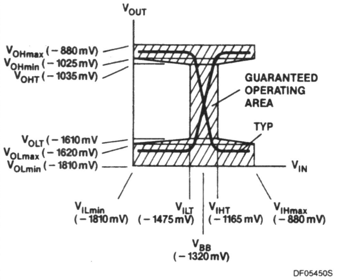
| PARAMETER | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] | |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | $V_{EE}$ = −4.2V | −1025 | | −870 | mV | $V_{IN} = V_{IHmax}$<br>or<br>$V_{IN} = V_{ILmin}$ | Loading with 50Ω to −2.0V ±0.010V |
| | | $V_{EE}$ = −4.5V | −1025 | −955 | −880 | mV | | |
| | | $V_{EE}$ = −4.8V | −1035 | | −880 | mV | | |
| $V_{OHT}$ | HIGH level output threshold voltage | $V_{EE}$ = −4.2V | −1035 | | | mV | $V_{IN} = V_{IHmin}$<br>or<br>$V_{IN} = V_{ILmax}$ | |
| | | $V_{EE}$ = −4.5V | −1035 | | | mV | | |
| | | $V_{EE}$ = −4.8V | −1045 | | | mV | | |
| $V_{OLT}$ | LOW level output threshold voltage | $V_{EE}$ = −4.2V | | | −1590 | mV | $V_{IN} = V_{IHmin}$<br>or<br>$V_{IN} = V_{ILmax}$ | |
| | | $V_{EE}$ = −4.5V | | | −1610 | mV | | |
| | | $V_{EE}$ = −4.8V | | | −1610 | mV | | |
| $V_{OL}$ | LOW level output voltage | $V_{EE}$ = −4.2V | −1810 | | −1600 | mV | $V_{IN} = V_{IHmax}$<br>or<br>$V_{IN} = V_{ILmin}$ | |
| | | $V_{EE}$ = −4.5V | −1810 | −1705 | −1620 | mV | | |
| | | $V_{EE}$ = −4.8V | −1830 | | −1620 | mV | | |
| $I_{IH}$ | HIGH level input current | | | | 350 | μA | $V_{IN} = V_{IHmax}$ | |
| $I_{IL}$ | LOW level input current | | 0.5 | | | μA | $V_{IN} = V_{ILmin}$ | |
| $-I_{EE}$ | $V_{EE}$ supply current | | 46 | 78 | 96 | mA | Inputs open | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | $V_{EE}$ = −4.2V<br>$T_A$ = +25°C | | | 0.025 | V/V | | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | | 0.050 | V/V | | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 3.

## Buffer

## 100122



**NOTES:**

$V_{IHmax}$ – Maximum HIGH level input voltage (the most positive $V_{IH}$).

$V_{IHT}$ – HIGH level input threshold voltage.

$V_{ILT}$ – LOW level input threshold voltage.

$V_{ILmin}$ – Minimum LOW level input voltage (the most negative $V_{IL}$).

$V_{OHmax}$ – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition.

$V_{OHmin}$ – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition.

$V_{OHT}$ – HIGH level output threshold voltage with the inputs set to their respective threshold levels.

$V_{OLT}$ – LOW level output threshold voltage with the inputs set to their respective threshold levels.

$V_{OLmax}$ – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions.

$V_{OLmin}$ – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions.

$V_{BB}$ – Reference Bias voltage. The internally generated reference voltage which is used to set the input and output threshold level.

**Figure 3. Transfer Characteristics**

## AC ELECTRICAL CHARACTERISTICS

### Ceramic DIP $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 0.45 | 1.60 | 0.45 | 1.45 | 0.45 | 1.60 | ns | Figs. 4, 5, 6 |
| $t_{PHL}$ | $D_n$ to $Q_n$ | 0.45 | 1.60 | 0.45 | 1.45 | 0.45 | 1.60 | ns | |
| $t_{TLH}$ | Transition time | 0.45 | 1.40 | 0.45 | 1.30 | 0.45 | 1.30 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.40 | 0.45 | 1.30 | 0.45 | 1.30 | ns | |

### Ceramic DIP $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V \pm 5\%$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 0.45 | 1.60 | 0.45 | 1.45 | 0.45 | 1.60 | ns | Figs. 4, 5, 6 |
| $t_{PHL}$ | $D_n$ to $Q_n$ | 0.45 | 1.60 | 0.45 | 1.45 | 0.45 | 1.60 | ns | |
| $t_{TLH}$ | Transition time | 0.45 | 1.40 | 0.45 | 1.30 | 0.45 | 1.30 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.40 | 0.45 | 1.30 | 0.45 | 1.30 | ns | |

### Flat Pack $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 0.45 | 1.40 | 0.45 | 1.25 | 0.45 | 1.40 | ns | Figs. 4, 5, 6 |
| $t_{PHL}$ | $D_n$ to $Q_n$ | 0.45 | 1.40 | 0.45 | 1.25 | 0.45 | 1.40 | ns | |
| $t_{TLH}$ | Transition time | 0.45 | 1.40 | 0.45 | 1.30 | 0.45 | 1.30 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.40 | 0.45 | 1.30 | 0.45 | 1.30 | ns | |

### Flat Pack $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V \pm 5\%$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 0.45 | 1.40 | 0.45 | 1.25 | 0.45 | 1.40 | ns | Figs. 4, 5, 6 |
| $t_{PHL}$ | $D_n$ to $Q_n$ | 0.45 | 1.40 | 0.45 | 1.25 | 0.45 | 1.40 | ns | |
| $t_{TLH}$ | Transition time | 0.45 | 1.40 | 0.45 | 1.30 | 0.45 | 1.30 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.40 | 0.45 | 1.30 | 0.45 | 1.30 | ns | |

## AC WAVEFORMS

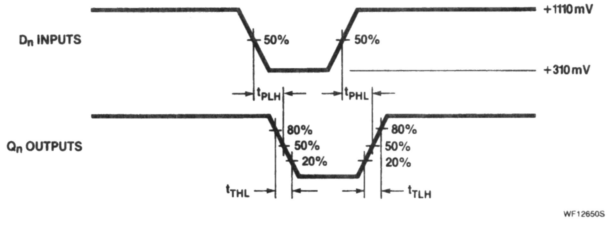

$D_n$ INPUTS
50%
50%
+1110mV
+310mV
$t_{PLH}$
$t_{PHL}$
$Q_n$ OUTPUTS
80%
50%
20%
80%
50%
20%
$t_{THL}$
$t_{TLH}$
WF12650S

Figure 4. Propagation Delay and Transition Times

## TEST CIRCUITS AND WAVEFORMS

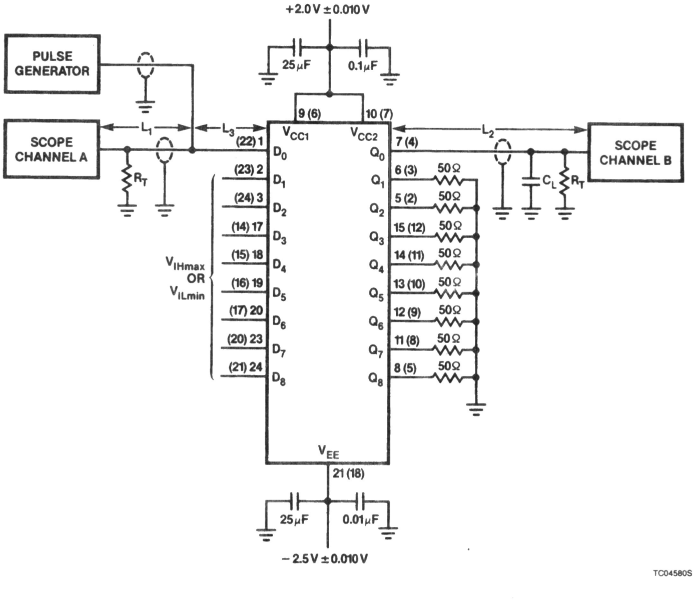
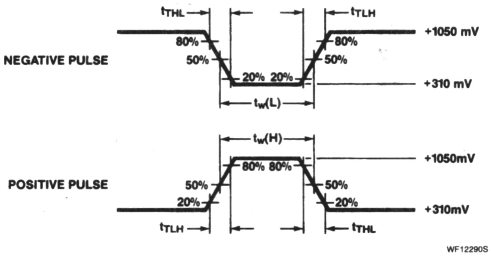

+2.0V ±0.010V
25μF
0.1μF
PULSE GENERATOR
SCOPE CHANNEL A
$L_1$
$L_3$
$R_T$
9 (6)
10 (7)
$V_{CC1}$
$V_{CC2}$
(22) 1 $D_0$
(23) 2 $D_1$
(24) 3 $D_2$
(14) 17 $D_3$
(15) 18 $D_4$
(16) 19 $D_5$
(17) 20 $D_6$
(20) 23 $D_7$
(21) 24 $D_8$
$V_{IHmax}$ OR $V_{ILmin}$
7 (4) $Q_0$
6 (3) $Q_1$
5 (2) $Q_2$
15 (12) $Q_3$
14 (11) $Q_4$
13 (10) $Q_5$
12 (9) $Q_6$
11 (8) $Q_7$
8 (5) $Q_8$
50Ω
$L_2$
$C_L$
$R_T$
SCOPE CHANNEL B
$V_{EE}$
21 (18)
25μF
0.01μF
−2.5V ±0.010V
TC04580S

Figure 5. Test Circuit

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1μF and 25μF from GND to $V_{CC}$, 0.01μF and 25μF from GND to $V_{EE}$. (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance $\leqslant$ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ±1% or better.
11. Pin connections are for Flat Pack and in parentheses for Ceramic DIP.


tTHL
tTLH
NEGATIVE PULSE
80%
50%
20% 20%
80%
50%
+1050 mV
+310 mV
tw(L)
tw(H)
POSITIVE PULSE
80% 80%
50%
20%
50%
20%
+1050mV
+310mV
tTLH
tTHL
WF12290S

| INPUT PULSE REQUIREMENTS<br>$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -2.5V \pm 0.010V$, $V_T$ = GND (0V) | | | | | |
|---|---|---|---|---|---|
| **Family** | **Amplitude** | **Rep Rate** | **Pulse Width** | **$t_{TLH}$** | **$t_{THL}$** |
| 100K ECL | 740mVp-p | 1MHz | 500ns | 0.7 ±0.1ns | 0.7 ±0.1ns |

**Figure 6. Input Pulse Definition**

Signetics

# 100123
## Driver

**Bus Driver**
***Product Specification***

**ECL Products**

## DESCRIPTION

The 100123 contains six bus drivers capable of driving terminated lines with terminations as low as 25Ω. Each output has its respective ground connection. The driver itself performs the positive logic AND of a data input and the OR of two enable inputs. The output voltage LOW level is more negative than usual ECL outputs. This allows an emitter-follower output transistor to turn off, when the termination supply $V_T$ is −2.0V ± 10%.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 100123 | 0.75ns | 176mA |

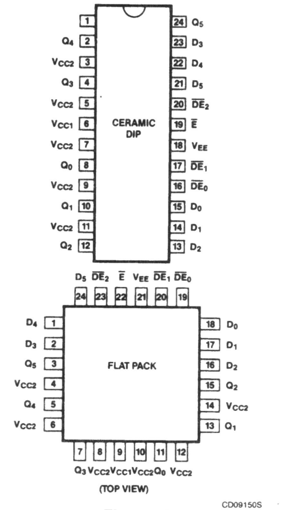
## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} = GND$; $V_{EE} = -4.2V$ to $-4.8V$<br>$T_A = 0°C$ to $+85°C$ |
|---|---|
| Ceramic DIP | 100123F |
| Ceramic Flat Pack | 100123Y |

## PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_0 - D_5$ | Data Inputs |
| $\overline{E}$ | Common Enable Input |
| $\overline{DE}_0 - \overline{DE}_2$ | Dual Enable Inputs |
| $Q_0 - Q_5$ | Data Outputs |

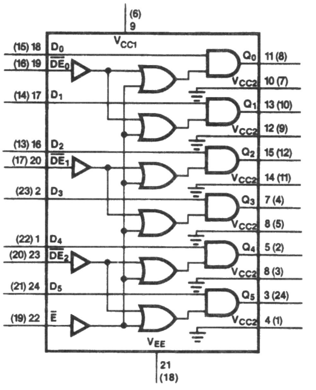
## PIN CONFIGURATION



1
Q4 2
VCC2 3
Q3 4
VCC2 5
VCC1 6
VCC2 7
Q0 8
VCC2 9
Q1 10
VCC2 11
Q2 12
24 Q5
23 D3
22 D4
21 D5
20 DE2
19 E
18 VEE
17 DE1
16 DE0
15 D0
14 D1
13 D2
CERAMIC DIP
D5 DE2 E VEE DE1 DE0
24 23 22 21 20 19
D4 1
D3 2
Q5 3
VCC2 4
Q4 5
VCC2 6
18 D0
17 D1
16 D2
15 Q2
14 VCC2
13 Q1
FLAT PACK
7 8 9 10 11 12
Q3 VCC2 VCC1 VCC2 Q0 VCC2
(TOP VIEW)
CD09150S

Figure 1

## LOGIC SYMBOL



(6)
9
VCC1
(15) 18 D0
(16) 19 DE0
(14) 17 D1
(13) 16 D2
(17) 20 DE1
(23) 2 D3
(22) 1 D4
(20) 23 DE2
(21) 24 D5
(19) 22 E
Q0 11 (8)
VCC2 10 (7)
Q1 13 (10)
VCC2 12 (9)
Q2 15 (12)
VCC2 14 (11)
Q3 7 (4)
VCC2 8 (5)
Q4 5 (2)
VCC2 6 (3)
Q5 3 (24)
VCC2 4 (1)
VEE
21
(18)
LD05181S

Pin connections for Flat Pack and in ( ) for Ceramic DIP package

Figure 2

## FUNCTION TABLE

| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{E}$ | $\overline{DE}$ | $D_n$ | $Q_n$ |
| X | X | L | L |
| L | L | H | L |
| H | X | H | H |
| X | H | H | H |

Positive Logic:
H = HIGH state (more positive voltage) = 1
L = LOW state (less positive voltage) = 0
X = Don't Care

## ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | 100K ECL | UNIT |
|---|---|---|---|
| $V_{EE}$ | Supply voltage ($V_{CC1} = V_{CC2} = GND$) | -7.0 to o | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | $V_{EE}$ to +0.5 | V |
| $I_O$ | Output source current | -55 | mA |
| $T_S$ | Storage temperature | -65 to +150 | °C |
| $T_J$ | Maximum junction temperature | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | | 100K ECL | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | -4.2 | -4.5 | -4.8 | V |
| $V_{EE}$ | Supply voltage (negative) when operating with 10K ECL family | | | | | -5.7 | V |
| $V_{IH}$ | HIGH level input voltage | $V_{CC1} = V_{CC2} = GND$<br>$T_A = 0°C$ to $+85°C$ | $V_{EE} = -4.2V$ | -1150 | | -880 | mV |
| | | | $V_{EE} = -4.5V$ | -1165 | | | |
| | | | $V_{EE} = -4.8V$ | | | | |
| $V_{IHT}$ | HIGH level input threshold voltage | | $V_{EE} = -4.2V$ | -1150 | | | mV |
| | | | $V_{EE} = -4.5V$ | -1165 | | | mV |
| | | | $V_{EE} = -4.8V$ | | | | |
| $V_{ILT}$ | LOW level input threshold voltage | | $V_{EE} = -4.2V$ | | | -1475 | mV |
| | | | $V_{EE} = -4.5V$ | | | | |
| | | | $V_{EE} = -4.8V$ | | | -1490 | mV |
| $V_{IL}$ | LOW level input voltage | | $V_{EE} = -4.2V$ | -1810 | | -1475 | mV |
| | | | $V_{EE} = -4.5V$ | | | | |
| | | | $V_{EE} = -4.8V$ | | | -1490 | |
| $T_A$ | Operating ambient temperature | | | 0 | +25 | +85 | °C |

**NOTE:**
When operating at other than specified voltages (-4.2V, -4.5V, -4.8V) DC & AC Characteristics will vary slightly from specified values.

## DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2} = GND$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$, $T_A = 0°C$ to $+85°C$ unless otherwise specified[1, 3]

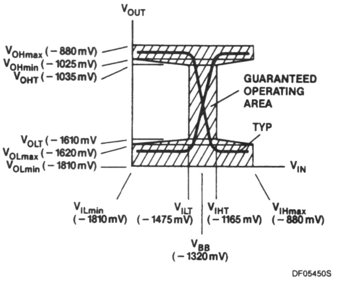
| PARAMETER | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] | |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | $V_{EE} = -4.2V$ | −1035 | | −870 | mV | $V_{IN} = V_{IHmax}$<br>or<br>$V_{IN} = V_{ILmin}$ | Loading with 25Ω to −2.0V |
| | | $V_{EE} = -4.5V$ | −1025 | −955 | −880 | mV | | |
| | | $V_{EE} = -4.8V$ | −1035 | | −870 | mV | | |
| $V_{OHT}$ | HIGH level output threshold voltage | $V_{EE} = -4.2V$ | −1045 | | | mV | $V_{IN} = V_{IHmin}$<br>or<br>$V_{IN} = V_{ILmax}$ | Loading with 25Ω to −2.1V |
| | | $V_{EE} = -4.5V$ | −1035 | | | mV | | |
| | | $V_{EE} = -4.8V$ | −1045 | | | mV | | |
| $V_{OLT}$ | LOW level output threshold voltage | $V_{EE} = -4.2V$ | | | −1590 | mV | $V_{IN} = V_{IHmin}$<br>or<br>$V_{IN} = V_{ILmax}$ | Loading with 25Ω to −2.0V ±0.010V |
| | | $V_{EE} = -4.5V$ | | | −1610 | mV | | |
| | | $V_{EE} = -4.8V$ | | | −1610 | mV | | |
| $V_{OL}$ | LOW level output voltage | $V_{EE} = -4.2V$ | | | −2200 | mV | $V_{IN} = V_{IHmax}$<br>or<br>$V_{IN} = V_{ILmin}$ | Loading with 25Ω to −2.4V |
| | | $V_{EE} = -4.5V$ | | | −2200 | mV | | |
| | | $V_{EE} = -4.8V$ | | | −2200 | mV | | |
| $I_{IH}$ | HIGH level input current | $\overline{E}$ | | | 350 | µA | $V_{IN} = V_{IHmax}$ | |
| | | $D_n$, $\overline{DE}$ | | | 260 | µA | | |
| $I_{IL}$ | LOW level input current | | 0.5 | | | µA | $V_{IN} = V_{ILmin}$ | |
| $-I_{EE}$ | $V_{EE}$ supply current | | 113 | 176 | 235 | mA | Inputs open | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | $V_{EE} = -4.2V$<br>$T_A = +25°C$ | | | 0.035 | V/V | | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 3.

## Driver

## 100123



**NOTES:**

| | |
|---|---|
| $V_{IHmax}$ | – Maximum HIGH level input voltage (the most positive $V_{IH}$). |
| $V_{IHT}$ | – HIGH level input threshold voltage. |
| $V_{ILT}$ | – LOW level input threshold voltage. |
| $V_{ILmin}$ | – Minimum LOW level input voltage (the most negative $V_{IL}$). |
| $V_{OHmax}$ | – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition. |
| $V_{OHmin}$ | – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition. |
| $V_{OHT}$ | – HIGH level output threshold voltage with the inputs set to their respective threshold levels. |
| $V_{OLT}$ | – LOW level output threshold voltage with the inputs set to their respective threshold levels. |
| $V_{OLmax}$ | – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions. |
| $V_{OLmin}$ | – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions. |
| $V_{BB}$ | – Reference Bias voltage. The internally generated reference voltage which is used to set the input and output threshold level. |

**Figure 3. Transfer Characteristics**

## AC ELECTRICAL CHARACTERISTICS

### Ceramic DIP $V_{CC1} = V_{CC2} = \text{GND}$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 1.70 | 4.35 | 1.75 | 4.35 | 1.75 | 4.65 | ns | Figs. 4, 5, 6 |
| $t_{PHL}$ | $D_n$ to $Q_n$ | 1.00 | 2.40 | 1.00 | 2.40 | 1.10 | 2.60 | ns | |
| $t_{PLH}$ | Propagation delay | 2.00 | 4.70 | 2.00 | 4.70 | 2.00 | 5.10 | ns | |
| $t_{PHL}$ | $\overline{DE}_n$ to $Q_n$ | 1.20 | 3.00 | 1.20 | 3.00 | 1.20 | 3.40 | ns | |
| $t_{PLH}$ | Propagation delay | 2.10 | 5.40 | 2.10 | 5.30 | 2.10 | 5.80 | ns | |
| $t_{PHL}$ | $\overline{E}$ to $Q_n$ | 1.20 | 3.30 | 1.20 | 3.30 | 1.20 | 3.70 | ns | |
| $t_{TLH}$ | Transition time | 0.70 | 2.00 | 0.70 | 1.90 | 0.70 | 2.10 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.30 | 0.45 | 1.20 | 0.45 | 1.30 | ns | |

### Ceramic DIP $V_{CC1} = V_{CC2} = \text{GND}$, $V_{EE} = -5.2V \pm 5\%$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 1.70 | 4.35 | 1.75 | 4.35 | 1.75 | 4.65 | ns | Figs. 4, 5, 6 |
| $t_{PHL}$ | $D_n$ to $Q_n$ | 1.00 | 2.40 | 1.00 | 2.40 | 1.10 | 2.60 | ns | |
| $t_{PLH}$ | Propagation delay | 2.00 | 4.70 | 2.00 | 4.70 | 2.00 | 5.10 | ns | |
| $t_{PHL}$ | $\overline{DE}_n$ to $Q_n$ | 1.20 | 3.00 | 1.20 | 3.00 | 1.20 | 3.40 | ns | |
| $t_{PLH}$ | Propagation delay | 2.10 | 5.40 | 2.10 | 5.30 | 2.10 | 5.80 | ns | |
| $t_{PHL}$ | $\overline{E}$ to $Q_n$ | 1.20 | 3.30 | 1.20 | 3.30 | 1.20 | 3.70 | ns | |
| $t_{TLH}$ | Transition time | 0.70 | 2.00 | 0.70 | 1.90 | 0.70 | 2.10 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.30 | 0.45 | 1.20 | 0.45 | 1.30 | ns | |

### Flat Pack $V_{CC1} = V_{CC2} = \text{GND}$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 1.70 | 4.15 | 1.75 | 4.15 | 1.75 | 4.45 | ns | Figs. 4, 5, 6 |
| $t_{PHL}$ | $D_n$ to $Q_n$ | 1.00 | 2.20 | 1.00 | 2.20 | 1.10 | 2.40 | ns | |
| $t_{PLH}$ | Propagation delay | 2.00 | 4.50 | 2.00 | 4.50 | 2.00 | 4.90 | ns | |
| $t_{PHL}$ | $\overline{DE}_n$ to $Q_n$ | 1.20 | 2.80 | 1.20 | 2.80 | 1.20 | 3.20 | ns | |
| $t_{PLH}$ | Propagation delay | 2.10 | 5.20 | 2.10 | 5.10 | 2.10 | 5.60 | ns | |
| $t_{PHL}$ | $\overline{E}$ to $Q_n$ | 1.20 | 3.10 | 1.20 | 3.10 | 1.20 | 3.50 | ns | |
| $t_{TLH}$ | Transition time | 0.70 | 2.00 | 0.70 | 1.90 | 0.70 | 2.10 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.30 | 0.45 | 1.20 | 0.45 | 1.30 | ns | |

## Driver

## 100123

### AC ELECTRICAL CHARACTERISTICS

**Flat Pack** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V \pm 5\%$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$D_n$ to $Q_n$ | 1.70<br>1.00 | 4.15<br>2.20 | 1.75<br>1.00 | 4.15<br>2.20 | 1.75<br>1.10 | 4.45<br>2.40 | ns<br>ns | Figs. 4, 5, 6 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$\overline{DE}_n$ to $Q_n$ | 2.00<br>1.20 | 4.50<br>2.80 | 2.00<br>1.20 | 4.50<br>2.80 | 2.00<br>1.20 | 4.90<br>3.20 | ns<br>ns | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$\overline{E}$ to $Q_n$ | 2.10<br>1.20 | 5.20<br>3.10 | 2.10<br>1.20 | 5.10<br>3.10 | 2.10<br>1.20 | 5.60<br>3.50 | ns<br>ns | |
| $t_{TLH}$<br>$t_{THL}$ | Transition time<br>20% to 80%, 80% to 20% | 0.70<br>0.45 | 2.00<br>1.30 | 0.70<br>0.45 | 1.90<br>1.20 | 0.70<br>0.45 | 2.10<br>1.30 | ns<br>ns | |

### AC WAVEFORMS

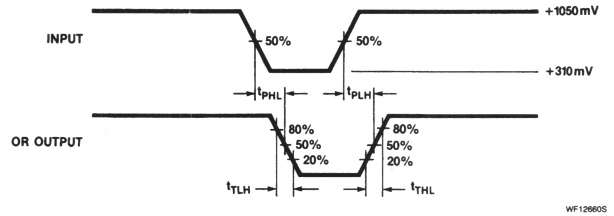
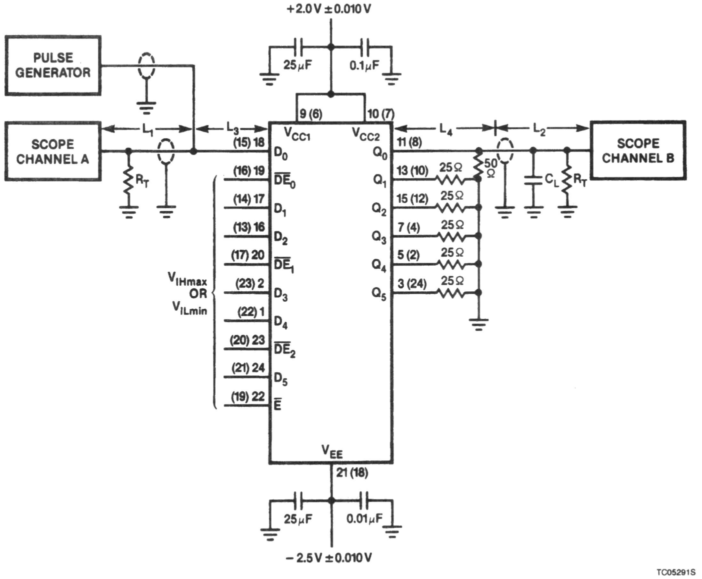

INPUT
OR OUTPUT
+1050mV
+310mV
50%
50%
$t_{PHL}$
$t_{PLH}$
80%
50%
20%
80%
50%
20%
$t_{TLH}$
$t_{THL}$
WF12660S

Figure 4. Propagation Delay and Transition Times

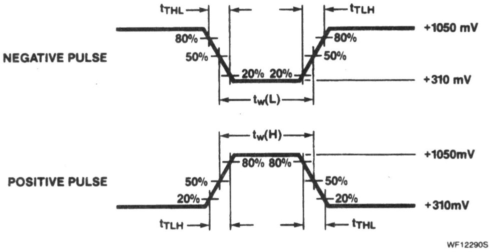
## TEST CIRCUITS AND WAVEFORMS


+2.0V ±0.010V
25μF
0.1μF
PULSE GENERATOR
SCOPE CHANNEL A
SCOPE CHANNEL B
L1
L2
L3
L4
RT
50 Ω
CL
9 (6)
10 (7)
VCC1
VCC2
(15) 18 D0
(16) 19 DE0
(14) 17 D1
(13) 16 D2
(17) 20 DE1
(23) 2 D3
(22) 1 D4
(20) 23 DE2
(21) 24 D5
(19) 22 E
VIHmax OR VILmin
11 (8) Q0
13 (10) Q1 25Ω
15 (12) Q2 25Ω
7 (4) Q3 25Ω
5 (2) Q4 25Ω
3 (24) Q5 25Ω
VEE
21 (18)
25μF
0.01μF
−2.5V ±0.010V
TC05291S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1μF and 25μF from GND to $V_{CC}$, 0.01μF and 25μF from GND to $V_{EE}$. (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 25Ω to GND.
5. $L_1$ and $L_2$ are equal length 25Ω impedance lines. $L_4$ and $L_3$, the distance from the DUT input and output pins to the junction of their respective interconnecting cables should not exceed 1/4 inch (6mm).
6. $R_T = 50\Omega$ terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance $\leqslant$ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All load resistors should have tolerance of ± 1% or better.
11. Pin connections are for Flat Pack and in parentheses for Ceramic DIP.

Figure 5. Test Circuit


NEGATIVE PULSE
tTHL
tTLH
80%
50%
20%
20%
80%
50%
tw(L)
+1050 mV
+310 mV
POSITIVE PULSE
tw(H)
80%
80%
50%
20%
50%
20%
tTLH
tTHL
+1050mV
+310mV
WF12290S

| INPUT PULSE REQUIREMENTS<br>$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -2.5V \pm 0.010V$, $V_T$ = GND (0V) | | | | | |
|---|---|---|---|---|---|
| Family | Amplitude | Rep Rate | Pulse Width | $t_{TLH}$ | $t_{THL}$ |
| 100K ECL | 740mVp-p | 1MHz | 500ns | 0.7 ±0.1ns | 0.7 ±0.1ns |

Figure 6. Input Pulse Definition

**Signetics**

# 100124
# Translator

**Hex TTL-to-ECL Translator**
***Preliminary Specification***

**ECL Products**

## DESCRIPTION

The 100124 is a Hex Translator, designed to convert TTL logic levels to 100K ECL logic levels. The inputs are compatible with standard or Schottky TTL. A common Enable input (E), when LOW, holds all inverting HIGH and holds all true outputs LOW. The differential outputs allow each circuit to be used as an inverting/non-inverting translator or as a differential line driver. The output levels are voltage compensated. When the circuit is used in the differential mode, the 100124, due to its high common-mode rejection, overcomes voltage gradients between the mode rejection, overcomes voltage gradients between the TTL and ECL ground systems. The $V_{EE}$ and $V_{CC}$ power may be applied in either order.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 100124 | 1.7ns | 105mA |

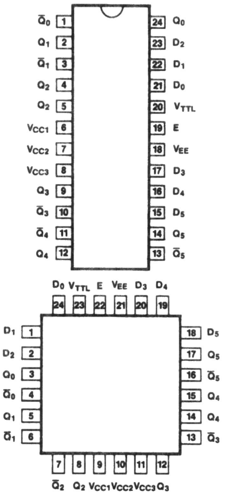
## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC1} = V_{CC2} = V_{CC3}$ = GND; $V_{TTL} = +5.0V$; $V_{EE} = -4.2V$ to $-4.8V$; $T_A = 0°C$ to $+85°C$ |
|---|---|
| Ceramic DIP | 100124F |
| Ceramic Flat Pack | 100124Y |

## PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_0 - D_5$ | Data Inputs (Schottky TTL) |
| E | Enable Inputs (Schottky TTL) |
| $Q_0 - Q_5$ | Data Outputs |
| $\overline{Q}_0 - \overline{Q}_5$ | Complementary Data Outputs |

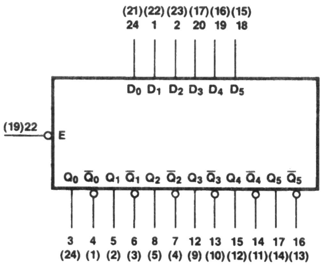
## PIN CONFIGURATION



$\overline{Q}_0$ 1
$Q_1$ 2
$\overline{Q}_1$ 3
$Q_2$ 4
$Q_2$ 5
$V_{CC1}$ 6
$V_{CC2}$ 7
$V_{CC3}$ 8
$Q_3$ 9
$\overline{Q}_3$ 10
$\overline{Q}_4$ 11
$Q_4$ 12
24 $Q_0$
23 $D_2$
22 $D_1$
21 $D_0$
20 $V_{TTL}$
19 E
18 $V_{EE}$
17 $D_3$
16 $D_4$
15 $D_5$
14 $Q_5$
13 $\overline{Q}_5$
$D_0$ $V_{TTL}$ E $V_{EE}$ $D_3$ $D_4$
24 23 22 21 20 19
$D_1$ 1
$D_2$ 2
$Q_0$ 3
$\overline{Q}_0$ 4
$Q_1$ 5
$\overline{Q}_1$ 6
18 $D_5$
17 $Q_5$
16 $\overline{Q}_5$
15 $Q_4$
14 $Q_4$
13 $\overline{Q}_3$
7 8 9 10 11 12
$\overline{Q}_2$ $Q_2$ $V_{CC1}$ $V_{CC2}$ $V_{CC3}$ $Q_3$
CD09201S

Figure 1

## LOGIC SYMBOL



(21)(22)(23)(17)(16)(15)
24 1 2 20 19 18
$D_0$ $D_1$ $D_2$ $D_3$ $D_4$ $D_5$
(19)22
E
$Q_0$ $\overline{Q}_0$ $Q_1$ $\overline{Q}_1$ $Q_2$ $\overline{Q}_2$ $Q_3$ $\overline{Q}_3$ $Q_4$ $\overline{Q}_4$ $Q_5$ $\overline{Q}_5$
3 4 5 6 8 7 12 13 15 14 17 16
(24) (1) (2) (3) (5) (4) (9) (10) (12) (11) (14) (13)

$V_{CC}$ = Pin 23(20)
$V_{CC1}$ = Pin 9(6), 10(7), 11(8)
$V_{EE}$ = Pin 21(18)

Pin connections for Flat Pack and in ( ) for Slim CERDIP package

LS10670S

Figure 2

**ABSOLUTE MAXIMUM RATINGS** (Operation beyond the limits set forth in this table may impair useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | | VALUE | UNIT |
|---|---|---|---|---|
| 100K ECL | $V_{EE}$ | Supply voltage (GND1 = GND2 = GND3 = GND) | −7.0 to 0 | V |
| | $I_O$ | Output source current | 55 | mA |
| TTL | $V_{CC}$ | Supply voltage | +7.0 | V |
| | $V_{IN}$ | Input voltage | −0.5 to +5.5 | V |
| | $I_{IN}$ | Input current | −30 to +5.0 | mA |
| $T_S$ | | Storage temperature | −65 to +150 | °C |
| $T_J$ | | Maximum junction temperature | +150 | °C |

## DC OPERATING CONDITIONS FOR TTL

| PARAMETER | | TTL | | | UNIT |
|---|---|---|---|---|---|
| | | Min | Nom | Max | |
| $V_{CC1}$<br>$V_{CC2}$ | Supply voltage | 4.5 | 5.0 | 5.5 | V |
| $V_{IH}$ | HIGH level input voltage | 2.0 | | | V |
| $V_{IL}$ | LOW level input voltage | | | +0.8 | V |
| $I_{IK}$ | Input clamp current | | | −18 | mA |
| $I_{OH}$ | HIGH level output current | | | −1 | V |
| $I_{OL}$ | LOW level output current | 2.0 | | 20 | V |
| $T_A$ | Operating ambient temperature | 0 | +25 | +85 | °C |

## DC OPERATING CONDITIONS FOR ECL

| PARAMETER | | 100K ECL | | | UNIT |
|---|---|---|---|---|---|
| | | Min | Nom | Max | |
| $V_{CC1}$<br>$V_{CC2}$ | Circuit ground | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | −4.2 | −4.5 | −4.8 | V |
| $V_{EE}$ | Supply voltage (negative) when operating with 10K ECL family | | | −5.7 | V |

# Translator

# 100124

## DC ELECTRICAL CHARACTERISTICS (TTL)

$V_{CC1} = V_{CC2} = V_{CC3}$ = GND, $V_{TTL}$ = +5.0V ±0.010V, $V_{EE}$ = −4.2V ±0.010V to −4.8V ±0.010V, $T_A$ = 0°C to +85°C unless otherwise specified[1]

| PARAMETER | | | 100124 | | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|
| $I_I$ | Input current at maximum input voltage | | | | 1.0 | mA | $V_{IN}$ = +5.5V<br>All other inputs = GND |
| $I_{IH}$ | HIGH level input current | $D_n$ inputs | | | 20 | µA | $V_{IN}$ = +2.4V<br>All other inputs = GND |
| | | E inputs | | | 120 | | |
| $I_{IL}$ | LOW level input current | $D_n$ inputs | −1.6 | | | mA | $V_{IN}$ = +0.4V<br>All other inputs = GND |
| | | E inputs | −9.6 | | | | |
| $I_{CC}$ | Supply current | | | 44 | 75 | mA | All inputs $V_{IN}$ = GND |

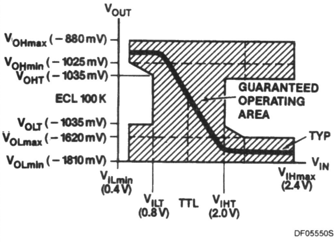
## DC ELECTRICAL CHARACTERISTICS (100K ECL)

$V_{CC1} = V_{CC2} = V_{CC3}$ = GND, $V_{TTL}$ = +5.0V ±0.010V, $V_{EE}$ = −4.2V to −4.8V ±0.010V, $T_A$ = 0°C to +85°C unless otherwise specified[1,3]

| PARAMETER | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] | |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | $V_{EE}$ = −4.2V | −1025 | | −870 | mV | $V_{IN}$ = 0.4V (TTL) | Loading with 25Ω to −2.0V |
| | | $V_{EE}$ = −4.5V | −1025 | −955 | −880 | mV | | |
| | | $V_{EE}$ = −4.8V | −1035 | | −880 | mV | | |
| $V_{OHT}$ | HIGH level output threshold voltage | $V_{EE}$ = −4.2V | −1035 | | | mV | $V_{IN}$ = 0.8V (TTL) | |
| | | $V_{EE}$ = −4.5V | −1035 | | | mV | | |
| | | $V_{EE}$ = −4.8V | −1045 | | | mV | | |
| $V_{OLT}$ | LOW level output threshold voltage | $V_{EE}$ = −4.2V | | | −1590 | mV | $V_{IN}$ = 2.0V (TTL) | |
| | | $V_{EE}$ = −4.5V | | | −1610 | mV | | |
| | | $V_{EE}$ = −4.8V | | | −1610 | mV | | |
| $V_{OL}$ | LOW level output voltage | $V_{EE}$ = −4.2V | −1810 | | −1600 | mV | $V_{IN}$ = 2.4V (TTL) | |
| | | $V_{EE}$ = −4.5V | −1810 | −1705 | −1620 | mV | | |
| | | $V_{EE}$ = −4.8V | −1830 | | −1620 | mV | | |
| $-I_{EE}$ | Supply current | | 52 | 96 | 140 | mA | For all inputs $V_{IN}$ = +4.0V | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | $V_{EE}$ = −4.2V<br>$T_A$ = +25°C | | | 0.035 | V/V | | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | | 0.070 | V/V | | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to Section 3 Testing, DC testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 3.



NOTES:

$V_{IHmax}$ – Maximum HIGH level input voltage (the most positive $V_{IH}$).
$V_{IHT}$ – HIGH level input threshold voltage.
$V_{ILT}$ – LOW level input threshold voltage.
$V_{ILmin}$ – Minimum LOW level input voltage (the most negative $V_{IL}$).
$V_{OHmax}$ – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition.
$V_{OHmin}$ – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition.
$V_{OHT}$ – HIGH level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLT}$ – LOW level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLmax}$ – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions.
$V_{OLmin}$ – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions.
$V_{BB}$ – Reference Bias voltage. The internally generated reference voltage which is used to set the input and output threshold level.

Figure 3. Transfer Characteristics (TTL to ECL)

## AC ELECTRICAL CHARACTERISTICS

**Ceramic DIP** $V_{CC1} = V_{CC2} = V_{CC3} = GND$, $V_{TTL} = +5.0V \pm 0.010V$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$

| | PARAMETER | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 0.50 | 3.00 | 0.50 | 2.90 | 0.50 | 3.00 | ns | Fig. 5, 6, 7 |
| $t_{PHL}$ | $D_n$ to $Q_n$, $\overline{Q}_n$ | 0.50 | 3.00 | 0.50 | 2.90 | 0.50 | 3.00 | ns | |
| $t_{TLH}$ | Transition time TTL | 0.45 | 1.80 | 0.45 | 1.80 | 0.45 | 1.80 | ns | Fig. 5, 7 |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.80 | 0.45 | 1.80 | 0.45 | 1.80 | ns | |

**Ceramic DIP** $V_{CC1} = V_{CC2} = V_{CC3} = GND$, $V_{TTL} = +5.0V \pm 0.010V$, $V_{EE} = -5.2V \pm 5\%$

| | PARAMETER | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 0.50 | 3.00 | 0.50 | 2.90 | 0.50 | 3.00 | ns | Fig. 5, 6, 7 |
| $t_{PHL}$ | $D_n$ to $Q_n$, $\overline{Q}_n$ | 0.50 | 3.00 | 0.50 | 2.90 | 0.50 | 3.00 | ns | |
| $t_{TLH}$ | Transition time TTL | 0.45 | 1.80 | 0.45 | 1.80 | 0.45 | 1.80 | ns | Fig. 5, 7 |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.80 | 0.45 | 1.80 | 0.45 | 1.80 | ns | |

**Flat Pack** $V_{CC1} = V_{CC2} = V_{CC3} = GND$, $V_{TTL} = +5.0V \pm 0.010V$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$

| | PARAMETER | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 0.50 | 2.80 | 0.50 | 2.70 | 0.50 | 2.80 | ns | Fig. 5, 6, 7 |
| $t_{PHL}$ | $D_n$ to $Q_n$, $\overline{Q}_n$ | 0.50 | 2.80 | 0.50 | 2.70 | 0.50 | 2.80 | ns | |
| $t_{TLH}$ | Transition time TTL | 0.45 | 1.70 | 0.45 | 1.70 | 0.45 | 1.70 | ns | Fig. 5, 7 |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.70 | 0.45 | 1.70 | 0.45 | 1.70 | ns | |

**Flat Pack** $V_{CC1} = V_{CC2} = V_{CC3} = GND$, $V_{TTL} = +5.0V \pm 0.010V$, $V_{EE} = -5.2V \pm 5\%$

| | PARAMETER | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 0.50 | 2.80 | 0.50 | 2.70 | 0.50 | 2.80 | ns | Fig. 5, 6, 7 |
| $t_{PHL}$ | $D_n$ to $Q_n$, $\overline{Q}_n$ | 0.50 | 2.80 | 0.50 | 2.70 | 0.50 | 2.80 | ns | |
| $t_{TLH}$ | Transition time TTL | 0.45 | 1.70 | 0.45 | 1.70 | 0.45 | 1.70 | ns | Fig. 5, 7 |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.70 | 0.45 | 1.70 | 0.45 | 1.70 | ns | |

## AC WAVEFORMS

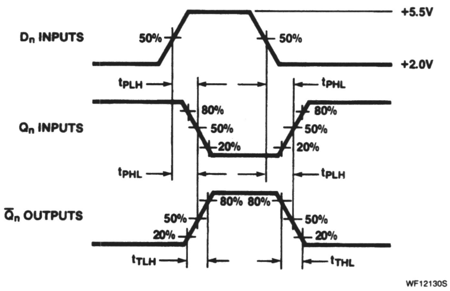
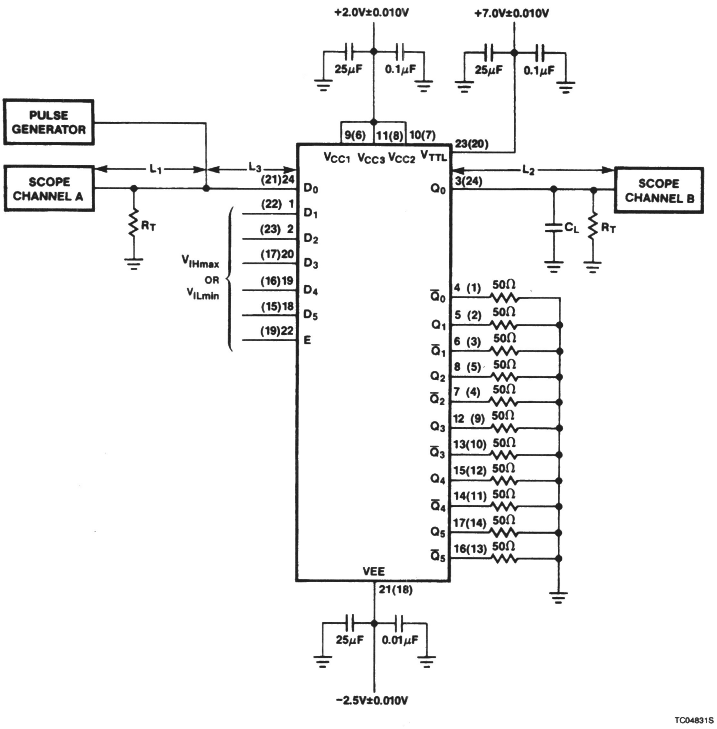

Dn INPUTS
50%
50%
+5.5V
+2.0V
tPLH
tPHL
Qn INPUTS
80%
50%
20%
80%
50%
20%
tPHL
tPLH
Q̄n OUTPUTS
80% 80%
50%
20%
50%
20%
tTLH
tTHL
WF12130S

Figure 4. Propagation Delay and Transition Times for Data to Output

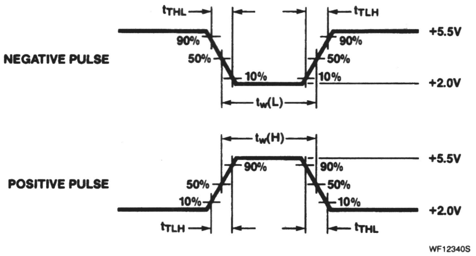
## TEST CIRCUITS AND WAVEFORMS


+2.0V±0.010V
+7.0V±0.010V
25μF
0.1μF
25μF
0.1μF
PULSE GENERATOR
SCOPE CHANNEL A
L1
L3
RT
9(6)
11(8)
10(7)
23(20)
VCC1 VCC3 VCC2 VTTL
(21)24
D0
(22) 1
D1
(23) 2
D2
(17)20
D3
(16)19
D4
(15)18
D5
(19)22
E
VIHmax OR VILmin
Q0
3(24)
L2
SCOPE CHANNEL B
CL
RT
Q̄0
4 (1)
Q1
5 (2)
Q̄1
6 (3)
Q2
8 (5)
Q̄2
7 (4)
Q3
12 (9)
Q̄3
13(10)
Q4
15(12)
Q̄4
14(11)
Q5
17(14)
Q̄5
16(13)
50Ω
VEE
21(18)
25μF
0.01μF
-2.5V±0.010V
TC04831S

**NOTES:**

1. $V_{CC1} = V_{CC2} = V_{CC3} = +2V \pm 0.010V$, $V_{TTL} = +7.0V \pm 0.010V$, $V_{EE} = -2.5V \pm 0.010V$
2. Decoupling 0.1μF and 25μF from GND to $V_{CC}$, 0.01μF and 25μF from GND to $V_{EE}$. (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance $\leqslant$ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ±1% or better.
11. Pin connections are for Flat Pack and in parentheses for Ceramic DIP packages.

Figure 5. AC Test Circuit for 100124


$t_{THL}$
$t_{TLH}$
90%
50%
10%
NEGATIVE PULSE
+5.5V
+2.0V
$t_w(L)$
$t_w(H)$
POSITIVE PULSE
90%
50%
10%
+5.5V
+2.0V
$t_{TLH}$
$t_{THL}$
WF12340S

**INPUT PULSE REQUIREMENTS**

**$V_{CC1} = V_{CC2} = V_{CC3} = +2.0V \pm 0.010V$, $V_{TTL} = +7.0V \pm 0.010V$, $V_{EE} = -2.5V \pm 0.010V$, $V_T$ = GND (0V)**

| Family | Amplitude | Rep Rate | Pulse Width | $t_{TLH}$ | $t_{THL}$ |
|---|---|---|---|---|---|
| TTL | 3.5Vp-p | 1MHz | 500ns | 5.5 ±0.3ns | 5.5 ±0.2ns |

**Figure 6. Input Pulse Definition**

# 100125
## Translator

**Hex ECL-to-TTL Translator**
***Preliminary Specification***

**ECL Products**

## DESCRIPTION

100125 is a Hex Translator to convert 100K ECL logic levels to TTL logic levels. Differential inputs allow each circuit to be used as an inverting, non-inverting or differential receiver. An internal reference voltage generator provides $V_{BB}$ for single-ended operation or for use in Schmitt trigger applications.

All inputs have 50kΩ pulldown resistors; therefore, the outputs will go LOW when the inputs are left unconnected. When used in the differential mode, the inputs have a common-mode rejection of +1V, making this device tolerant of ground offsets and transients between the signal source and the translator. The $V_{EE}$ and $V_{CC}$ power may be applied in either order.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 100125 | 2.2ns | 105mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{TTL1} = V_{TTL2} = +5.0V$, $V_{CC1} = V_{CC2} = GND$; $V_{EE} = -4.2V$ to $-4.8V$; $T_A = 0°C$ to $+85°C$ |
|---|---|
| Ceramic DIP | 100125F |
| Ceramic Flat Pack | 100125Y |

## PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_0 - D_5$ | Data Inputs |
| $\overline{D}_0 - \overline{D}_5$ | Data Inputs, Inverting |
| $V_{BB}$ | Reference Bias Voltage Output |
| $Q_0 - Q_5$ | Data Outputs (Schottky TTL) |

## PIN CONFIGURATION

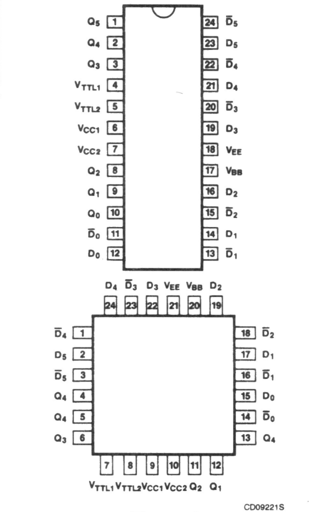
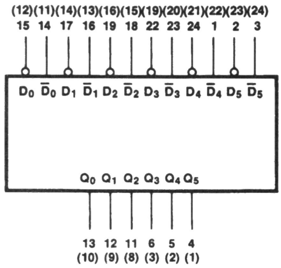

Q5 1
Q4 2
Q3 3
VTTL1 4
VTTL2 5
VCC1 6
VCC2 7
Q2 8
Q1 9
Q0 10
D̄0 11
D0 12
24 D̄5
23 D5
22 D̄4
21 D4
20 D̄3
19 D3
18 VEE
17 VBB
16 D2
15 D̄2
14 D1
13 D̄1
D4 D̄3 D3 VEE VBB D2
24 23 22 21 20 19
D̄4 1
D5 2
D̄5 3
Q4 4
Q4 5
Q3 6
18 D̄2
17 D1
16 D̄1
15 D0
14 D̄0
13 Q4
7 8 9 10 11 12
VTTL1 VTTL2 VCC1 VCC2 Q2 Q1
CD09221S

Figure 1

## LOGIC SYMBOL


(12)(11)(14)(13)(16)(15)(19)(20)(21)(22)(23)(24)
15 14 17 16 19 18 22 23 24 1 2 3
D0 D̄0 D1 D̄1 D2 D̄2 D3 D̄3 D4 D̄4 D5 D̄5
Q0 Q1 Q2 Q3 Q4 Q5
13 12 11 6 5 4
(10) (9) (8) (3) (2) (1)

$V_{TTL}$ = Pin 7(4), 8(5)
$V_{CC}$ = Pin 9(6), 10(7)
$V_{EE}$ = Pin 21(18)
$V_{BB}$ = Pin 20(17)

**Pin connections for FLAT PACK and in ( ) for Slim CERDIP package.**

LS10681S

Figure 2

# Translator

# 100125

## ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | | 100K ECL | UNIT |
|---|---|---|---|---|
| 100K ECL | $V_{EE}$ | Supply voltage (GND1 = GND2 = GND3 = GND) | -7.0 to 0 | V |
| | $I_O$ | Output source current | 55 | mA |
| TTL | $V_{CC}$ | Supply voltage | +7.0 | V |
| | $V_{IN}$ | Input voltage | -0.5 to +5.5 | V |
| | $I_{IN}$ | Input current | -30 to +5.0 | mA |
| $T_S$ | | Storage temperature | -65 to +150 | °C |
| $T_J$ | | Maximum junction temperature | +150 | °C |

## DC OPERATING CONDITIONS FOR SINGLE ENDED MODE

| PARAMETER | | | | 100K ECL | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | -4.2 | -4.5 | -4.8 | V |
| $V_{EE}$ | Supply voltage (negative) when operating with 10K ECL Family | | | | | -5.7 | V |
| $V_{IH}$ | HIGH level input voltage (Single ended) | $V_{CC1} = V_{CC2} = GND$<br>$T_A = 0°C$ to $+85°C$ | $V_{EE} = -4.2V$ | -1150 | | -880 | mV |
| | | | $V_{EE} = -4.5V$ | -1165 | | | |
| | | | $V_{EE} = -4.8V$ | | | | |
| $V_{IHT}$ | HIGH level input threshold voltage | | $V_{EE} = -4.2V$ | -1150 | | | mV |
| | | | $V_{EE} = -4.5V$ | -1165 | | | mV |
| | | | $V_{EE} = -4.8V$ | | | | |
| $V_{ILT}$ | LOW level input threshold voltage | | $V_{EE} = -4.2V$ | | | -1475 | mV |
| | | | $V_{EE} = -4.5V$ | | | | |
| | | | $V_{EE} = -4.8V$ | | | -1490 | mV |
| $V_{IL}$ | LOW level input voltage (Single ended) | | $V_{EE} = -4.2V$ | -1810 | | -1475 | mV |
| | | | $V_{EE} = -4.5V$ | | | | |
| | | | $V_{EE} = -4.8V$ | | | -1490 | |
| $V_{BB}$ | Output reference voltage | | $V_{EE} = -4.2V$ | -1396 | -1320 | -1244 | mV |
| | | | $V_{EE} = -4.5V$ | -1380 | | -1260 | |
| | | | $V_{EE} = -4.8V$ | -1396 | | -1244 | |
| $T_A$ | Operating ambient temperature | | | 0 | +25 | +85 | °C |

**NOTE:**
When operating at other than specified voltages (-4.2V, -4.5V, -4.8V) DC & AC Characteristics will vary slightly from specified values.

# Translator 100125

## DC OPERATING CONDITIONS FOR DIFFERENTIAL MODE

| PARAMETER | | | 100K ECL | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | |
| $V_{IHH}$ | $V_{IHmax} + 1.0V$ | $V_{EE} = -4.2V$ | −150 | | +120 | mV |
| | | $V_{EE} = -4.5V$ | −165 | | | mV |
| | | $V_{EE} = -4.8V$ | | | | mV |
| $V_{IHL}$ | $V_{IHmax} - 1.0V$ | $V_{EE} = -4.2V$ | −2150 | | −1880 | mV |
| | | $V_{EE} = -4.5V$ | −2165 | | | mV |
| | | $V_{EE} = -4.8V$ | | | | mV |
| $V_{ILH}$ | $V_{ILmin} + 1.0V$ | $V_{EE} = -4.2V$ | −810 | | −475 | mV |
| | | $V_{EE} = -4.5V$ | | | | mV |
| | | $V_{EE} = -4.8V$ | | | −490 | mV |
| $V_{ILL}$ | $V_{ILmin} - 1.0V$ | $V_{EE} = -4.2V$ | −2810 | | −2475 | mV |
| | | $V_{EE} = -4.5V$ | | | | mV |
| | | $V_{EE} = -4.8V$ | | | −2490 | mV |
| $V_{DIFF}$ | Input voltage differential | $V_{EE} = -4.2V$ | 150 | | | mV |
| | | $V_{EE} = -4.5V$ | | | | |
| | | $V_{EE} = -4.8V$ | | | | |
| $V_{CM}$ | Common-mode voltage | $V_{EE} = -4.2V$ | | | | V |
| | | $V_{EE} = -4.5V$ | | | | |
| | | $V_{EE} = -4.8V$ | | | | |

**NOTE:**
When operating at $V_{EE}$ other than specified voltage (−4.2V, −4.5V, −4.8V), the DC and AC Characteristics will vary slightly from specified values.

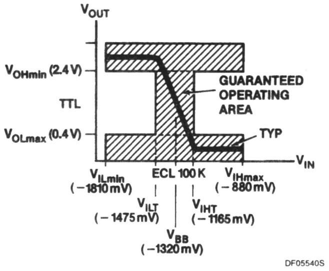
## DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2} = GND$, $V_{TTL} = +5.0 \pm 0.010V$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$, $T_A = 0°C$ to $+85°C$ unless otherwise specified[1, 3]

| PARAMETER | | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] |
|---|---|---|---|---|---|---|---|---|
| ECL | $I_{IH}$ | HIGH level input current | | | | 350 | µA | $V_{IN} = V_{IHmax}$, $D_0 - D_5 = V_{BB}$<br>$D_0 - D_5 = V_{ILmin}$ |
| | $I_{IL}$ | LOW input current | | 0.5 | | | µA | $V_{IN} = V_{ILmin}$, $D_0 - D_5 = V_{BB}$ |
| | $-I_{EE}$ | $V_{EE}$ supply current | | 60 | 105 | 150 | mA | $D_0 - D_1 = V_{BB}$ |
| | $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | $V_{EE} = -4.2V$<br>$T_A = +25°C$ | | | 0.035 | V/V | |
| | $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | | 0.070 | V/V | |
| TTL | $V_{OH}$ | HIGH level output voltage | | 2.4 | 3.4 | | V | $I_{OH} = -2.0mA$ |
| | $V_{OL}$ | LOW level output voltage | | | | 0.4 | V | $I_{OL} = 20mA$ |
| | $I_{OS}$ | Short circuit output current[4] | | −100 | | −40 | mA | $V_{OUT} = GND$ |
| | $I_{CC}$ | $V_{CC}$ Supply Current | | | 75 | 115 | mA | $D_0 - D_5 = VBB$ |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst-case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 3.



**NOTES:**

| | |
|---|---|
| $V_{IHmax}$ | – Maximum HIGH level input voltage (the most positive $V_{IH}$). |
| $V_{IHT}$ | – HIGH level input threshold voltage. |
| $V_{ILT}$ | – LOW level input threshold voltage. |
| $V_{ILmin}$ | – Minimum LOW level input voltage (the most negative $V_{IL}$). |
| $V_{OHmax}$ | – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition. |
| $V_{OHmin}$ | – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition. |
| $V_{OHT}$ | – HIGH level output threshold voltage with the inputs set to their respective threshold levels. |
| $V_{OLT}$ | – LOW level output threshold voltage with the inputs set to their respective threshold levels. |
| $V_{OLmax}$ | – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions. |
| $V_{OLmin}$ | – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions. |
| $V_{BB}$ | – Reference Bias voltage. The internally generated reference voltage which is used to set the input and output threshold level. |

**Figure 3. Transfer Characteristics for ECL 100K to TTL**

## AC ELECTRICAL CHARACTERISTICS

**Ceramic DIP** $V_{CC1} = V_{CC2} = GND$, $V_{TTL} = +5V \pm 0.010V$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8 \pm 0.010V$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 0.80 | 3.50 | 0.90 | 3.70 | 1.00 | 4.00 | ns | Figs. 4, 5, 6 |
| $t_{PHL}$ | $D_n$ to $Q_n$ | 0.80 | 3.50 | 0.90 | 3.70 | 1.00 | 4.00 | ns | |
| $t_{TLH}$ | Transition time TTL | 0.50 | 2.60 | 0.50 | 2.60 | 0.50 | 2.60 | ns | Figs. 4, 6 |
| $t_{THL}$ | 10% to 90% to 90% to 10% | 0.50 | 2.60 | 0.50 | 2.60 | 0.50 | 2.60 | ns | |

**Ceramic DIP** $V_{CC1} = V_{CC2} = GND$, $V_{TTL} = +5V \pm 0.010V$, $V_{EE} = -5.2V \pm 5\%$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 0.80 | 3.50 | 0.90 | 3.70 | 1.00 | 4.00 | ns | Figs. 4, 5, 6 |
| $t_{PHL}$ | $D_n$ to $Q_n$ | 0.80 | 3.50 | 0.90 | 3.70 | 1.00 | 4.00 | ns | |
| $t_{TLH}$ | Transition time TTL | 0.50 | 2.60 | 0.50 | 2.60 | 0.50 | 2.60 | ns | Figs. 4, 6 |
| $t_{THL}$ | 10% to 90% to 90% to 10% | 0.50 | 2.60 | 0.50 | 2.60 | 0.50 | 2.60 | ns | |

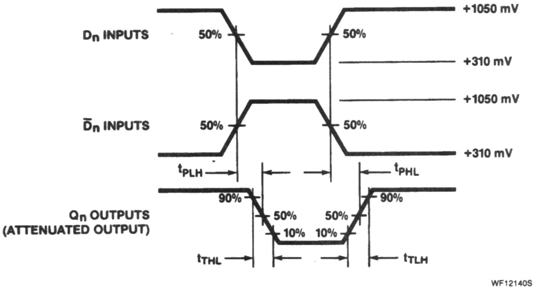
**Flat Pack** $V_{CC1} = V_{CC2} = GND$, $V_{TTL} = +5V \pm 0.010V$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 0.80 | 3.30 | 0.90 | 3.50 | 1.00 | 3.80 | ns | Figs. 4, 5, 6 |
| $t_{PHL}$ | $D_n$ to $Q_n$ | 0.80 | 3.30 | 0.90 | 3.50 | 1.00 | 3.80 | ns | |
| $t_{TLH}$ | Transition time TTL | 0.50 | 2.50 | 0.50 | 2.50 | 0.50 | 2.50 | ns | Figs. 4, 6 |
| $t_{THL}$ | 10% to 90% to 90% to 10% | 0.50 | 2.50 | 0.50 | 2.50 | 0.50 | 2.50 | ns | |

**Flat Pack** $V_{CC1} = V_{CC2} = GND$, $V_{TTL} = +5V \pm 0.010V$, $V_{EE} = -5.2V \pm 5\%$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 0.80 | 3.30 | 0.90 | 3.50 | 1.00 | 3.80 | ns | Figs. 4, 5, 6 |
| $t_{PHL}$ | $D_n$ to $Q_n$ | 0.80 | 3.30 | 0.90 | 3.50 | 1.00 | 3.80 | ns | |
| $t_{TLH}$ | Transition time TTL | 0.50 | 2.50 | 0.50 | 2.50 | 0.50 | 2.50 | ns | Figs. 4, 6 |
| $t_{THL}$ | 10% to 90% to 90% to 10% | 0.50 | 2.50 | 0.50 | 2.50 | 0.50 | 2.50 | ns | |

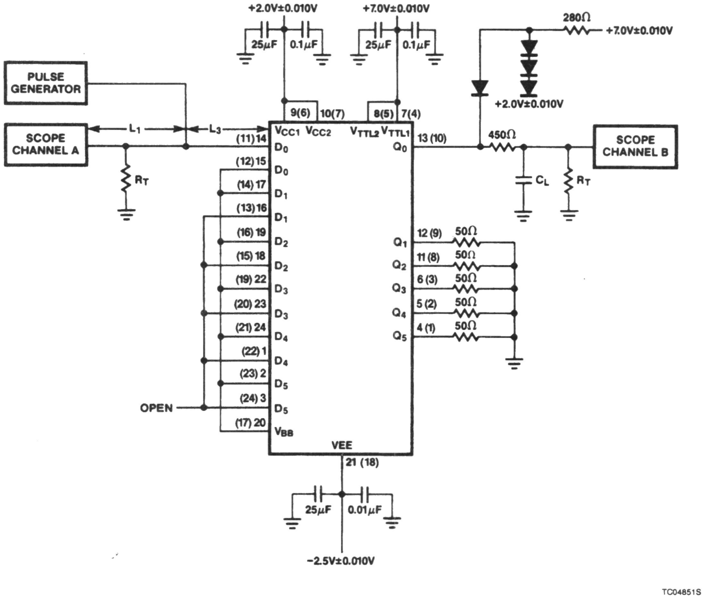
## AC WAVEFORMS



+1050 mV
D_n INPUTS
50%
50%
+310 mV
+1050 mV
D̄_n INPUTS
50%
50%
+310 mV
t_PLH
t_PHL
Q_n OUTPUTS
(ATTENUATED OUTPUT)
90%
90%
50%
50%
10%
10%
t_THL
t_TLH
WF12140S

Figure 4. Propagation Delay and Transition Times for Data to Output

## TEST CIRCUITS AND WAVEFORMS

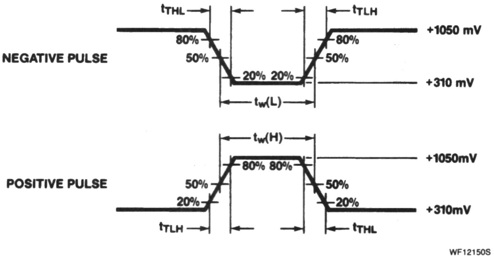


+2.0V±0.010V
25μF
0.1μF
+7.0V±0.010V
25μF
0.1μF
280Ω
+7.0V±0.010V
+2.0V±0.010V
PULSE GENERATOR
SCOPE CHANNEL A
L1
L3
RT
9(6)
10(7)
8(5)
7(4)
VCC1 VCC2
VTTL2 VTTL1
(11)14 D0
(12)15 D̄0
(14)17 D1
(13)16 D̄1
(16)19 D2
(15)18 D̄2
(19)22 D3
(20)23 D̄3
(21)24 D4
(22)1 D̄4
(23)2 D5
(24)3 D̄5
(17)20 VBB
OPEN
13 (10) Q0
450Ω
CL
RT
SCOPE CHANNEL B
12 (9) Q1 50Ω
11 (8) Q2 50Ω
6 (3) Q3 50Ω
5 (2) Q4 50Ω
4 (1) Q5 50Ω
VEE
21 (18)
25μF
0.01μF
-2.5V±0.010V
TC04851S

Figure 5. AC Test Circuit for 100125

**NOTES:**

1. $V_{TTL1} = V_{TTL2} = 7.0V \pm 0.010V$, $V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -2.5V \pm 0.010V$.
2. Decoupling 0.1μF and 25μF from GND to $V_{CC}$, 0.01μF from GND to $V_{EE}$ (0.01 and 0.1uF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than ¼ inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin and the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed ¼ inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than ¼ inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance ⩽ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed ¼ inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.
11. Pin connections are for Flat Pack and in parentheses for Ceramic DIP.


NEGATIVE PULSE
$t_{THL}$
$t_{TLH}$
80%
50%
20%
20%
80%
50%
$t_w(L)$
+1050 mV
+310 mV
POSITIVE PULSE
$t_w(H)$
80%
80%
50%
20%
50%
20%
$t_{TLH}$
$t_{THL}$
+1050mV
+310mV
WF12150S

| INPUT PULSE REQUIREMENTS<br>$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{TTL} = +7.0V \pm 0.010V$, $V_{EE} = -2.5V \pm 0.010V$,<br>$V_T$ = GND (0V) | | | | | |
|---|---|---|---|---|---|
| **Family** | **Amplitude** | **Rep Rate** | **Pulse Width** | **$t_{TLH}$** | **$t_{THL}$** |
| 100K ECL | 740mVp-p | 1MHz | 500ns | 0.7 ±0.1ns | 0.7 ±0.1ns |

Figure 6. Input Pulse Definition

Signetics

# 100126
## Backplane Driver

**9-Bit Backplane Driver**
***Product Specification***

**ECL Products**

## DESCRIPTION

100126 contains nine independent, high-speed buffer gates each with a single input and a single output. The gates are non-inverting. These buffers are useful in bus-oriented systems where minimal output loading or bus isolation is desired. The output transition times are longer to minimize noise when used as a backplane driver.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 100126 | 2.0ns | 78mA |

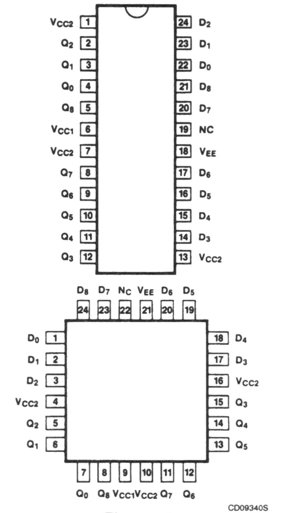
## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} = GND$; $V_{EE} = -4.2V$ to $-4.8V$<br>$T_A = 0°C$ to $+85°C$ |
|---|---|
| Ceramic DIP | 100126F |
| Ceramic Flat Pack | 100126Y |

## PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_0 - D_8$ | Data Inputs |
| $Q_0 - Q_8$ | Data Outputs |

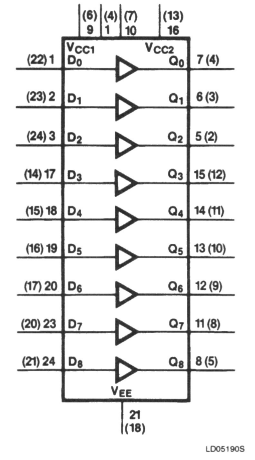
## PIN CONFIGURATION



VCC2 1
Q2 2
Q1 3
Q0 4
Q8 5
VCC1 6
VCC2 7
Q7 8
Q6 9
Q5 10
Q4 11
Q3 12
24 D2
23 D1
22 D0
21 D8
20 D7
19 NC
18 VEE
17 D6
16 D5
15 D4
14 D3
13 VCC2
D8 D7 NC VEE D6 D5
24 23 22 21 20 19
D0 1
D1 2
D2 3
VCC2 4
Q2 5
Q1 6
18 D4
17 D3
16 VCC2
15 Q3
14 Q4
13 Q5
7 8 9 10 11 12
Q0 Q8 VCC1 VCC2 Q7 Q6
CD09340S

Figure 1

## LOGIC SYMBOL



(6) 9
(4) 1
(7) 10
(13) 16
VCC1
VCC2
(22) 1 D0
(23) 2 D1
(24) 3 D2
(14) 17 D3
(15) 18 D4
(16) 19 D5
(17) 20 D6
(20) 23 D7
(21) 24 D8
Q0 7 (4)
Q1 6 (3)
Q2 5 (2)
Q3 15 (12)
Q4 14 (11)
Q5 13 (10)
Q6 12 (9)
Q7 11 (8)
Q8 8 (5)
VEE
21
(18)
LD05190S

Figure 2

**ABSOLUTE MAXIMUM RATINGS** (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | 100K ECL | UNIT |
|---|---|---|---|
| $V_{EE}$ | Supply voltage ($V_{CC1}$ = $V_{CC2}$ = GND) | −7.0 to 0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | $V_{EE}$ to +0.5 | V |
| $I_O$ | Output source current | −55 | mA |
| $T_S$ | Storage temperature | −55 to +150 | °C |
| $T_J$ | Maximum junction temperature | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | | 100K ECL | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | −4.2 | −4.5 | −4.8 | V |
| $V_{EE}$ | Supply voltage (negative) when operating with 10K ECL family | | | | | −5.7 | V |
| $V_{IH}$ | HIGH level input voltage | $V_{CC1}$ = $V_{CC2}$ = GND<br>$T_A$ = 0°C to +85°C | $V_{EE}$ = −4.2V | −1150 | | −880 | mV |
| | | | $V_{EE}$ = −4.5V | −1165 | | | |
| | | | $V_{EE}$ = −4.8V | | | | |
| $V_{IHT}$ | HIGH level input threshold voltage | | $V_{EE}$ = −4.2V | −1150 | | | mV |
| | | | $V_{EE}$ = −4.5V | −1165 | | | mV |
| | | | $V_{EE}$ = −4.8V | | | | |
| $V_{ILT}$ | LOW level input threshold voltage | | $V_{EE}$ = −4.2V | | | −1475 | mV |
| | | | $V_{EE}$ = −4.5V | | | | |
| | | | $V_{EE}$ = −4.8V | | | −1490 | mV |
| $V_{IL}$ | LOW level input voltage | | $V_{EE}$ = −4.2V | −1810 | | −1475 | mV |
| | | | $V_{EE}$ = −4.5V | | | | |
| | | | $V_{EE}$ = −4.8V | | | −1490 | |
| $T_A$ | Operating ambient temperature | | | 0 | +25 | +85 | °C |

**NOTE:**
When operating at other than specified voltages (−4.2V, −4.5V, −4.8V) DC & AC Characteristics will vary slightly from specified values.

## DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2} = GND$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$, $T_A = 0°C$ to $+85°C$ unless otherwise specified[1,3]

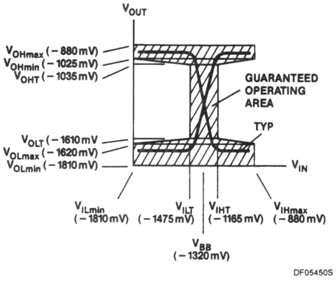
| PARAMETER | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] | |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | $V_{EE} = -4.2V$ | −1025 | | −870 | mV | $V_{IN} = V_{IHmax}$ or $V_{IN} = V_{ILmin}$ | Loading with 50Ω to −2.0V ±0.010V |
| | | $V_{EE} = -4.5V$ | −1025 | −955 | −880 | mV | | |
| | | $V_{EE} = -4.8V$ | −1035 | | −880 | mV | | |
| $V_{OHT}$ | HIGH level output threshold voltage | $V_{EE} = -4.2V$ | −1035 | | | mV | $V_{IN} = V_{IHmin}$ or $V_{IN} = V_{ILmax}$ | |
| | | $V_{EE} = -4.5V$ | −1035 | | | mV | | |
| | | $V_{EE} = -4.8V$ | −1045 | | | mV | | |
| $V_{OLT}$ | LOW level output threshold voltage | $V_{EE} = -4.2V$ | | | −1590 | mV | $V_{IN} = V_{IHmin}$ or $V_{IN} = V_{ILmax}$ | |
| | | $V_{EE} = -4.5V$ | | | −1610 | mV | | |
| | | $V_{EE} = -4.8V$ | | | −1610 | mV | | |
| $V_{OL}$ | LOW level output voltage | $V_{EE} = -4.2V$ | −1810 | | −1600 | mV | $V_{IN} = V_{IHmax}$ or $V_{IN} = V_{ILmin}$ | |
| | | $V_{EE} = -4.5V$ | −1810 | −1705 | −1620 | mV | | |
| | | $V_{EE} = -4.8V$ | −1830 | | −1620 | mV | | |
| $I_{IH}$ | HIGH level input current | | | | 350 | μA | $V_{IN} = V_{IHmax}$ | |
| $I_{IL}$ | LOW level input current | | 0.5 | | | μA | $V_{IN} = V_{ILmin}$ | |
| $-I_{EE}$ | $V_{EE}$ supply current | | 46 | 78 | 96 | mA | Inputs open | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | $V_{EE} = -4.2V$<br>$T_A = +25°C$ | | | 0.025 | V/V | | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | | 0.050 | V/V | | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 3.

# Backplane Driver

# 100126



**NOTES:**

| | |
|---|---|
| $V_{IHmax}$ | – Maximum HIGH level input voltage (the most positive $V_{IH}$). |
| $V_{IHT}$ | – HIGH level input threshold voltage. |
| $V_{ILT}$ | – LOW level input threshold voltage. |
| $V_{ILmin}$ | – Minimum LOW level input voltage (the most negative $V_{IL}$). |
| $V_{OHmax}$ | – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition. |
| $V_{OHmin}$ | – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition. |
| $V_{OHT}$ | – HIGH level output threshold voltage with the inputs set to their respective threshold levels. |
| $V_{OLT}$ | – LOW level output threshold voltage with the inputs set to their respective threshold levels. |
| $V_{OLmax}$ | – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions. |
| $V_{OLmin}$ | – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions. |
| $V_{BB}$ | – Reference bias voltage. The internally generated reference voltage which is used to set the input and output threshold level. |

**Figure 3. Transfer Characteristics**

## AC ELECTRICAL CHARACTERISTICS

### Ceramic DIP $V_{CC1} = V_{CC2} = \text{GND}$, $V_{EE} = -4.2\text{V} \pm 0.010\text{V}$ to $-4.8\text{V} \pm 0.010\text{V}$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 1.05 | 2.75 | 1.05 | 2.75 | 1.05 | 2.75 | ns | Figs. 4, 5, 6 |
| $t_{PHL}$ | $D_n$ to $Q_n$ | 1.05 | 2.75 | 1.05 | 2.75 | 1.05 | 2.75 | ns | |
| $t_{TLH}$ | Transition time | 1.15 | 3.30 | 1.15 | 3.30 | 1.05 | 3.30 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 1.15 | 3.30 | 1.15 | 3.30 | 1.05 | 3.30 | ns | |

### Ceramic DIP $V_{CC1} = V_{CC2} = \text{GND}$, $V_{EE} = -5.2\text{V} \pm 5\%$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 1.05 | 2.75 | 1.05 | 2.75 | 1.05 | 2.75 | ns | Figs. 4, 5, 6 |
| $t_{PHL}$ | $D_n$ to $Q_n$ | 1.05 | 2.75 | 1.05 | 2.75 | 1.05 | 2.75 | ns | |
| $t_{TLH}$ | Transition time | 1.15 | 3.30 | 1.15 | 3.30 | 1.05 | 3.30 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 1.15 | 3.30 | 1.15 | 3.30 | 1.05 | 3.30 | ns | |

### Flat Pack $V_{CC1} = V_{CC2} = \text{GND}$, $V_{EE} = -4.2\text{V} \pm 0.010\text{V}$ to $-4.8\text{V} \pm 0.010\text{V}$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 1.05 | 2.55 | 1.05 | 2.55 | 1.05 | 2.55 | ns | Figs. 4, 5, 6 |
| $t_{PHL}$ | $D_n$ to $Q_n$ | 1.05 | 2.55 | 1.05 | 2.55 | 1.05 | 2.55 | ns | |
| $t_{PLH}$ | Transition time | 1.15 | 3.30 | 1.15 | 3.30 | 1.05 | 3.30 | ns | |
| $t_{PHL}$ | 20% to 80%, 80% to 20% | 1.15 | 3.30 | 1.15 | 3.30 | 1.05 | 3.30 | ns | |

### Flat Pack $V_{CC1} = V_{CC2} = \text{GND}$, $V_{EE} = -5.2\text{V} \pm 5\%$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 1.05 | 2.55 | 1.05 | 2.55 | 1.05 | 2.55 | ns | Figs. 4, 5, 6 |
| $t_{PHL}$ | $D_n$ to $Q_n$ | 1.05 | 2.55 | 1.05 | 2.55 | 1.05 | 2.55 | ns | |
| $t_{PLH}$ | Transition time | 1.15 | 3.30 | 1.15 | 3.30 | 1.05 | 3.30 | ns | |
| $t_{PHL}$ | 20% to 80%, 80% to 20% | 1.15 | 3.30 | 1.15 | 3.30 | 1.05 | 3.30 | ns | |

## AC WAVEFORMS

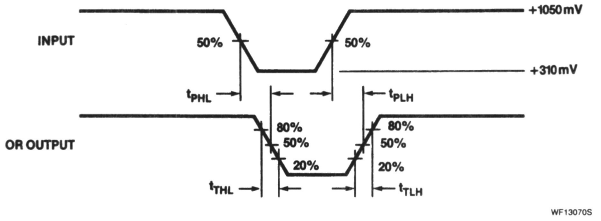
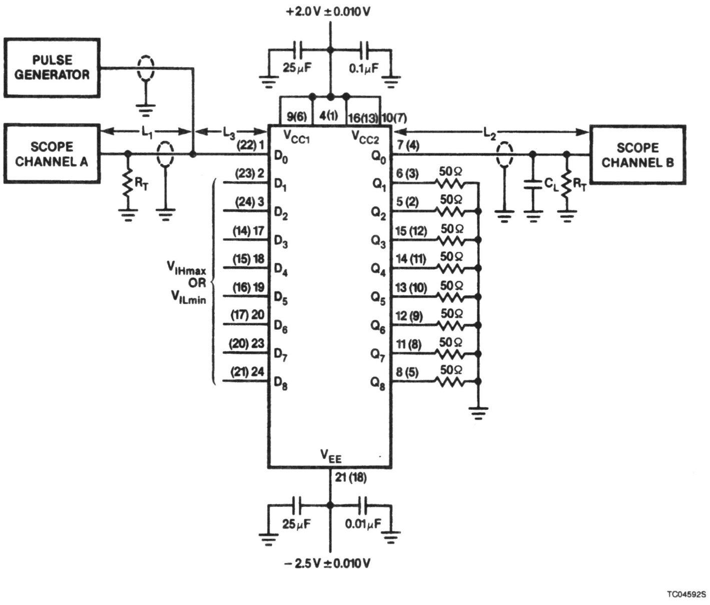

INPUT
50%
50%
+1050mV
+310mV
$t_{PHL}$
$t_{PLH}$
OR OUTPUT
80%
50%
20%
80%
50%
20%
$t_{THL}$
$t_{TLH}$
WF13070S

Figure 4. Propagation Delay and Transition Times

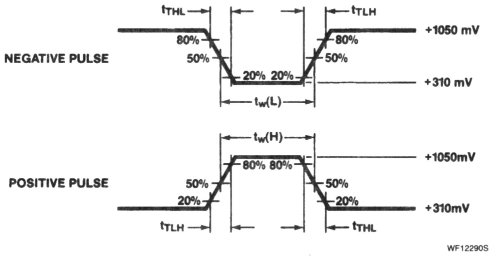
## TEST CIRCUITS AND WAVEFORMS


+2.0V ±0.010V
25µF
0.1µF
PULSE GENERATOR
SCOPE CHANNEL A
$L_1$
$L_3$
$R_T$
9(6)
4(1)
16(13)
10(7)
$V_{CC1}$
$V_{CC2}$
(22) 1
(23) 2
(24) 3
(14) 17
(15) 18
(16) 19
(17) 20
(20) 23
(21) 24
$D_0$
$D_1$
$D_2$
$D_3$
$D_4$
$D_5$
$D_6$
$D_7$
$D_8$
$V_{IHmax}$ OR $V_{ILmin}$
$Q_0$
$Q_1$
$Q_2$
$Q_3$
$Q_4$
$Q_5$
$Q_6$
$Q_7$
$Q_8$
7 (4)
6 (3)
5 (2)
15 (12)
14 (11)
13 (10)
12 (9)
11 (8)
8 (5)
50Ω
$L_2$
$C_L$
$R_T$
SCOPE CHANNEL B
$V_{EE}$
21 (18)
25µF
0.01µF
−2.5V ±0.010V
TC04592S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1µF and 25µF from GND to $V_{CC}$, 0.01µF and 25µF from GND to $V_{EE}$. (0.01 and 0.1µF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T = 50\Omega$ terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance $\leqslant 3pF$.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.

Figure 5. Test Circuit


NEGATIVE PULSE
$t_{THL}$
$t_{TLH}$
80%
50%
20%
20%
80%
50%
$t_w(L)$
+1050 mV
+310 mV
POSITIVE PULSE
$t_w(H)$
80%
80%
50%
20%
50%
20%
$t_{TLH}$
$t_{THL}$
+1050mV
+310mV
WF12290S

| INPUT PULSE REQUIREMENTS | | | | | |
|---|---|---|---|---|---|
| $V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -2.5V \pm 0.010V$, $V_T$ = GND (0V) | | | | | |
| **Family** | **Amplitude** | **Rep Rate** | **Pulse Width** | **$t_{TLH}$** | **$t_{THL}$** |
| 100K ECL | 740mVp-p | 1MHz | 500ns | 0.7 ±0.1ns | 0.7 ±0.1ns |

Figure 6. Input Pulse Definition

Signetics

# 100131
## Flip-Flop

**Triple D-Type Master-Slave Flip-Flop**
***Product Specification***

**ECL Products**

### DESCRIPTION

100131 has three D-type master-slave flip-flops, with direct and complement output, separate clock, set and reset. In addition, all three flip-flops have a common clock, set and reset.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 100131 | 1.3ns | 110mA |

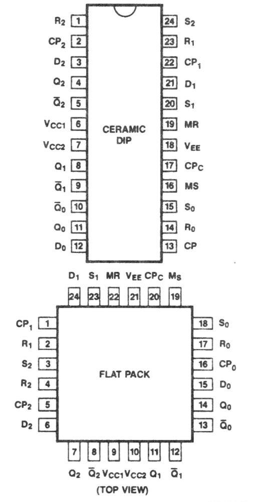
### ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} = GND$; $V_{EE} = -4.2V$ to $-4.8V$<br>$T_A = 0°C$ to $+85°C$ |
|---|---|
| Ceramic DIP | 100131F |
| Ceramic Flat Pack | 100131Y |

### PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_0 - D_2$ | Data Inputs |
| $CP_c$ | Common Clock Input |
| $CP_0 - CP_2$ | Clock Inputs |
| MS | Master Set Input |
| $S_0 - S_2$ | Set Inputs |
| MR | Master Reset Input |
| $R_0 - R_2$ | Reset Inputs |
| $Q_0 - Q_2$, $\overline{Q}_0 - \overline{Q}_2$ | Data Outputs |

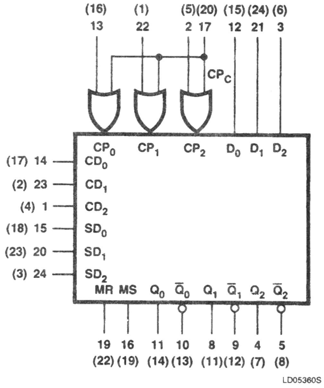
### PIN CONFIGURATION



R2 1
CP2 2
D2 3
Q2 4
Q̄2 5
VCC1 6
VCC2 7
Q1 8
Q̄1 9
Q̄0 10
Q0 11
D0 12
24 S2
23 R1
22 CP1
21 D1
20 S1
19 MR
18 VEE
17 CPC
16 MS
15 S0
14 R0
13 CP
CERAMIC DIP
D1 S1 MR VEE CPC MS
24 23 22 21 20 19
CP1 1
R1 2
S2 3
R2 4
CP2 5
D2 6
18 S0
17 R0
16 CP0
15 D0
14 Q0
13 Q̄0
FLAT PACK
7 8 9 10 11 12
Q2 Q̄2 VCC1 VCC2 Q1 Q̄1
(TOP VIEW)
CD09260S

Figure 1

### LOGIC SYMBOL



(16) 13
(1) 22
(5)(20) 2 17
(15) 12
(24) 21
(6) 3
CPC
CP0 CP1 CP2 D0 D1 D2
(17) 14 CD0
(2) 23 CD1
(4) 1 CD2
(18) 15 SD0
(23) 20 SD1
(3) 24 SD2
MR MS Q0 Q̄0 Q1 Q̄1 Q2 Q̄2
19 16 11 10 8 9 4 5
(22) (19) (14) (13) (11) (12) (7) (8)
LD05360S

Figure 2

## TRUTH TABLE

| INPUTS | | | | | | | OUTPUTS | |
|---|---|---|---|---|---|---|---|---|
| D | $CP_C$ | $CP_n$ | MS | S | MR | R | $Q_n + 1$ | $\overline{Q}_n + 1$ |
| X | X | X | L | L | H | X | L | H |
| X | X | X | L | L | X | H | L | H |
| X | X | X | H | X | L | L | H | L |
| X | X | X | X | H | L | L | H | L |
| X | X | ↑ | L | L | L | L | $Q_n$ | $\overline{Q}_n$ |
| X | ↑ | H | L | L | L | L | $Q_n$ | $\overline{Q}_n$ |
| X | X | X | L | L | L | L | $Q_n$ | $\overline{Q}_n$ |
| H | ↑ | L | L | L | L | L | H | L |
| L | ↑ | L | L | L | L | L | L | H |
| H | L | ↑ | L | L | L | L | H | L |
| L | L | ↑ | L | L | L | L | L | H |

D: Data input; $CP_C$: Common Clock; $CK_i$: Clock; MS: Master Set; S: Set; MR: Master Reset; R: Reset; Q: Direct output; $\overline{Q}$: Complement output; n: State before transition; n + 1: State after transition; ↑ : LOW to HIGH transition.

Data enters a master when both clock and common clock are LOW, and transfers to the slave when the clock or master clock (or both) go HIGH. If the set (or master set) is HIGH while the reset (or master reset) is HIGH, the output is undefined.

Positive Logic:
H = HIGH state (more positive voltage) = 1
L = LOW state (less positive voltage) = 0
X = Don't Care

## Flip-Flop

## 100131

**ABSOLUTE MAXIMUM RATINGS** (Operation beyond the limits set forth in this table may impair useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | 10K ECL | UNIT |
|---|---|---|---|
| $V_{EE}$ | Supply voltage ($V_{CC1} = V_{CC2}$ = GND) | -7.0 to 0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | $V_{EE}$ to +0.5 | V |
| $I_O$ | Output source current | -55 | mA |
| $T_S$ | Storage temperature | -65 to +150 | °C |
| $T_J$ | Maximum junction temperature | +150 | °C |

### DC OPERATING CONDITIONS

| PARAMETER | | | | 100K ECL | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | -4.2 | -4.5 | -4.8 | V |
| $V_{EE}$ | Supply voltage (negative) when operating with 10K ECL family | | | | | -5.7 | V |
| $V_{IH}$ | HIGH level input voltage | $V_{CC1} = V_{CC2}$ = GND<br>$T_A$ = 0°C to +85°C | $V_{EE}$ = -4.2V | -1150 | | -880 | mV |
| | | | $V_{EE}$ = -4.5V | -1165 | | | |
| | | | $V_{EE}$ = -4.8V | | | | |
| $V_{IHT}$ | HIGH level input threshold voltage | | $V_{EE}$ = -4.2V | -1150 | | | mV |
| | | | $V_{EE}$ = -4.5V | -1165 | | | mV |
| | | | $V_{EE}$ = -4.8V | | | | |
| $V_{ILT}$ | LOW level input threshold voltage | | $V_{EE}$ = -4.2V | | | -1475 | mV |
| | | | $V_{EE}$ = -4.5V | | | | |
| | | | $V_{EE}$ = -4.8V | | | -1490 | mV |
| $V_{IL}$ | LOW level input voltage | | $V_{EE}$ = -4.2V | -1810 | | -1475 | mV |
| | | | $V_{EE}$ = -4.5V | | | | |
| | | | $V_{EE}$ = -4.8V | | | -1490 | |
| $T_A$ | Operating ambient temperature | | | 0 | +25 | +85 | °C |

**NOTE:**
When operating at other than specified voltages (-4.2V, -4.5V, -4.8V) DC & AC Characteristics will vary slightly from specified values.

# Flip-Flop

# 100131

## DC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$, $T_A = 0°C$ to $+85°C$ unless otherwise specified[1, 3]

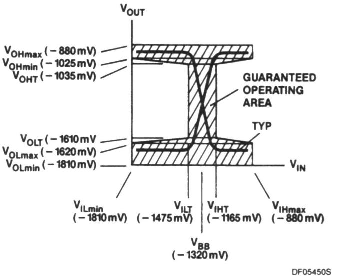
| PARAMETER | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] | |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | $V_{EE} = -4.2V$ | −1025 | | −870 | mV | $V_{IN} = V_{IHmax}$ or $V_{IN} = V_{ILmin}$ | Loading with 50Ω to −2.0V ±0.010V |
| | | $V_{EE} = -4.5V$ | −1025 | −955 | −880 | mV | | |
| | | $V_{EE} = -4.8V$ | −1035 | | −880 | mV | | |
| $V_{OHT}$ | HIGH level output threshold voltage | $V_{EE} = -4.2V$ | −1035 | | | mV | $V_{IN} = V_{IHmin}$ or $V_{IN} = V_{ILmax}$ | |
| | | $V_{EE} = -4.5V$ | −1035 | | | mV | | |
| | | $V_{EE} = -4.8V$ | −1045 | | | mV | | |
| $V_{OLT}$ | LOW level output threshold voltage | $V_{EE} = -4.2V$ | | | −1590 | mV | $V_{IN} = V_{IHmin}$ or $V_{IN} = V_{ILmax}$ | |
| | | $V_{EE} = -4.5V$ | | | −1610 | mV | | |
| | | $V_{EE} = -4.8V$ | | | −1610 | mV | | |
| $V_{OL}$ | LOW level output voltage | $V_{EE} = -4.2V$ | −1810 | | −1600 | mV | $V_{IN} = V_{IHmax}$ or $V_{IN} = V_{ILmin}$ | |
| | | $V_{EE} = -4.5V$ | −1810 | −1705 | −1620 | mV | | |
| | | $V_{EE} = -4.8V$ | −1830 | | −1620 | mV | | |
| $I_{IH}$ | HIGH level input current | $D_n$, $CP_n$ | | | 240 | μA | $V_{IN} = V_{IHmax}$ | |
| | | MC, MS, MR, | | | 450 | μA | | |
| | | $R_n$, $S_n$ | | | 530 | μA | | |
| $I_{IL}$ | LOW level input current | | 0.5 | | | μA | $V_{IN} = V_{ILmin}$ | |
| $-I_{EE}$ | $V_{EE}$ supply current | | 74 | 110 | 149 | mA | Inputs open | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | $V_{EE} = -4.2V$<br>$T_A = +25°C$ | | | 0.035 | V/V | | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | | 0.070 | V/V | | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 3.

## Flip-Flop

## 100131



**NOTES:**

$V_{IHmax}$ – Maximum HIGH level input voltage (the most positive $V_{IH}$).
$V_{IHT}$ – HIGH level input threshold voltage.
$V_{ILT}$ – LOW level input threshold voltage.
$V_{ILmin}$ – Minimum LOW level input voltage (the most negative $V_{IL}$).
$V_{OHmax}$ – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition.
$V_{OHmin}$ – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition.
$V_{OHT}$ – HIGH level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLT}$ – LOW level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLmax}$ – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions.
$V_{OLmin}$ – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions.
$V_{BB}$ – Reference bias voltage (the internally generated reference voltage which is used to set the input and output threshold level).

**Figure 3. Transfer Characteristics**

## AC ELECTRICAL CHARACTERISTICS

**Ceramic DIP** $V_{CC1} = V_{CC2} = \text{GND}$, $V_{EE} = -4.2\text{V} \pm 0.010\text{V}$ to $-4.8\text{V} \pm 0.010\text{V}$

| | PARAMETER | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | | |
| $f_{MAX}$ | Maximum toggle frequency | 350 | | 350 | | 350 | | MHz | Figs. 3, 8 | |
| $t_{PLH}$ | Propagation delay | 0.75 | 2.40 | 0.75 | 2.15 | 0.70 | 2.30 | ns | | |
| $t_{PHL}$ | MC to $Q_n$ | 0.75 | 2.40 | 0.75 | 2.15 | 0.70 | 2.30 | ns | | |
| $t_{PLH}$ | Propagation delay | 0.70 | 2.20 | 0.70 | 2.00 | 0.70 | 2.20 | ns | Figs. 3, 7, 8 | |
| $t_{PHL}$ | $CP_n$ to $Q_n$, | 0.70 | 2.20 | 0.70 | 2.00 | 0.70 | 2.20 | ns | | |
| $t_{PLH}$ | Propagation delay | 1.10 | 2.70 | 1.05 | 2.60 | 1.05 | 2.70 | ns | $CP_n$ = LOW | Figs. 4, 6, 8 |
| $t_{PHL}$ | MS, MR to $Q_n$ | 1.10 | 2.70 | 1.05 | 2.60 | 1.05 | 2.70 | ns | | |
| $t_{PLH}$ | Propagation delay | 1.10 | 3.05 | 1.10 | 2.95 | 1.10 | 3.05 | ns | $CP_n$ = HIGH | |
| $t_{PHL}$ | MS, MR to $Q_n$ | 1.10 | 3.05 | 1.10 | 2.95 | 1.10 | 3.05 | ns | | |
| $t_{PLH}$ | Propagation delay | 0.65 | 1.90 | 0.70 | 1.70 | 0.70 | 1.90 | ns | $CP_n$ = LOW | |
| $t_{PHL}$ | $R_n$, $S_n$ to $Q_n$ | 0.65 | 1.90 | 0.70 | 1.70 | 0.70 | 1.90 | ns | | |
| $t_{PLH}$ | Propagation delay | 0.70 | 2.10 | 0.70 | 2.00 | 0.70 | 2.20 | ns | $CP_n$ = HIGH | |
| $t_{PHL}$ | $R_n$, $S_n$ to $Q_n$ | 0.70 | 2.10 | 0.70 | 2.00 | 0.70 | 2.20 | ns | | |
| $t_{TLH}$ | Transition time | 0.45 | 2.00 | 0.45 | 1.60 | 0.45 | 1.70 | ns | Figs. 4, 6, 8 | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 2.00 | 0.45 | 1.60 | 0.45 | 1.70 | ns | | |
| $t_s$ | Setup time<br>$D_n$ to $CP_n$ | 0.90 | | 0.70 | | 0.90 | | ns | Figs. 5, 8 | |
| $t_h$ | Hold time<br>$D_n$ to $CP_n$ | 0.60 | | 0.60 | | 0.80 | | ns | | |
| $t_r$ | Release time<br>$R_n$, $S_n$ to $CP_n$ | 1.50 | | 1.30 | | 1.50 | | ns | Figs. 4, 8 | |
| $t_r$ | Release time<br>MR, MS to $CP_n$ | 2.50 | | 2.30 | | 2.50 | | ns | | |
| $t_w(H)$ | Pulse width HIGH<br>MR, MS, $R_n$, $S_n$, $CP_n$ | 2.50 | | 2.50 | | 2.50 | | ns | Figs. 3, 4, 8 | |

## AC ELECTRICAL CHARACTERISTICS

**Ceramic DIP** $V_{CC1} = V_{CC2} = \text{GND}$, $V_{EE} = -5.2V \pm 5\%$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | | |
| $f_{MAX}$ | Maximum toggle frequency | 350 | | 350 | | 350 | | MHz | Figs. 3, 8 | |
| $t_{PLH}$ | Propagation delay | 0.75 | 2.40 | 0.75 | 2.15 | 0.70 | 2.30 | ns | | |
| $t_{PHL}$ | MC to $Q_n$ | 0.75 | 2.40 | 0.75 | 2.15 | 0.70 | 2.30 | ns | | |
| $t_{PLH}$ | Propagation delay | 0.70 | 2.20 | 0.70 | 2.00 | 0.70 | 2.20 | ns | Figs. 3, 7, 8 | |
| $t_{PHL}$ | $CP_n$ to $Q_n$, | 0.70 | 2.20 | 0.70 | 2.00 | 0.70 | 2.20 | ns | | |
| $t_{PLH}$ | Propagation delay | 1.10 | 2.70 | 1.05 | 2.60 | 1.05 | 2.70 | ns | $CP_n$ = LOW | Figs. 4, 6, 8 |
| $t_{PHL}$ | MS, MR to $Q_n$ | 1.10 | 2.70 | 1.05 | 2.60 | 1.05 | 2.70 | ns | | |
| $t_{PLH}$ | Propagation delay | 1.10 | 3.05 | 1.10 | 2.95 | 1.10 | 3.05 | ns | $CP_n$ = HIGH | |
| $t_{PHL}$ | MS, MR to $Q_n$ | 1.10 | 3.05 | 1.10 | 2.95 | 1.10 | 3.05 | ns | | |
| $t_{PLH}$ | Propagation delay | 0.65 | 1.90 | 0.70 | 1.70 | 0.70 | 1.90 | ns | $CP_n$ = LOW | |
| $t_{PHL}$ | $R_n$, $S_n$ to $Q_n$ | 0.65 | 1.90 | 0.70 | 1.70 | 0.70 | 1.90 | ns | | |
| $t_{PLH}$ | Propagation delay | 0.70 | 2.10 | 0.70 | 2.00 | 0.70 | 2.20 | ns | $CP_n$ = HIGH | |
| $t_{PHL}$ | $R_n$, $S_n$ to $Q_n$ | 0.70 | 2.10 | 0.70 | 2.00 | 0.70 | 2.20 | ns | | |
| $t_{TLH}$ | Transition time | 0.45 | 2.00 | 0.45 | 1.60 | 0.45 | 1.70 | ns | Figs. 4, 6, 8 | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 2.00 | 0.45 | 1.60 | 0.45 | 1.70 | ns | | |
| $t_s$ | Setup time<br>$D_n$ to $CP_n$ | 0.90 | | 0.70 | | 0.90 | | ns | Figs. 5, 8 | |
| $t_h$ | Hold time<br>$D_n$ to $CP_n$ | 0.60 | | 0.60 | | 0.80 | | ns | | |
| $t_r$ | Release time<br>$R_n$, $S_n$ to $CP_n$ | 1.50 | | 1.30 | | 1.50 | | ns | Figs. 4, 8 | |
| $t_r$ | Release time<br>MR, MS to $CP_n$ | 2.50 | | 2.30 | | 2.50 | | ns | | |
| $t_w(H)$ | Pulse width HIGH<br>MR, MS, $R_n$, $S_n$, $CP_n$ | 2.50 | | 2.50 | | 2.50 | | ns | Figs. 3, 4, 8 | |

## AC ELECTRICAL CHARACTERISTICS

**Flat Pack** $V_{CC1} = V_{CC2} = \text{GND}$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | | |
| $f_{MAX}$ | Maximum toggle frequency | 350 | | 350 | | 350 | | MHz | Figs. 3, 8 | |
| $t_{PLH}$ | Propagation delay | 0.75 | 2.20 | 0.75 | 1.95 | 0.70 | 2.10 | ns | | |
| $t_{PHL}$ | MC to $Q_n$ | 0.75 | 2.20 | 0.75 | 1.95 | 0.70 | 2.10 | ns | | |
| $t_{PLH}$ | Propagation delay | 0.70 | 2.00 | 0.70 | 1.80 | 0.70 | 2.00 | ns | Figs. 3, 7, 8 | |
| $t_{PHL}$ | $CP_n$ to $Q_n$ | 0.70 | 2.00 | 0.70 | 1.80 | 0.70 | 2.00 | ns | | |
| $t_{PLH}$ | Propagation delay | 1.10 | 2.50 | 1.05 | 2.40 | 1.05 | 2.50 | ns | $CP_n$ = LOW | Figs. 4, 6, 8 |
| $t_{PHL}$ | MS, MR to $Q_n$ | 1.10 | 2.50 | 1.05 | 2.40 | 1.05 | 2.50 | ns | | |
| $t_{PLH}$ | Propagation delay | 1.15 | 2.85 | 1.05 | 2.75 | 1.05 | 2.85 | ns | $CP_n$ = HIGH | |
| $t_{PHL}$ | MS, MR to $Q_n$ | 1.15 | 2.85 | 1.05 | 2.75 | 1.05 | 2.85 | ns | | |
| $t_{PLH}$ | Propagation delay | 0.65 | 1.70 | 0.70 | 1.50 | 0.70 | 1.70 | ns | $CP_n$ = LOW | |
| $t_{PHL}$ | $R_n$, $S_n$ to $Q_n$ | 0.65 | 1.70 | 0.70 | 1.50 | 0.70 | 1.70 | ns | | |
| $t_{PLH}$ | Propagation delay | 0.70 | 1.90 | 0.70 | 1.80 | 0.70 | 2.00 | ns | $CP_n$ = HIGH | |
| $t_{PHL}$ | $R_n$, $S_n$ to $Q_n$ | 0.70 | 1.90 | 0.70 | 1.80 | 0.70 | 2.00 | ns | | |
| $t_{TLH}$ | Transition time | 0.45 | 2.00 | 0.45 | 1.60 | 0.45 | 1.70 | ns | Figs. 4, 6, 8 | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 2.00 | 0.45 | 1.60 | 0.45 | 1.70 | ns | | |
| $t_s$ | Setup time $D_n$ to $CP_n$ | 0.80 | | 0.60 | | 0.80 | | ns | Figs. 5, 8 | |
| $t_h$ | Hold time $D_n$ to $CP_n$ | 0.50 | | 0.50 | | 0.70 | | ns | | |
| $t_r$ | Release time $R_n$, $S_n$ to $CP_n$ | 1.40 | | 1.20 | | 1.40 | | ns | Figs. 4, 8 | |
| $t_r$ | Release time MR, MS to $CP_n$ | 2.40 | | 2.20 | | 2.40 | | ns | | |
| $t_w(H)$ | Pulse width HIGH MR, MS, $R_n$, $S_n$, $CP_n$ | 2.50 | | 2.50 | | 2.50 | | ns | Figs. 3, 4, 8 | |

## AC ELECTRICAL CHARACTERISTICS

**Flat Pack** $V_{CC1} = V_{CC2} = \text{GND}$, $V_{EE} = -5.2\text{V} \pm 5\%$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | | |
| $f_{MAX}$ | Maximum toggle frequency | 350 | | 350 | | 350 | | MHz | Figs. 3, 8 | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>MC to $Q_n$ | 0.75<br>0.75 | 2.20<br>2.20 | 0.75<br>0.75 | 1.95<br>1.95 | 0.70<br>0.70 | 2.10<br>2.10 | ns<br>ns | | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$CP_n$ to $Q_n$ | 0.70<br>0.70 | 2.00<br>2.00 | 0.70<br>0.70 | 1.80<br>1.80 | 0.70<br>0.70 | 2.00<br>2.00 | ns<br>ns | Figs. 3, 7, 8 | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>MS, MR to $Q_n$ | 1.10<br>1.10 | 2.50<br>2.50 | 1.05<br>1.05 | 2.40<br>2.40 | 1.05<br>1.05 | 2.50<br>2.50 | ns<br>ns | $CP_n$ = LOW | Figs. 4, 6, 8 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>MS, MR to $Q_n$ | 1.15<br>1.15 | 2.85<br>2.85 | 1.05<br>1.05 | 2.75<br>2.75 | 1.05<br>1.05 | 2.85<br>2.85 | ns<br>ns | $CP_n$ = HIGH | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$R_n$, $S_n$ to $Q_n$ | 0.65<br>0.65 | 1.70<br>1.70 | 0.70<br>0.70 | 1.50<br>1.50 | 0.70<br>0.70 | 1.70<br>1.70 | ns<br>ns | $CP_n$ = LOW | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$R_n$, $S_n$ to $Q_n$ | 0.70<br>0.70 | 1.90<br>1.90 | 0.70<br>0.70 | 1.80<br>1.80 | 0.70<br>0.70 | 2.00<br>2.00 | ns<br>ns | $CP_n$ = HIGH | |
| $t_{TLH}$<br>$t_{THL}$ | Transition time<br>20% to 80%, 80% to 20% | 0.45<br>0.45 | 2.00<br>2.00 | 0.45<br>0.45 | 1.60<br>1.60 | 0.45<br>0.45 | 1.70<br>1.70 | ns<br>ns | Figs. 4, 6, 8 | |
| $t_s$ | Setup time<br>$D_n$ to $CP_n$ | 0.80 | | 0.60 | | 0.80 | | ns | Figs. 5, 8 | |
| $t_h$ | Hold time<br>$D_n$ to $CP_n$ | 0.50 | | 0.50 | | 0.70 | | ns | | |
| $t_r$ | Release time<br>$R_n$, $S_n$ to $CP_n$ | 1.40 | | 1.20 | | 1.40 | | ns | Figs. 4, 8 | |
| $t_r$ | Release time<br>MR, MS to $CP_n$ | 2.40 | | 2.20 | | 2.40 | | ns | | |
| $t_w(H)$ | Pulse width HIGH<br>MR, MS, $R_n$, $S_n$, $CP_n$ | 2.50 | | 2.50 | | 2.50 | | ns | Figs. 3, 4, 8 | |

## AC WAVEFORMS

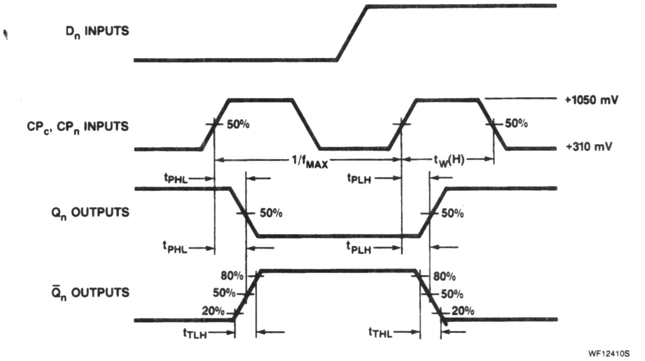

D<sub>n</sub> INPUTS
CP<sub>c</sub>, CP<sub>n</sub> INPUTS
Q<sub>n</sub> OUTPUTS
Q̄<sub>n</sub> OUTPUTS
+1050 mV
+310 mV
50%
1/f<sub>MAX</sub>
t<sub>W</sub>(H)
t<sub>PHL</sub>
t<sub>PLH</sub>
80%
20%
t<sub>TLH</sub>
t<sub>THL</sub>
WF12410S

Figure 4. Propagation Delay for Clock to Outputs and Transition Time

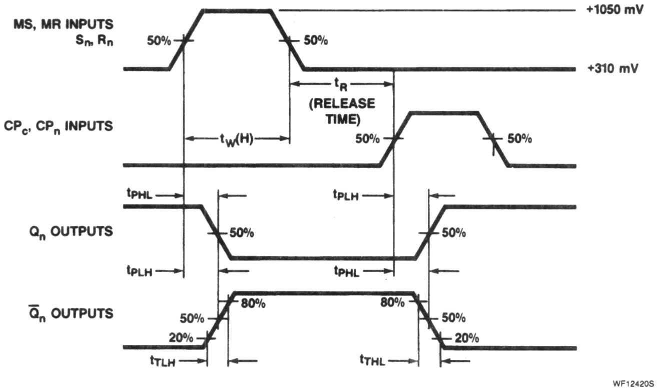

MS, MR INPUTS
S<sub>n</sub>, R<sub>n</sub>
CP<sub>c</sub>, CP<sub>n</sub> INPUTS
Q<sub>n</sub> OUTPUTS
Q̄<sub>n</sub> OUTPUTS
+1050 mV
+310 mV
50%
t<sub>R</sub>
(RELEASE TIME)
t<sub>W</sub>(H)
t<sub>PHL</sub>
t<sub>PLH</sub>
80%
20%
t<sub>TLH</sub>
t<sub>THL</sub>
WF12420S

Figure 5. Propagation Delay for Sets and Resets to Outputs

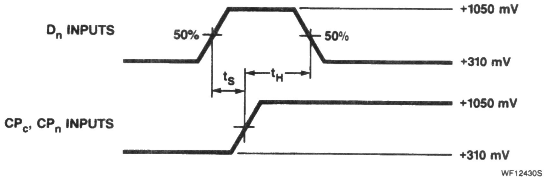
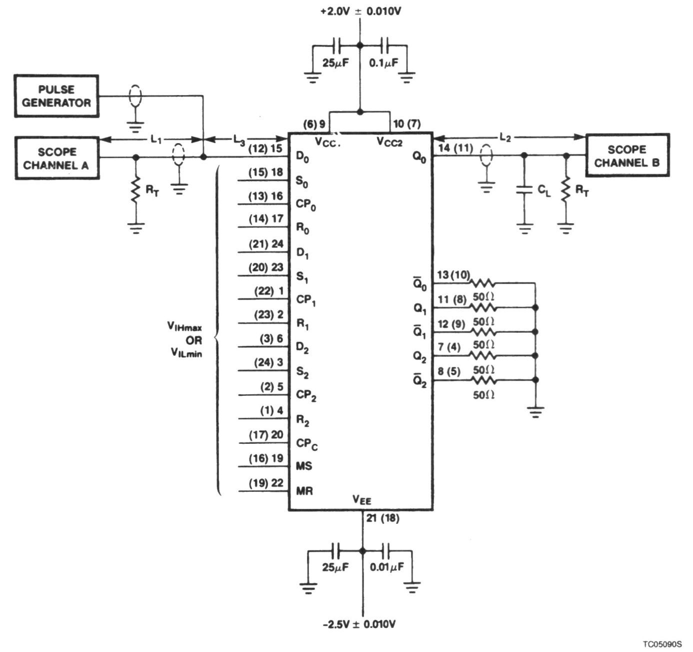

D<sub>n</sub> INPUTS
CP<sub>c</sub>, CP<sub>n</sub> INPUTS
50%
t<sub>S</sub>
t<sub>H</sub>
+1050 mV
+310 mV
WF12430S

Figure 6. Data Setup and Hold Time

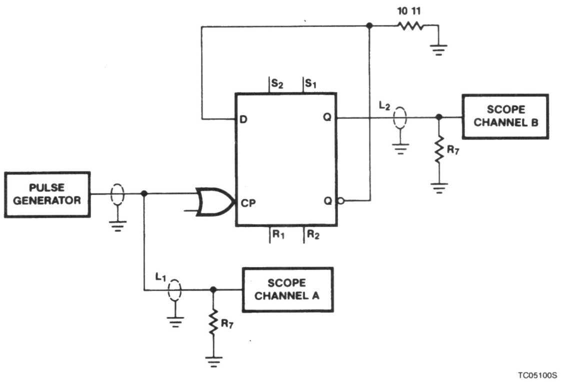
## TEST CIRCUITS AND WAVEFORMS


+2.0V ± 0.010V
25μF
0.1μF
PULSE GENERATOR
SCOPE CHANNEL A
L1
L3
$R_T$
(6) 9
10 (7)
$V_{CC}$
$V_{CC2}$
(12) 15 $D_0$
(15) 18 $S_0$
(13) 16 $CP_0$
(14) 17 $R_0$
(21) 24 $D_1$
(20) 23 $S_1$
(22) 1 $CP_1$
(23) 2 $R_1$
(3) 6 $D_2$
(24) 3 $S_2$
(2) 5 $CP_2$
(1) 4 $R_2$
(17) 20 $CP_C$
(16) 19 MS
(19) 22 MR
$V_{IHmax}$ OR $V_{ILmin}$
$Q_0$
14 (11)
L2
SCOPE CHANNEL B
$C_L$
$R_T$
$\bar{Q}_0$ 13 (10)
$Q_1$ 11 (8) 50Ω
$\bar{Q}_1$ 12 (9) 50Ω
$Q_2$ 7 (4) 50Ω
$\bar{Q}_2$ 8 (5) 50Ω
50Ω
$V_{EE}$
21 (18)
25μF
0.01μF
-2.5V ± 0.010V
TC05090S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1μF and 25μF from GND to $V_{CC}$, 0.01μF and 25μF from GND to $V_{EE}$. (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance ≤ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.
11. Pin connections are for Flat Pack and in parentheses for Ceramic DIP.

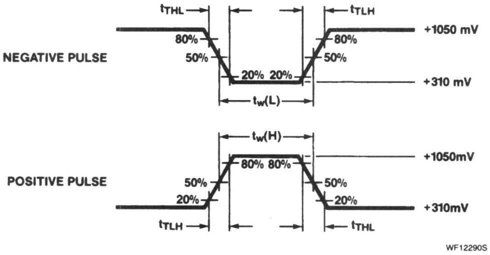
**Figure 7. Test Circuit**


10 11
$S_2$
$S_1$
D
Q
CP
$\bar{Q}$
$R_1$
$R_2$
L2
SCOPE CHANNEL B
$R_7$
PULSE GENERATOR
L1
SCOPE CHANNEL A
$R_7$
TC05100S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1μF and 25μF from GND to $V_{CC}$, 0.01μF and 25μF from GND to $V_{EE}$. (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance ≤ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.
11. Pin connections are for Flat Pack and in parentheses for Ceramic DIP.

**Figure 8. Toggle Frequency Test Circuit**


NEGATIVE PULSE
POSITIVE PULSE
tTHL
tTLH
80%
50%
20%
tw(L)
tw(H)
+1050 mV
+310 mV
+1050mV
+310mV
WF12290S

| INPUT PULSE REQUIREMENTS<br>$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -2.5V \pm 0.010V$, $V_T$ = GND (0V) | | | | | |
|---|---|---|---|---|---|
| **Family** | **Amplitude** | **Rep Rate** | **Pulse Width** | $t_{TLH}$ | $t_{THL}$ |
| 100K ECL | 740mVp-p | 1MHz | 500ns | 0.7 ±0.1ns | 0.7 ±0.1ns |

Figure 9. Input Pulse Definition

Signetics

# 100136
## Counter/Shift Register

**4-Stage Counter/Shift Register**
***Product Specification***

### DESCRIPTION

100136 operates as a 4-bit Up/Down Counter, or as a 4-bit Left/Right Shift Register; the operating mode is fixed by three selection inputs, $S_n$. These selection inputs also enable parallel loading, synchronous reset or complement of flip-flop outputs. $D_0$ is the serial input for left shifting, $D_3$ for right shifting. A carry output $\overline{TC}$ goes low for 15 value in up counting mode, for 0 in down counting mode. In shifting mode, $\overline{TC}$ repeats output $Q_3$. A HIGH level on MR enables asynchronous master reset. Two count enables ($\overline{CEP}$, $\overline{CET}$) allow multi-stage counter cascading.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 100136 | 1.8ns | 210mA |

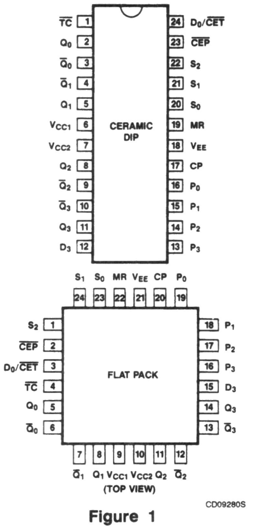
### ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC1} = V_{CC2} =$ GND; $V_{EE} = -4.2V$ to $-4.8V$ $T_A = 0°C$ to $+85°C$ |
|---|---|
| Ceramic DIP | 100136F |
| Ceramic Flat Pack | 100136Y |

### PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_3$ | Serial Data Input |
| $P_0 - P_3$ | Preset Inputs |
| CP | Clock Input |
| $D_0/\overline{CET}$ | Serial Data Input/Count Enable Trickle Input (Active LOW) |
| $\overline{CEP}$ | Count Enable Parallel Input (Active LOW) |
| $S_0 - S_2$ | Select Inputs |
| MR | Master Reset Input |
| $\overline{TC}$ | Terminal Count Output |
| $Q_0 - Q_3$, $\overline{Q}_0 - \overline{Q}_3$ | Data Outputs |

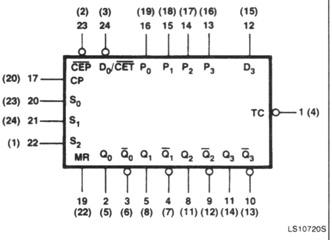
### PIN CONFIGURATION



$\overline{TC}$ 1
$Q_0$ 2
$\overline{Q}_0$ 3
$\overline{Q}_1$ 4
$Q_1$ 5
$V_{CC1}$ 6
$V_{CC2}$ 7
$Q_2$ 8
$\overline{Q}_2$ 9
$\overline{Q}_3$ 10
$Q_3$ 11
$D_3$ 12
24 $D_0/\overline{CET}$
23 $\overline{CEP}$
22 $S_2$
21 $S_1$
20 $S_0$
19 MR
18 $V_{EE}$
17 CP
16 $P_0$
15 $P_1$
14 $P_2$
13 $P_3$
CERAMIC DIP
$S_1$ $S_0$ MR $V_{EE}$ CP $P_0$
24 23 22 21 20 19
$S_2$ 1
$\overline{CEP}$ 2
$D_0/\overline{CET}$ 3
$\overline{TC}$ 4
$Q_0$ 5
$\overline{Q}_0$ 6
18 $P_1$
17 $P_2$
16 $P_3$
15 $D_3$
14 $Q_3$
13 $\overline{Q}_3$
FLAT PACK
7 8 9 10 11 12
$\overline{Q}_1$ $Q_1$ $V_{CC1}$ $V_{CC2}$ $Q_2$ $\overline{Q}_2$
(TOP VIEW)
CD09280S

Figure 1

### LOGIC SYMBOL



(2) 23
(3) 24
(19) 16
(18) 15
(17) 14
(16) 13
(15) 12
$\overline{CEP}$
$D_0/\overline{CET}$
$P_0$
$P_1$
$P_2$
$P_3$
$D_3$
(20) 17 CP
(23) 20 $S_0$
(24) 21 $S_1$
(1) 22 $S_2$
TC 1 (4)
MR $Q_0$ $\overline{Q}_0$ $Q_1$ $\overline{Q}_1$ $Q_2$ $\overline{Q}_2$ $Q_3$ $\overline{Q}_3$
19 2 3 5 4 8 9 11 10
(22) (5) (6) (8) (7) (11) (12) (14) (13)
LS10720S

Figure 2

## LOGIC DIAGRAM

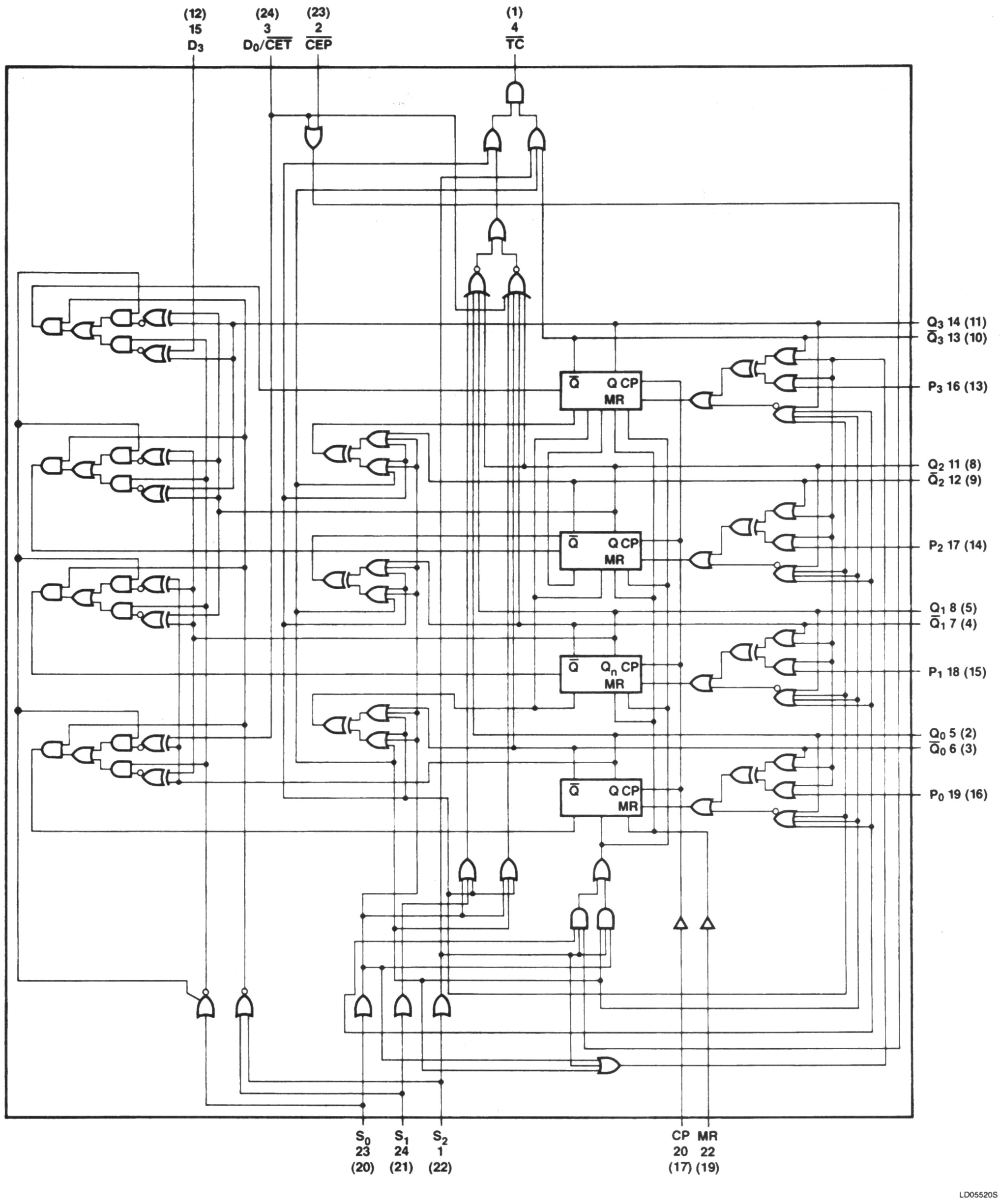

(12)
15
D3
(24)
3
D0/CET
(23)
2
CEP
(1)
4
TC
Q̄
Q CP
MR
Q̄
Q CP
MR
Q̄
Qn CP
MR
Q̄
Q CP
MR
Q3 14 (11)
Q̄3 13 (10)
P3 16 (13)
Q2 11 (8)
Q̄2 12 (9)
P2 17 (14)
Q1 8 (5)
Q̄1 7 (4)
P1 18 (15)
Q0 5 (2)
Q̄0 6 (3)
P0 19 (16)
S0
23
(20)
S1
24
(21)
S2
1
(22)
CP
20
(17)
MR
22
(19)
LD05520S

Figure 3

# Counter/Shift Register

# 100136

## FUNCTION TABLE

| MR | $S_0$ | $S_1$ | $S_2$ | $\overline{CEP}$ | $D_0/\overline{CET}$ | $D_3$ | CP | $Q_0$ | $Q_1$ | $Q_2$ | $Q_3$ | TC | MODE |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| H | L | L | L | X | X | X | X | L | L | L | L | L | ▲ |
| ▲ | L | H | L | ▲ | X | ▲ | ▲ | ▲ | ▲ | ▲ | ▲ | L | |
| | H | H | L | | X | | | | | | | L | |
| | L | L | H | | L | | | | | | | L | Asynchronous |
| | L | L | H | | H | | | | | | | H | Master reset |
| | L | H | H | | X | | | | | | | H | |
| | H | H | H | | X | | | | | | | H | |
| ▼ | H | L | L | ▼ | X | ▼ | ▼ | ▼ | ▼ | ▼ | ▼ | L | |
| H | H | L | H | X | X | X | X | L | L | L | L | H | ▼ |
| L | L | L | L | X | X | X | ↑ | $P_0$ | $P_1$ | $P_2$ | $P_3$ | L | Preset |
| L | L | L | H | L | L | X | ↑ | $(Q_{0-3})$ minus 1 | | | | ① | Count Down |
| L | L | L | H | H | L | X | X | $Q_0$ | $Q_1$ | $Q_2$ | $Q_3$ | ① | Count Down with $\overline{CEP}$ not active |
| L | L | L | H | X | H | X | X | $Q_0$ | $Q_1$ | $Q_2$ | $Q_3$ | H | Count Down with $\overline{CET}$ not active |
| L | L | H | L | X | X | X | ↑ | $Q_1$ | $Q_2$ | $Q_3$ | $D_3$ | $D_3$ | Shift Right |
| L | L | H | H | L | L | X | ↑ | $(Q_{0-3})$ plus 1 | | | | ② | Count Up |
| L | L | H | H | H | L | X | X | $Q_0$ | $Q_1$ | $Q_2$ | $Q_3$ | ② | Count Up with $\overline{CEP}$ not active |
| L | L | H | H | X | H | X | X | $Q_0$ | $Q_1$ | $Q_2$ | $Q_3$ | H | Count Up with $\overline{CET}$ not active |
| L | H | L | L | X | X | X | ↑ | $\overline{Q_0}$ | $\overline{Q_1}$ | $\overline{Q_2}$ | $\overline{Q_3}$ | L | Invert |
| L | H | L | H | X | X | X | ↑ | L | L | L | L | H | Clear |
| L | H | H | L | | X | X | ↑ | $D_0$ | $Q_0$ | $Q_1$ | $Q_2$ | $Q_2$ | Shift Left |
| L | H | H | H | X | X | X | X | $Q_0$ | $Q_1$ | $Q_2$ | $Q_3$ | H | Hold |

① L if $Q_0 - Q_3$ = LLLL : ② L if $Q_0 - Q_3$ = HHHH
H if $Q_0 - Q_3 \neq$ LLLL : H if $Q_0 - Q_3 \neq$ HHHH

Positive Logic:
H = HIGH state (the most positive voltage) = 1
L = LOW state (the less positive voltage) = 0
X = Don't Care
↑ = LOW to HIGH transition

## SELECTION TABLE

| $S_0$ | $S_1$ | $S_2$ | OPERATING MODES (SYNCHRONOUS) |
|---|---|---|---|
| L | L | L | Parallel load: Data available on $P_n$ will be loaded with next clock pulse. |
| L | L | H | Down counter: Each clock pulse decreases the counter value. |
| L | H | L | Right shift: Each clock pulse shifts $D_3$ to $Q_3$, $Q_n$ to $Q_{n-1}$. |
| L | H | H | Up counter: Each clock pulse increases the counter value. |
| H | L | L | Complement mode: contents of flip-flop can be synchronously inverted. |
| H | L | H | Reset: Enables a synchronous reset. |
| H | H | L | Left shift: Each clock pulse shifts $Q_n$ to $Q_{n+1}$, $D_0$ to $Q_0$. |
| H | H | H | Hold mode: No change for $Q_n$. |

The $\overline{C}/Q_3$ output of a 100136 can be connected to the $D_0/\overline{CET}$ input of another 100136, for multi-stage counting of left shift operation.

## Counter/Shift Register 100136

**ABSOLUTE MAXIMUM RATINGS** (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | 100K ECL | UNIT |
|---|---|---|---|
| $V_{EE}$ | Supply voltage ($V_{CC1}$ = $V_{CC3}$ = GND) | −7.0 to 0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | $V_{EE}$ to +0.5 | V |
| $I_O$ | Output source current | −55 | mA |
| $T_S$ | Storage temperature | −65 to +150 | °C |
| $T_J$ | Maximum junction temperature | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | | 100K ECL | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | −4.2 | −4.5 | −4.8 | V |
| $V_{EE}$ | Supply voltage (negative) when operating with 10K ECL family | | | | | −5.7 | V |
| $V_{IH}$ | HIGH level input voltage | $V_{CC1}$ = $V_{CC2}$ = GND<br>$T_A$ = 0°C to +85°C | $V_{EE}$ = −4.2V | −1150 | | −880 | mV |
| | | | $V_{EE}$ = −4.5V | −1165 | | | |
| | | | $V_{EE}$ = −4.8V | | | | |
| $V_{IHT}$ | HIGH level input threshold voltage | | $V_{EE}$ = −4.2V | −1150 | | | mV |
| | | | $V_{EE}$ = −4.5V | −1165 | | | mV |
| | | | $V_{EE}$ = −4.8V | | | | |
| $V_{ILT}$ | LOW level input threshold voltage | | $V_{EE}$ = −4.2V | | | −1475 | mV |
| | | | $V_{EE}$ = −4.5V | | | | |
| | | | $V_{EE}$ = −4.8V | | | −1490 | mV |
| $V_{IL}$ | LOW level input voltage | | $V_{EE}$ = −4.2V | −1810 | | −1475 | mV |
| | | | $V_{EE}$ = −4.5V | | | | |
| | | | $V_{EE}$ = −4.8V | | | −1490 | |
| $T_A$ | Operating ambient temperature | | | 0 | +25 | +85 | °C |

**NOTE:**
When operating at other than specified voltages (−4.2V, −4.5V, −4.8V) DC & AC Characteristics will vary slightly from specified values.

# Counter/Shift Register

# 100136

**DC ELECTRICAL CHARACTERISTICS** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$, $T_A = 0°C$ to $+85°C$ unless otherwise specified[1,3]

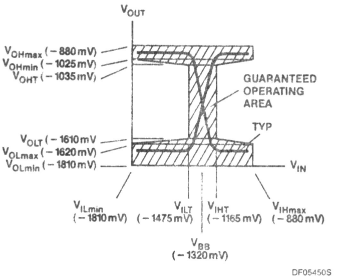
| PARAMETER | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] | |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | $V_{EE} = -4.2V$ | −1025 | | −870 | mV | $V_{IN} = V_{IHmax}$ or $V_{IN} = V_{ILmin}$ | Loading with 50Ω to −2.0V ±0.010V |
| | | $V_{EE} = -4.5V$ | −1025 | −955 | −880 | mV | | |
| | | $V_{EE} = -4.8V$ | −1035 | | −880 | mV | | |
| $V_{OHT}$ | HIGH level output threshold voltage | $V_{EE} = -4.2V$ | −1035 | | | mV | $V_{IN} = V_{IHmin}$ or $V_{IN} = V_{ILmax}$ | |
| | | $V_{EE} = -4.5V$ | −1035 | | | mV | | |
| | | $V_{EE} = -4.8V$ | −1045 | | | mV | | |
| $V_{OLT}$ | LOW level output threshold voltage | $V_{EE} = -4.2V$ | | | −1590 | mV | $V_{IN} = V_{IHmin}$ or $V_{IN} = V_{ILmax}$ | |
| | | $V_{EE} = -4.5V$ | | | −1610 | mV | | |
| | | $V_{EE} = -4.8V$ | | | −1610 | mV | | |
| $V_{OL}$ | LOW level output voltage | $V_{EE} = -4.2V$ | −1810 | | −1600 | mV | $V_{IN} = V_{IHmax}$ or $V_{IN} = V_{ILmin}$ | |
| | | $V_{EE} = -4.5V$ | −1810 | −1705 | −1620 | mV | | |
| | | $V_{EE} = -4.8V$ | −1830 | | −1620 | mV | | |
| $I_{IH}$ | HIGH level input current | $P_n$, $S_n$ | | | 180 | μA | $V_{IN} = V_{IHmax}$ | |
| | | $\overline{CEP}$ | | | 200 | μA | | |
| | | MR | | | 240 | μA | | |
| | | $D_3$ | | | 280 | μA | | |
| | | CP | | | 390 | μA | | |
| | | $D_0/\overline{CET}$ | | | 530 | μA | | |
| $I_{IL}$ | LOW level input current | | 0.5 | | | μA | $V_{IN} = V_{ILmin}$ | |
| $-I_{EE}$ | $V_{EE}$ supply current | | 136 | 210 | 283 | mA | Inputs open | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | $V_{EE} = -4.2V$<br>$T_A = +25°C$ | | | 0.035 | V/V | | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | | 0.070 | V/V | | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 4.

## Counter/Shift Register

## 100136



NOTES:

$V_{IHmax}$ – Maximum HIGH level input voltage (the most positive $V_{IH}$).
$V_{IHT}$ – HIGH level input threshold voltage.
$V_{ILT}$ – LOW level input threshold voltage.
$V_{ILmin}$ – Minimum LOW level input voltage (the most negative $V_{IL}$).
$V_{OHmax}$ – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition.
$V_{OHmin}$ – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition.
$V_{OHT}$ – HIGH level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLT}$ – LOW level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLmax}$ – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions.
$V_{OLmin}$ – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions.
$V_{BB}$ – Reference bias voltage. The internally generated reference voltage which is used to set the input and output threshold level.

Figure 4. Transfer Characteristics

## AC ELECTRICAL CHARACTERISTICS

**Ceramic DIP** $V_{CC1} = V_{CC2} = \text{GND}$, $V_{EE} = -4.2\text{V} \pm 0.010\text{V}$ to $-4.8\text{V} \pm 0.010\text{V}$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $f_{MAX}$ | Maximum shift frequency | 250 | | 250 | | 250 | | MHz | Figs. 5, 10, 11 |
| $t_{PLH}$ | Propagation delay | 0.85 | 2.10 | 0.85 | 2.10 | 0.85 | 2.25 | ns | Figs. 5, 9, 11 |
| $t_{PHL}$ | CP to $Q_n$, $\overline{Q}_n$ | 0.85 | 2.10 | 0.85 | 2.10 | 0.85 | 2.25 | ns | |
| $t_{PLH}$ | Propagation delay | 1.80 | 4.80 | 1.80 | 4.60 | 1.80 | 5.20 | ns | |
| $t_{PHL}$ | CP to $\overline{TC}$ | 1.80 | 4.80 | 1.80 | 4.60 | 1.80 | 5.20 | ns | |
| $t_{PLH}$ | Propagation delay | 1.20 | 2.95 | 1.35 | 2.95 | 1.20 | 3.10 | ns | Figs. 6, 9, 11 |
| $t_{PHL}$ | MR to $Q_n$, $\overline{Q}$ | 1.20 | 2.95 | 1.35 | 2.95 | 1.20 | 3.10 | ns | |
| $t_{PLH}$ | Propagation delay | 2.10 | 4.80 | 2.10 | 4.80 | 2.10 | 5.00 | ns | |
| $t_{PHL}$ | MR to $\overline{TC}$ | 2.10 | 4.80 | 2.10 | 4.80 | 2.10 | 5.00 | ns | |
| $t_{PLH}$ | Propagation delay | 1.40 | 3.20 | 1.40 | 3.20 | 1.40 | 3.50 | ns | Figs. 7, 9, 11 |
| $t_{PHL}$ | $D_0/\overline{CET}$ to $\overline{TC}$ | 1.40 | 3.20 | 1.40 | 3.20 | 1.40 | 3.50 | ns | |
| $t_{PLH}$ | Propagation delay | 1.40 | 4.60 | 1.60 | 4.60 | 1.60 | 4.80 | ns | |
| $t_{PHL}$ | $S_n$ to $\overline{TC}$ | 1.40 | 4.60 | 1.60 | 4.60 | 1.60 | 4.80 | ns | |
| $t_{TLH}$ | Transition time | 0.45 | 1.80 | 0.45 | 1.80 | 0.45 | 1.80 | ns | Figs. 5, 6, 7, 9, 11 |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.80 | 0.45 | 1.80 | 0.45 | 1.80 | ns | |
| $t_s$ | Setup time $D_0$, $D_3$ to CP | 2.30 | | 2.30 | | 2.30 | | ns | Figs. 8, 11 |
| $t_h$ | Hold time $D_0$, $D_3$ to CP | 0.20 | | 0.20 | | 0.20 | | ns | |
| $t_s$ | Setup time $P_n$ to CP | 1.70 | | 1.70 | | 1.70 | | ns | |
| $t_h$ | Hold time $P_n$ to CP | 0.10 | | 0.10 | | 0.10 | | ns | |
| $t_s$ | Setup time $D_0/\overline{CEP}$, $\overline{CET}$ to CP | 2.30 | | 2.30 | | 2.30 | | ns | |
| $t_h$ | Hold time $D_0/\overline{CEP}$, $\overline{CET}$ to CP | 0.20 | | 0.20 | | 0.20 | | ns | |
| $t_s$ | Setup time $S_n$ to CP | 3.80 | | 3.80 | | 3.80 | | ns | |
| $t_h$ | Hold time $S_n$ to CP | −0.9 | | −0.9 | | −0.9 | | ns | |
| $t_r$ | Release time/ MR to $CP_n$ | 2.50 | | 2.50 | | 2.50 | | ns | Figs. 6, 11 |
| $t_w(H)$ | Pulse width HIGH MR, CP | 2.50 | | 2.50 | | 2.50 | | ns | Figs. 5, 6, 11 |

## AC ELECTRICAL CHARACTERISTICS

**Ceramic DIP** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V \pm 5\%$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $f_{MAX}$ | Maximum shift frequency | 250 | | 250 | | 250 | | MHz | Figs. 5, 10, 11 |
| $t_{PLH}$ | Propagation delay | 0.85 | 2.10 | 0.85 | 2.10 | 0.85 | 2.25 | ns | Figs. 5, 9, 11 |
| $t_{PHL}$ | CP to $Q_n$, $\overline{Q}_n$ | 0.85 | 2.10 | 0.85 | 2.10 | 0.85 | 2.25 | ns | |
| $t_{PLH}$ | Propagation delay | 1.80 | 4.80 | 1.80 | 4.60 | 1.80 | 5.20 | ns | |
| $t_{PHL}$ | CP to $\overline{TC}$ | 1.80 | 4.80 | 1.80 | 4.60 | 1.80 | 5.20 | ns | |
| $t_{PLH}$ | Propagation delay | 1.20 | 2.95 | 1.35 | 2.95 | 1.20 | 3.10 | ns | Figs. 6, 9, 11 |
| $t_{PHL}$ | MR to $Q_n$, $\overline{Q}$ | 1.20 | 2.95 | 1.35 | 2.95 | 1.20 | 3.10 | ns | |
| $t_{PLH}$ | Propagation delay | 2.10 | 4.80 | 2.10 | 4.80 | 2.10 | 5.00 | ns | |
| $t_{PHL}$ | MR to $\overline{TC}$ | 2.10 | 4.80 | 2.10 | 4.80 | 2.10 | 5.00 | ns | |
| $t_{PLH}$ | Propagation delay | 1.40 | 3.20 | 1.40 | 3.20 | 1.40 | 3.50 | ns | Figs. 7, 9, 11 |
| $t_{PHL}$ | $D_0/\overline{CET}$ to $\overline{TC}$ | 1.40 | 3.20 | 1.40 | 3.20 | 1.40 | 3.50 | ns | |
| $t_{PLH}$ | Propagation delay | 1.40 | 4.60 | 1.60 | 4.60 | 1.60 | 4.80 | ns | |
| $t_{PHL}$ | $S_n$ to $\overline{TC}$ | 1.40 | 4.60 | 1.60 | 4.60 | 1.60 | 4.80 | ns | |
| $t_{TLH}$ | Transition time | 0.45 | 1.80 | 0.45 | 1.80 | 0.45 | 1.80 | ns | Figs. 5, 6, 7, 9, 11 |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.80 | 0.45 | 1.80 | 0.45 | 1.80 | ns | |
| $t_s$ | Setup time $D_0$, $D_3$ to CP | 2.30 | | 2.30 | | 2.30 | | ns | Figs. 8, 11 |
| $t_h$ | Hold time $D_0$, $D_3$ to CP | 0.20 | | 0.20 | | 0.20 | | ns | |
| $t_s$ | Setup time $P_n$ to CP | 1.70 | | 1.70 | | 1.70 | | ns | |
| $t_h$ | Hold time $P_n$ to CP | 0.10 | | 0.10 | | 0.10 | | ns | |
| $t_s$ | Setup time $D_0/\overline{CEP}$, $\overline{CET}$ to CP | 2.30 | | 2.30 | | 2.30 | | ns | |
| $t_h$ | Hold time $D_0/\overline{CEP}$, $\overline{CET}$ to CP | 0.20 | | 0.20 | | 0.20 | | ns | |
| $t_s$ | Setup time $S_n$ to CP | 3.80 | | 3.80 | | 3.80 | | ns | |
| $t_h$ | Hold time $S_n$ to CP | −0.9 | | −0.9 | | −0.9 | | ns | |
| $t_r$ | Release time/ MR to $CP_n$ | 2.50 | | 2.50 | | 2.50 | | ns | Figs. 6, 11 |
| $t_w(H)$ | Pulse width HIGH MR, CP | 2.50 | | 2.50 | | 2.50 | | ns | Figs. 5, 6, 11 |

## AC ELECTRICAL CHARACTERISTICS

**Flat Pack** $V_{CC1} = V_{CC2} =$ GND, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$

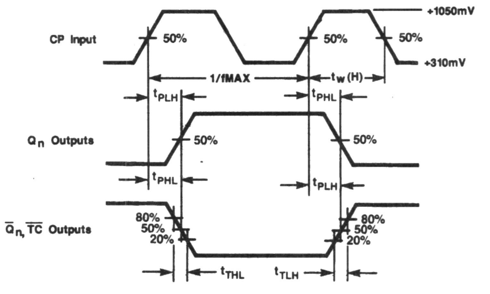
| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $f_{MAX}$ | Maximum shift frequency | 250 | | 250 | | 250 | | MHz | Figs. 5, 10, 11 |
| $t_{PLH}$ | Propagation delay | 0.85 | 2.15 | 0.85 | 2.15 | 0.85 | 2.30 | ns | Figs. 5, 9, 11 |
| $t_{PHL}$ | CP to $Q_n$, $\overline{Q}_n$ | 0.85 | 2.15 | 0.85 | 2.15 | 0.85 | 2.30 | ns | |
| $t_{PLH}$ | Propagation delay | 1.80 | 4.60 | 1.80 | 4.40 | 1.80 | 5.00 | ns | |
| $t_{PHL}$ | CP to $\overline{TC}$ | 1.80 | 4.60 | 1.80 | 4.40 | 1.80 | 5.00 | ns | |
| $t_{PLH}$ | Propagation delay | 1.20 | 2.75 | 1.35 | 2.75 | 1.20 | 2.90 | ns | Figs. 6, 9, 11 |
| $t_{PHL}$ | MR to $Q_n$, $\overline{Q}$ | 1.20 | 2.75 | 1.35 | 2.75 | 1.20 | 2.90 | ns | |
| $t_{PLH}$ | Propagation delay | 2.10 | 4.60 | 2.10 | 4.60 | 2.10 | 4.80 | ns | |
| $t_{PHL}$ | MR to $\overline{TC}$ | 2.10 | 4.60 | 2.10 | 4.60 | 2.10 | 4.80 | ns | |
| $t_{PLH}$ | Propagation delay | 1.40 | 3.00 | 1.40 | 3.00 | 1.40 | 3.30 | ns | Figs. 7, 9, 11 |
| $t_{PHL}$ | $D_0/\overline{CET}$ to $\overline{TC}$ | 1.40 | 3.00 | 1.40 | 3.00 | 1.40 | 3.30 | ns | |
| $t_{PLH}$ | Propagation delay | 1.40 | 4.60 | 1.60 | 4.60 | 1.60 | 4.80 | ns | |
| $t_{PHL}$ | $S_n$ to $\overline{TC}$ | 1.40 | 4.60 | 1.60 | 4.60 | 1.60 | 4.80 | ns | |
| $t_{TLH}$ | Transition time | 0.45 | 1.80 | 0.45 | 1.80 | 0.45 | 1.80 | ns | Figs. 5, 6, 7, 9, 11 |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.80 | 0.45 | 1.80 | 0.45 | 1.80 | ns | |
| $t_s$ | Setup time $D_0$, $D_3$ to CP | 1.40 | | 1.40 | | 1.40 | | ns | Figs. 8, 11 |
| $t_h$ | Hold time $D_0$, $D_3$ to CP | 0.00 | | 0.00 | | 0.00 | | ns | |
| $t_s$ | Setup time $P_n$ to CP | 1.60 | | 1.60 | | 1.60 | | ns | |
| $t_h$ | Hold time $P_n$ to CP | 0.00 | | 0.00 | | 0.00 | | ns | |
| $t_s$ | Setup time $D_0/\overline{CEP}$, $\overline{CET}$ to CP | 1.80 | | 1.80 | | 1.80 | | ns | |
| $t_h$ | Hold time $D_0/\overline{CEP}$, $\overline{CET}$ to CP | 0.00 | | 0.00 | | 0.00 | | ns | |
| $t_s$ | Setup time $S_n$ to CP | 3.60 | | 3.60 | | 3.60 | | ns | |
| $t_h$ | Hold time $S_n$ to CP | −0.4 | | −0.4 | | −0.4 | | ns | |
| $t_r$ | Release time MR to $CP_n$ | 2.50 | | 2.50 | | 2.50 | | ns | Figs. 6, 11 |
| $t_w(H)$ | Pulse width HIGH MR, CP | 2.50 | | 2.50 | | 2.50 | | ns | Figs. 5, 6, 11 |

## AC ELECTRICAL CHARACTERISTICS

**Flat Pack** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V \pm 5\%$

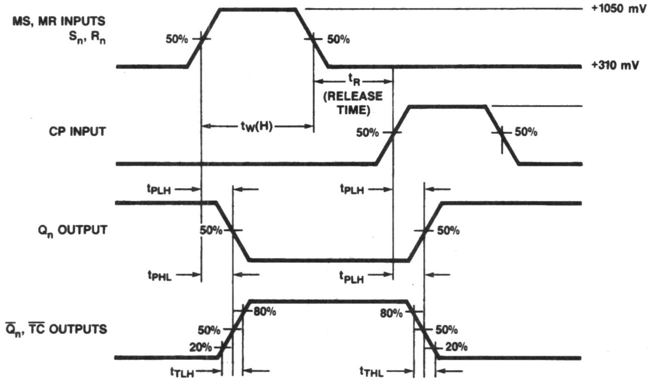
| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $f_{MAX}$ | Maximum shift frequency | 250 | | 250 | | 250 | | MHz | Figs. 5, 10, 11 |
| $t_{PLH}$ | Propagation delay CP to $Q_n$, $\overline{Q}_n$ | 0.85 | 2.15 | 0.85 | 2.15 | 0.85 | 2.30 | ns | Figs. 5, 9, 11 |
| $t_{PHL}$ | | 0.85 | 2.15 | 0.85 | 2.15 | 0.85 | 2.30 | ns | |
| $t_{PLH}$ | Propagation delay CP to $\overline{TC}$ | 1.80 | 4.60 | 1.80 | 4.40 | 1.80 | 5.00 | ns | |
| $t_{PHL}$ | | 1.80 | 4.60 | 1.80 | 4.40 | 1.80 | 5.00 | ns | |
| $t_{PLH}$ | Propagation delay MR to $Q_n$, $\overline{Q}$ | 1.20 | 2.75 | 1.35 | 2.75 | 1.20 | 2.90 | ns | Figs. 6, 9, 11 |
| $t_{PHL}$ | | 1.20 | 2.75 | 1.35 | 2.75 | 1.20 | 2.90 | ns | |
| $t_{PLH}$ | Propagation delay MR to $\overline{TC}$ | 2.10 | 4.60 | 2.10 | 4.60 | 2.10 | 4.80 | ns | |
| $t_{PHL}$ | | 2.10 | 4.60 | 2.10 | 4.60 | 2.10 | 4.80 | ns | |
| $t_{PLH}$ | Propagation delay $D_0/\overline{CET}$ to $\overline{TC}$ | 1.40 | 3.00 | 1.40 | 3.00 | 1.40 | 3.30 | ns | Figs. 7, 9, 11 |
| $t_{PHL}$ | | 1.40 | 3.00 | 1.40 | 3.00 | 1.40 | 3.30 | ns | |
| $t_{PLH}$ | Propagation delay $S_n$ to $\overline{TC}$ | 1.40 | 4.60 | 1.60 | 4.60 | 1.60 | 4.80 | ns | |
| $t_{PHL}$ | | 1.40 | 4.60 | 1.60 | 4.60 | 1.60 | 4.80 | ns | |
| $t_{TLH}$ | Transition time 20% to 80%, 80% to 20% | 0.45 | 1.80 | 0.45 | 1.80 | 0.45 | 1.80 | ns | Figs. 5, 6, 7, 9, 11 |
| $t_{THL}$ | | 0.45 | 1.80 | 0.45 | 1.80 | 0.45 | 1.80 | ns | |
| $t_s$ | Setup time $D_0$, $D_3$ to CP | 1.40 | | 1.40 | | 1.40 | | ns | Figs. 8, 11 |
| $t_h$ | Hold time $D_0$, $D_3$ to CP | 0.00 | | 0.00 | | 0.00 | | ns | |
| $t_s$ | Setup time $P_n$ to CP | 1.60 | | 1.60 | | 1.60 | | ns | |
| $t_h$ | Hold time $P_n$ to CP | 0.00 | | 0.00 | | 0.00 | | ns | |
| $t_s$ | Setup time $D_0/\overline{CEP}$, $\overline{CET}$ to CP | 1.80 | | 1.80 | | 1.80 | | ns | |
| $t_h$ | Hold time $D_0/\overline{CEP}$, $\overline{CET}$ to CP | 0.00 | | 0.00 | | 0.00 | | ns | |
| $t_s$ | Setup time $S_n$ to CP | 3.60 | | 3.60 | | 3.60 | | ns | |
| $t_h$ | Hold time $S_n$ to CP | −0.4 | | −0.4 | | −0.4 | | ns | |
| $t_r$ | Release time MR to $CP_n$ | 2.50 | | 2.50 | | 2.50 | | ns | Figs. 6, 11 |
| $t_w(H)$ | Pulse width HIGH MR, CP | 2.50 | | 2.50 | | 2.50 | | ns | Figs. 5, 6, 11 |

## AC WAVEFORMS


+1050mV
CP Input
50%
50%
50%
+310mV
1/fMAX
$t_{W}$ (H)
$t_{PLH}$
$t_{PHL}$
$Q_n$ Outputs
50%
50%
$t_{PHL}$
$t_{PLH}$
$\overline{Q}_n$, $\overline{TC}$ Outputs
80%
50%
20%
80%
50%
20%
$t_{THL}$
$t_{TLH}$

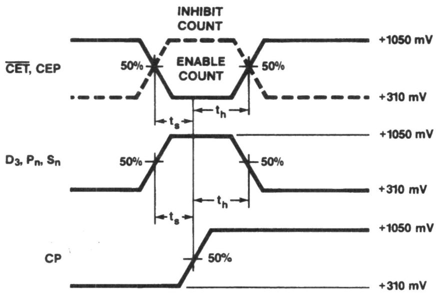
WF13200S

Figure 5. Propagation Delay for Clock to Outputs and Transition Times


MS, MR INPUTS
$S_n$, $R_n$
50%
50%
+1050 mV
+310 mV
$t_R$
(RELEASE TIME)
CP INPUT
tw(H)
50%
50%
$t_{PLH}$
$t_{PLH}$
$Q_n$ OUTPUT
50%
50%
$t_{PHL}$
$t_{PLH}$
$\overline{Q}_n$, $\overline{TC}$ OUTPUTS
80%
50%
20%
80%
50%
20%
$t_{TLH}$
$t_{THL}$

WF12840S

Figure 6. Propagation Delay for Sets and Resets to Outputs


INHIBIT COUNT
ENABLE COUNT
$\overline{CET}$, CEP
50%
50%
+1050 mV
+310 mV
$t_s$
$t_h$
$D_3$, $P_n$, $S_n$
50%
50%
+1050 mV
+310 mV
$t_s$
$t_h$
CP
50%
+1050 mV
+310 mV

WF12470S

Figure 7. Propagation Delay for Serial Data and Select Inputs Terminal Count Output

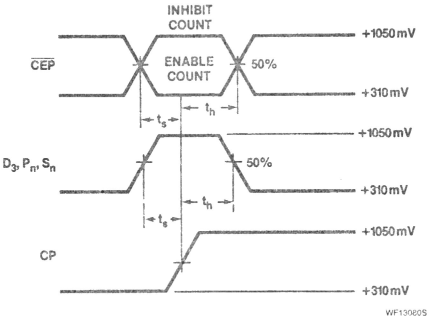
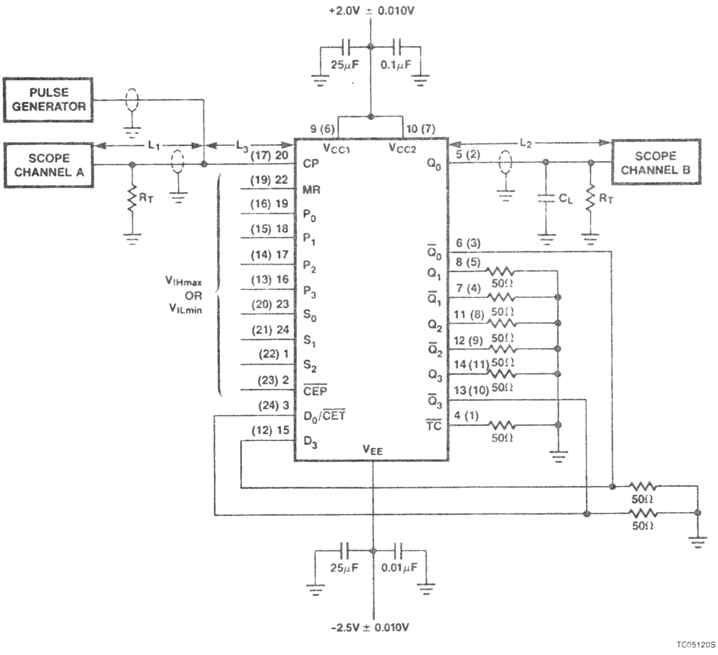

INHIBIT COUNT
ENABLE COUNT
$\overline{CEP}$
50%
+1050mV
+310mV
$t_s$
$t_h$
$D_3, P_n, S_n$
50%
+1050mV
+310mV
$t_s$
$t_h$
CP
+1050mV
+310mV
WF13080S

Figure 8. Data Setup and Hold Times

## TEST CIRCUITS AND WAVEFORMS


+2.0V ± 0.010V
25μF
0.1μF
PULSE GENERATOR
SCOPE CHANNEL A
$R_T$
$L_1$
$L_3$
9 (6)
10 (7)
$V_{CC1}$
$V_{CC2}$
$L_2$
SCOPE CHANNEL B
(17) 20
CP
(19) 22
MR
(16) 19
$P_0$
(15) 18
$P_1$
(14) 17
$P_2$
(13) 16
$P_3$
(20) 23
$S_0$
(21) 24
$S_1$
(22) 1
$S_2$
(23) 2
$\overline{CEP}$
(24) 3
$D_0/\overline{CET}$
(12) 15
$D_3$
$V_{EE}$
$V_{IHmax}$ OR $V_{ILmin}$
$Q_0$
5 (2)
$C_L$
$R_T$
$\overline{Q}_0$
6 (3)
$Q_1$
8 (5)
$\overline{Q}_1$
7 (4)
$Q_2$
11 (8)
$\overline{Q}_2$
12 (9)
$Q_3$
14 (11)
$\overline{Q}_3$
13 (10)
$\overline{TC}$
4 (1)
50Ω
50Ω
50Ω
25μF
0.01μF
-2.5V ± 0.010V
TC05120S

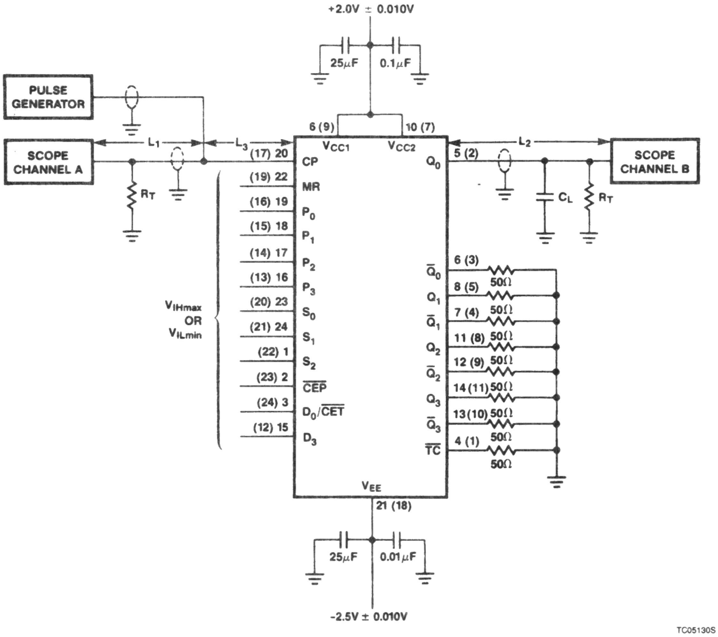
NOTES:

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1μF and 25μF from GND to $V_{CC}$, 0.01μF and 25μF from GND to $V_{EE}$ (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance ≤ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.
11. Pin connections are for Flat Pack and in parentheses for Ceramic DIP package.

Figure 9. AC Test Circuit

## Counter/Shift Register

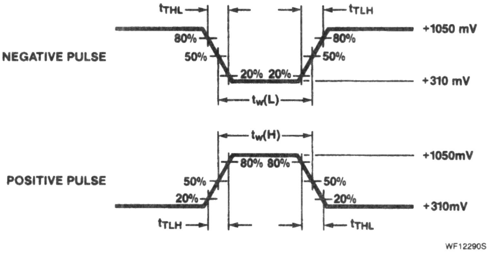
## 100136


+2.0V ± 0.010V
25µF
0.1µF
PULSE GENERATOR
SCOPE CHANNEL A
L1
L3
RT
6 (9)
10 (7)
VCC1
VCC2
(17) 20 CP
(19) 22 MR
(16) 19 P0
(15) 18 P1
(14) 17 P2
(13) 16 P3
(20) 23 S0
(21) 24 S1
(22) 1 S2
(23) 2 CEP
(24) 3 D0/CET
(12) 15 D3
VIHmax OR VILmin
Q0 5 (2)
L2
SCOPE CHANNEL B
CL
RT
Q̄0 6 (3)
Q1 8 (5)
Q̄1 7 (4)
Q2 11 (8)
Q̄2 12 (9)
Q3 14 (11)
Q̄3 13 (10)
TC 4 (1)
50Ω
VEE
21 (18)
25µF
0.01µF
-2.5V ± 0.010V
TC05130S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1µF and 25µF from GND to $V_{CC}$, 0.01µF and 25µF from GND to $V_{EE}$. (0.01 and 0.1µF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance $\leqslant$ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.
11. Pin connections are for Flat Pack and in parentheses for Ceramic DIP package.

**Figure 10. Shift Frequency Test Circuit (Shift Left)**


NEGATIVE PULSE
tTHL
tTLH
80%
50%
20%
20%
80%
50%
+1050 mV
+310 mV
tw(L)
tw(H)
POSITIVE PULSE
80%
80%
50%
20%
50%
20%
+1050mV
+310mV
tTLH
tTHL
WF12290S

| INPUT PULSE REQUIREMENTS<br>$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -2.5V \pm 0.010V$, $V_T$ = GND (0V) | | | | | |
|---|---|---|---|---|---|
| **Family** | **Amplitude** | **Rep Rate** | **Pulse Width** | $t_{TLH}$ | $t_{THL}$ |
| 100K ECL | 740mVp-p | 1MHz | 500ns | 0.7 ± 0.1ns | 0.7 ± 0.1ns |

**Figure 11. Input Pulse Definition**

**Signetics**

# 100141
## Shift Register

**8-Bit Shift Register**
***Product Specification***

**ECL Products**

### DESCRIPTION

100141 has eight D-type flip-flops, and two selection inputs, $S_0$, $S_1$, allowing a parallel loading or left shifting or right shifting, or hold operation mode.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 100141 | 1.7ns | 175mA |

### ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} = GND$; $V_{EE} = -4.2V$ to $-4.8V$<br>$T_A = 0°C$ to $+85°C$ |
|---|---|
| Ceramic DIP | 100141F |
| Ceramic Flat Pack | 100141Y |

### PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_0 - D_7$ | Serial Data Inputs |
| $P_0 - P_3$ | Parallel Data Inputs |
| CP | Clock Input |
| $S_0$, $S_1$ | Select Inputs |
| $Q_0 - Q_7$ | Data Outputs |

### PIN CONFIGURATION

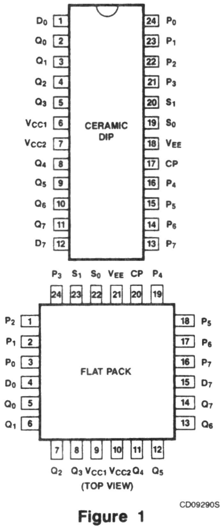

D0 1
Q0 2
Q1 3
Q2 4
Q3 5
VCC1 6
VCC2 7
Q4 8
Q5 9
Q6 10
Q7 11
D7 12
24 P0
23 P1
22 P2
21 P3
20 S1
19 S0
18 VEE
17 CP
16 P4
15 P5
14 P6
13 P7
CERAMIC DIP
P3 S1 S0 VEE CP P4
24 23 22 21 20 19
P2 1
P1 2
P0 3
D0 4
Q0 5
Q1 6
18 P5
17 P6
16 P7
15 D7
14 Q7
13 Q6
FLAT PACK
7 8 9 10 11 12
Q2 Q3 VCC1 VCC2 Q4 Q5
(TOP VIEW)
CD09290S

**Figure 1**

### LOGIC SYMBOL

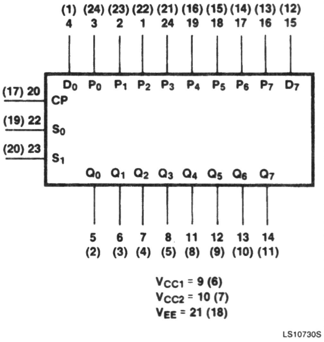

(1) (24) (23) (22) (21) (16) (15) (14) (13) (12)
4 3 2 1 24 19 18 17 16 15
D0 P0 P1 P2 P3 P4 P5 P6 P7 D7
(17) 20 CP
(19) 22 S0
(20) 23 S1
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
5 6 7 8 11 12 13 14
(2) (3) (4) (5) (8) (9) (10) (11)
VCC1 = 9 (6)
VCC2 = 10 (7)
VEE = 21 (18)
LS10730S

**Figure 2**

# Shift Register

# 100141

## LOGIC DIAGRAM

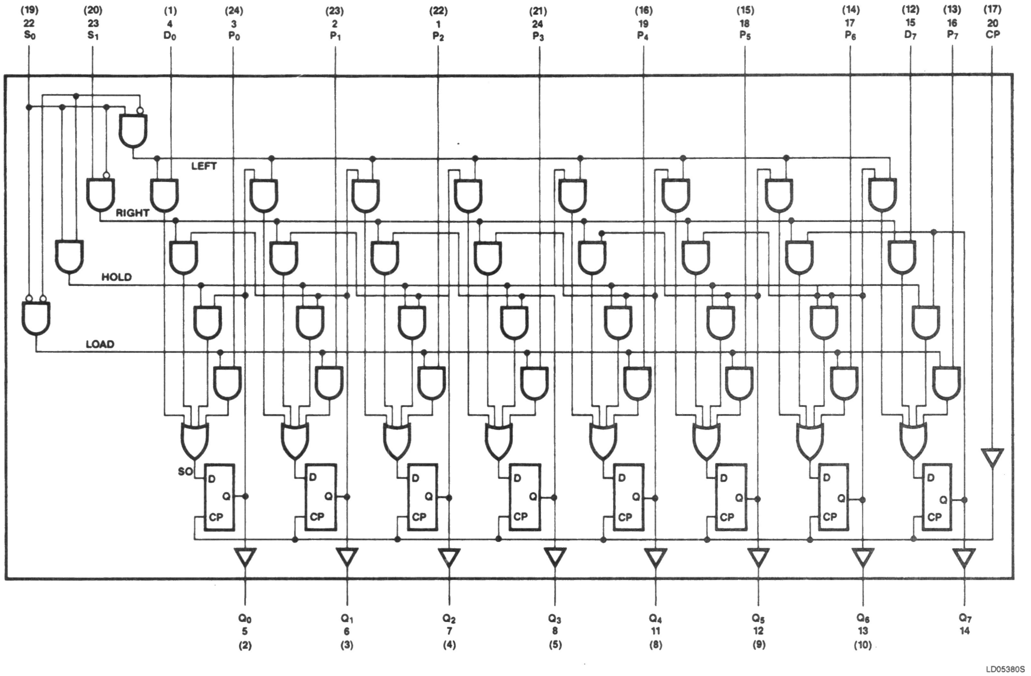

(19)
22
$S_0$
(20)
23
$S_1$
(1)
4
$D_0$
(24)
3
$P_0$
(23)
2
$P_1$
(22)
1
$P_2$
(21)
24
$P_3$
(16)
19
$P_4$
(15)
18
$P_5$
(14)
17
$P_6$
(12)
15
$D_7$
(13)
16
$P_7$
(17)
20
CP
LEFT
RIGHT
HOLD
LOAD
SO
D
Q
CP
$Q_0$
5
(2)
$Q_1$
6
(3)
$Q_2$
7
(4)
$Q_3$
8
(5)
$Q_4$
11
(8)
$Q_5$
12
(9)
$Q_6$
13
(10)
$Q_7$
14
LD05380S

Figure 3

## FUNCTION TABLE

| MODE | INPUTS | | | OUTPUTS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | $S_0$ | $S_1$ | CP | 7 $Q_{n+1}$ | 6 $Q_{n+1}$ | 5 $Q_{n+1}$ | 4 $Q_{n+1}$ | 3 $Q_{n+1}$ | 2 $Q_{n+1}$ | 1 $Q_{n+1}$ | 0 $Q_{n+1}$ |
| Register load | L | L | ↑ | $\overset{7}{P_n}$ | $\overset{6}{P_n}$ | $\overset{5}{P_n}$ | $\overset{4}{P_n}$ | $\overset{3}{P_n}$ | $\overset{2}{P_n}$ | $\overset{1}{P_n}$ | $\overset{0}{P_n}$ |
| Right shift | L | H | ↑ | $\overset{7}{D_n}$ | $\overset{7}{Q_n}$ | $\overset{6}{Q_n}$ | $\overset{5}{Q_n}$ | $\overset{4}{Q_n}$ | $\overset{3}{Q_n}$ | $\overset{2}{Q_n}$ | $\overset{1}{Q_n}$ |
| Left shift | H | L | ↑ | $\overset{6}{Q_n}$ | $\overset{5}{Q_n}$ | $\overset{4}{Q_n}$ | $\overset{3}{Q_n}$ | $\overset{2}{Q_n}$ | $\overset{1}{Q_n}$ | $\overset{0}{Q_n}$ | $\overset{0}{D_n}$ |
| Hold state | H | H | X | $\overset{7}{Q_n}$ | $\overset{6}{Q_n}$ | $\overset{5}{Q_n}$ | $\overset{4}{Q_n}$ | $\overset{3}{Q_n}$ | $\overset{2}{Q_n}$ | $\overset{1}{Q_n}$ | $\overset{0}{Q_n}$ |

Positive Logic:
H = HIGH state (more positive voltage) = 1
L = LOW state (less positive voltage) = 0
↑ = LOW-to-HIGH transition
X = Don't Care
n = last state
n + 1 = next state after transition

## Shift Register 100141

**ABSOLUTE MAXIMUM RATINGS** (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | 100K ECL | UNIT |
|---|---|---|---|
| $V_{EE}$ | Supply voltage ($V_{CC1}$ = $V_{CC2}$ = GND) | -7.0 to 0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | $V_{EE}$ to +0.5 | V |
| $I_O$ | Output source current | -55 | mA |
| $T_S$ | Storage temperature | -65 to +150 | °C |
| $T_J$ | Maximum junction temperature | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | | 100K ECL | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | -4.2 | -4.5 | -4.8 | V |
| $V_{EE}$ | Supply voltage (negative) when operating with 10K ECL family | | | | | -5.7 | V |
| $V_{IH}$ | HIGH level input voltage | $V_{CC1}$ = $V_{CC2}$ = GND<br>$T_A$ = 0°C to +85°C | $V_{EE}$ = -4.2V | -1150 | | -880 | mV |
| | | | $V_{EE}$ = -4.5V | -1165 | | | |
| | | | $V_{EE}$ = -4.8V | | | | |
| $V_{IHT}$ | HIGH level input threshold voltage | | $V_{EE}$ = -4.2V | -1150 | | | mV |
| | | | $V_{EE}$ = -4.5V | -1165 | | | mV |
| | | | $V_{EE}$ = -4.8V | | | | |
| $V_{ILT}$ | LOW level input threshold voltage | | $V_{EE}$ = -4.2V | | | -1475 | mV |
| | | | $V_{EE}$ = -4.5V | | | | |
| | | | $V_{EE}$ = -4.8V | | | -1490 | mV |
| $V_{IL}$ | LOW level input voltage | | $V_{EE}$ = -4.2V | -1810 | | -1475 | mV |
| | | | $V_{EE}$ = -4.5V | | | | |
| | | | $V_{EE}$ = -4.8V | | | -1490 | |
| $T_A$ | Operating ambient temperature | | | 0 | +25 | +85 | °C |

**NOTE:**
When operating at other than specified voltages (-4.2V, -4.5V, -4.8V) DC & AC Characteristics will vary slightly from specified values.

# Shift Register

# 100141

**DC ELECTRICAL CHARACTERISTICS** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$, $T_A = 0°C$ to $+85°C$ unless otherwise specified[1, 3]

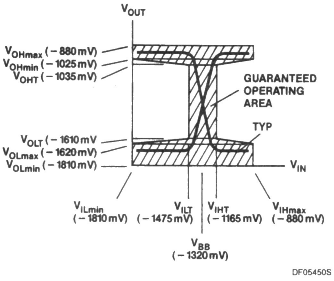
| PARAMETER | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] | |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | $V_{EE} = -4.2V$ | -1025 | | -870 | mV | $V_{IN} = V_{IHmax}$ or $V_{IN} = V_{ILmin}$ | Loading with 50Ω to -2.0V ±0.010V |
| | | $V_{EE} = -4.5V$ | -1025 | -955 | -880 | mV | | |
| | | $V_{EE} = -4.8V$ | -1035 | | -880 | mV | | |
| $V_{OHT}$ | HIGH level output threshold voltage | $V_{EE} = -4.2V$ | -1035 | | | mV | $V_{IN} = V_{IHmin}$ or $V_{IN} = V_{ILmax}$ | |
| | | $V_{EE} = -4.5V$ | -1035 | | | mV | | |
| | | $V_{EE} = -4.8V$ | -1045 | | | mV | | |
| $V_{OLT}$ | LOW level output threshold voltage | $V_{EE} = -4.2V$ | | | -1590 | mV | $V_{IN} = V_{IHmin}$ or $V_{IN} = V_{ILmax}$ | |
| | | $V_{EE} = -4.5V$ | | | -1610 | mV | | |
| | | $V_{EE} = -4.8V$ | | | -1610 | mV | | |
| $V_{OL}$ | LOW level output voltage | $V_{EE} = -4.2V$ | -1810 | | -1600 | mV | $V_{IN} = V_{IHmax}$ or $V_{IN} = V_{ILmin}$ | |
| | | $V_{EE} = -4.5V$ | -1810 | -1705 | -1620 | mV | | |
| | | $V_{EE} = -4.8V$ | -1830 | | -1620 | mV | | |
| $I_{IH}$ | HIGH level input current | CP | | | 640 | μA | $V_{IN} = V_{IHmax}$ | |
| | | $D_n$, $P_n$, $S_n$ | | | 220 | μA | | |
| $I_{IL}$ | LOW level input current | | 0.5 | | | μA | $V_{IN} = V_{ILmin}$ | |
| $-I_{EE}$ | $V_{EE}$ supply current | | 120 | 175 | 238 | mA | Inputs open | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | $V_{EE} = -4.2V$<br>$T_A = +25°C$ | | | 0.025 | V/V | | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | | 0.050 | V/V | | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 4.

# Shift Register

# 100141


V_OUT
V_OHmax (−880mV)
V_OHmin (−1025mV)
V_OHT (−1035mV)
GUARANTEED OPERATING AREA
TYP
V_OLT (−1610mV
V_OLmax (−1620mV)
V_OLmin (−1810mV)
V_IN
V_ILmin (−1810mV)
V_ILT (−1475mV)
V_IHT (−1165mV)
V_IHmax (−880mV)
V_BB (−1320mV)
DF05450S

**NOTES:**

| | |
|---|---|
| $V_{IHmax}$ | – Maximum HIGH level input voltage (the most positive $V_{IH}$). |
| $V_{IHT}$ | – HIGH level input threshold voltage. |
| $V_{ILT}$ | – LOW level input threshold voltage. |
| $V_{ILmin}$ | – Minimum LOW level input voltage (the most negative $V_{IL}$). |
| $V_{OHmax}$ | – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition. |
| $V_{OHmin}$ | – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition. |
| $V_{OHT}$ | – HIGH level output threshold voltage with the inputs set to their respective threshold levels. |
| $V_{OLT}$ | – LOW level output threshold voltage with the inputs set to their respective threshold levels. |
| $V_{OLmax}$ | – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions. |
| $V_{OLmin}$ | – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions. |
| $V_{BB}$ | – Reference bias voltage. The internally generated reference voltage which is used to set the input and output threshold level. |

**Figure 4. Transfer Characteristics**

## AC ELECTRICAL CHARACTERISTICS

**Ceramic DIP** $V_{CC1} = V_{CC2} = \text{GND}$, $V_{EE} = -4.2\text{V} \pm 0.010\text{V}$ to $-4.8\text{V} \pm 0.010\text{V}$

| | PARAMETER | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $f_{MAX}$ | Maximum shift frequency | 275 | | 275 | | 275 | | MHz | Figs. 5, 8, 9 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>CP to $Q_n$ | 0.90<br>0.90 | 2.40<br>2.40 | 1.10<br>1.10 | 2.40<br>2.40 | 1.10<br>1.10 | 2.55<br>2.55 | ns<br>ns | Figs. 5, 7, 9 |
| $t_{TLH}$<br>$t_{THL}$ | Transition time<br>20% to 80%, 80% to 20% | 0.45<br>0.45 | 1.40<br>1.40 | 0.45<br>0.45 | 1.30<br>1.30 | 0.45<br>0.45 | 1.40<br>1.40 | ns<br>ns | |
| $t_s$ | Setup time<br>$D_n$, $P_n$ to CP | 1.40 | | 1.40 | | 1.70 | | ns | Figs. 6, 9 |
| $t_h$ | Hold time<br>$D_n$, $P_n$ to CP | 0.60 | | 0.60 | | 0.60 | | ns | |
| $t_s$ | Setup time<br>$S_n$ to CP | 3.80 | | 3.80 | | 3.40 | | ns | Figs. 6, 9 |
| $t_h$ | Hold time<br>$S_n$ to CP | 0.10 | | 0.10 | | 0.10 | | ns | |
| $t_w$(H) | Pulse width HIGH<br>CP | 2.50 | | 2.50 | | 2.50 | | ns | Figs. 5, 9 |

## AC ELECTRICAL CHARACTERISTICS

**Ceramic DIP** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V \pm 5\%$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $f_{MAX}$ | Maximum shift frequency | 275 | | 275 | | 275 | | MHz | Figs. 5, 8, 9 |
| $t_{PLH}$ | Propagation delay | 0.90 | 2.40 | 1.10 | 2.40 | 1.10 | 2.55 | ns | Figs. 5, 7, 9 |
| $t_{PHL}$ | CP to $Q_n$ | 0.90 | 2.40 | 1.10 | 2.40 | 1.10 | 2.55 | ns | |
| $t_{TLH}$ | Transition time | 0.45 | 1.40 | 0.45 | 1.30 | 0.45 | 1.40 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.40 | 0.45 | 1.30 | 0.45 | 1.40 | ns | |
| $t_s$ | Setup time<br>$D_n$, $P_n$ to CP | 1.40 | | 1.40 | | 1.70 | | ns | Figs. 6, 9 |
| $t_h$ | Hold time<br>$D_n$, $P_n$ to CP | 0.60 | | 0.60 | | 0.60 | | ns | |
| $t_s$ | Setup time<br>$S_n$ to CP | 3.80 | | 3.80 | | 3.40 | | ns | Figs. 6, 9 |
| $t_h$ | Hold time<br>$S_n$ to CP | 0.10 | | 0.10 | | 0.10 | | ns | |
| $t_w(H)$ | Pulse width HIGH<br>CP | 2.50 | | 2.50 | | 2.50 | | ns | Figs. 5, 9 |

**Flat Pack** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $f_{MAX}$ | Maximum shift frequency | 300 | | 300 | | 300 | | MHz | Figs. 5, 8, 9 |
| $t_{PLH}$ | Propagation delay | 0.90 | 2.20 | 1.10 | 2.20 | 1.10 | 2.35 | ns | Figs. 5, 7, 9 |
| $t_{PHL}$ | CP to $Q_n$ | 0.90 | 2.20 | 1.10 | 2.20 | 1.10 | 2.35 | ns | |
| $t_{TLH}$ | Transition time | 0.45 | 1.40 | 0.45 | 1.30 | 0.45 | 1.40 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.40 | 0.45 | 1.30 | 0.45 | 1.40 | ns | |
| $t_s$ | Setup time<br>$D_n$, $P_n$ to CP | 1.20 | | 1.20 | | 1.50 | | ns | Figs. 6, 9 |
| $t_h$ | Hold time<br>$D_n$, $P_n$ to CP | 0.50 | | 0.50 | | 0.50 | | ns | |
| $t_s$ | Setup time<br>$S_n$ to CP | 2.80 | | 2.80 | | 3.20 | | ns | Figs. 6, 9 |
| $t_h$ | Hold time<br>$S_n$ to CP | 0.00 | | 0.00 | | 0.00 | | ns | |
| $t_w(H)$ | Pulse width HIGH<br>CP | 2.50 | | 2.50 | | 2.50 | | ns | Figs. 5, 9 |

## AC ELECTRICAL CHARACTERISTICS

**Flat Pack** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V \pm 5\%$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $f_{MAX}$ | Maximum shift frequency | 300 | | 300 | | 300 | | MHz | Figs. 5, 8, 9 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>CP to $Q_n$ | 0.90<br>0.90 | 2.20<br>2.20 | 1.10<br>1.10 | 2.20<br>2.20 | 1.10<br>1.10 | 2.35<br>2.35 | ns<br>ns | Figs. 5, 7, 9 |
| $t_{TLH}$<br>$t_{THL}$ | Transition time<br>20% to 80%, 80% to 20% | 0.45<br>0.45 | 1.40<br>1.40 | 0.45<br>0.45 | 1.30<br>1.30 | 0.45<br>0.45 | 1.40<br>1.40 | ns<br>ns | |
| $t_s$ | Setup time<br>$D_n$, $P_n$ to CP | 1.20 | | 1.20 | | 1.50 | | ns | Figs. 6, 9 |
| $t_h$ | Hold time<br>$D_n$, $P_n$ to CP | 0.50 | | 0.50 | | 0.50 | | ns | |
| $t_s$ | Setup time<br>$S_n$ to CP | 2.80 | | 2.80 | | 3.20 | | ns | Figs. 6, 9 |
| $t_h$ | Hold time<br>$S_n$ to CP | 0.00 | | 0.00 | | 0.00 | | ns | |
| $t_w(H)$ | Pulse width HIGH<br>CP | 2.50 | | 2.50 | | 2.50 | | ns | Figs. 5, 9 |

## AC WAVEFORMS

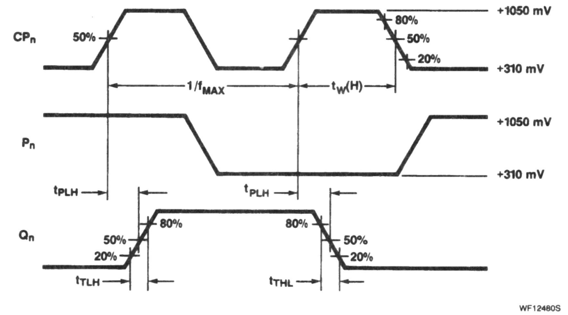

CPn
50%
80%
50%
20%
+1050 mV
+310 mV
1/fMAX
tw(H)
Pn
+1050 mV
+310 mV
tPLH
tPLH
Qn
80%
80%
50%
20%
50%
20%
tTLH
tTHL
WF12480S

**Figure 5. Propagation Delay For Clock to Outputs and Transition Times**

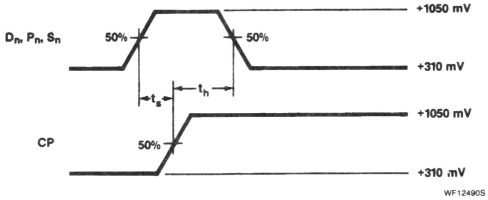
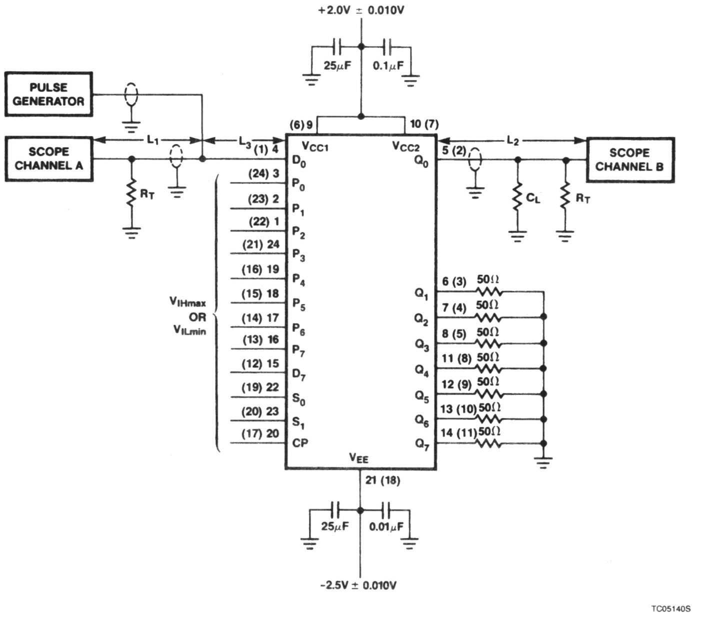

Dn, Pn, Sn
50%
50%
+1050 mV
+310 mV
ts
th
CP
50%
+1050 mV
+310 mV
WF12490S

**Figure 6. Data Setup and Hold Time**

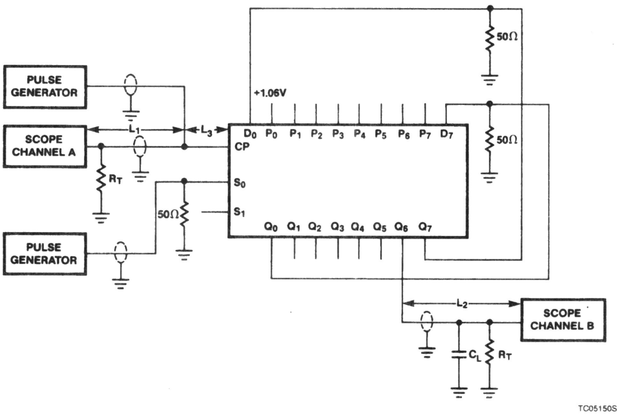
## TEST CIRCUITS AND WAVEFORMS


+2.0V ± 0.010V
25µF
0.1µF
PULSE GENERATOR
SCOPE CHANNEL A
L1
L3
RT
(6) 9
10 (7)
(1) 4
VCC1
VCC2
D0
Q0
5 (2)
L2
SCOPE CHANNEL B
CL
RT
(24) 3
P0
(23) 2
P1
(22) 1
P2
(21) 24
P3
(16) 19
P4
(15) 18
P5
(14) 17
P6
(13) 16
P7
(12) 15
D7
(19) 22
S0
(20) 23
S1
(17) 20
CP
VIHmax OR VILmin
6 (3) 50Ω
Q1
7 (4) 50Ω
Q2
8 (5) 50Ω
Q3
11 (8) 50Ω
Q4
12 (9) 50Ω
Q5
13 (10) 50Ω
Q6
14 (11) 50Ω
Q7
VEE
21 (18)
25µF
0.01µF
-2.5V ± 0.010V
TC05140S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1µF and 25µF from GND to $V_{CC}$, 0.01µF and 25µF from GND to $V_{EE}$. (0.01 and 0.1µF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance ≤ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.
11. Pins connections are for Flat Pack and in parentheses for Ceramic DIP.

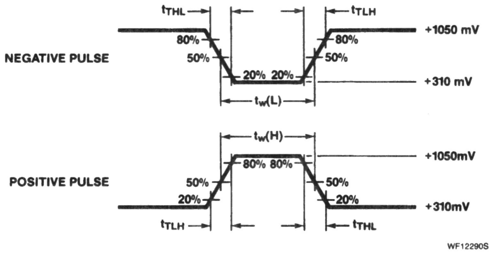
Figure 7. Test Circuit


50Ω
PULSE GENERATOR
SCOPE CHANNEL A
L1
L3
+1.06V
D0 P0 P1 P2 P3 P4 P5 P6 P7 D7
CP
S0
S1
RT
50Ω
50Ω
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
PULSE GENERATOR
L2
SCOPE CHANNEL B
CL
RT
TC05150S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1µF and 25µF from GND to $V_{CC}$, 0.01µF and 25µF from GND to $V_{EE}$. (0.01 and 0.1µF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance ≤ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.
11. Pins connections are for Flat Pack and in parentheses for Ceramic DIP.

Figure 8. Shift Frequency Test Circuit (Shift Left)


$t_{THL}$
$t_{TLH}$
80%
50%
20% 20%
NEGATIVE PULSE
$t_w(L)$
+1050 mV
+310 mV
$t_w(H)$
80% 80%
POSITIVE PULSE
50%
20%
$t_{TLH}$
$t_{THL}$
+1050mV
+310mV
WF12290S

**INPUT PULSE REQUIREMENTS**
**$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -2.5V \pm 0.010V$, $V_T$ = GND (0V)**

| Family | Amplitude | Rep Rate | Pulse Width | $t_{TLH}$ | $t_{THL}$ |
|---|---|---|---|---|---|
| 100K ECL | 740mVp-p | 1MHz | 500ns | 0.7 ±0.1ns | 0.7 ±0.1ns |

Figure 9. Input Pulse Definition

Signetics

# 100145

# Read-While-Write Register File

**16 × 4 Read-While-Write Register File**
***Preliminary Specification***

**ECL Products**

## DESCRIPTION

The 100145 is a 64-bit Register File organized as an array of 16 × 4. Separate address inputs for Read ($AR_n$) and Write ($AW_n$) are intended for shorter overall cycle time by allowing one address to be setting up, while the other is being executed.

Four output latches, which store data from previous operation while writing is in progress, also increase operating speed. The Write Enable input ($\overline{WE}$) selects the Read or Write mode. In the Read mode, the outputs can be forced LOW by a HIGH level on either of the output enables ($\overline{OE}_n$). One $\overline{WE}$ and one $\overline{OE}$ can be tied together, to serve as a Chip Select ($\overline{CS}$). When $\overline{CS}$ input is HIGH (with other $\overline{OE}$ at LOW) the circuit is in the Read mode and the data are latched in the output latches, and become available as soon as $\overline{CS}$ goes LOW.

The Master Reset signal (MR) clears all cells, forces the outputs LOW and resets the output latches.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 100145 | 3.5ns | 167mA |

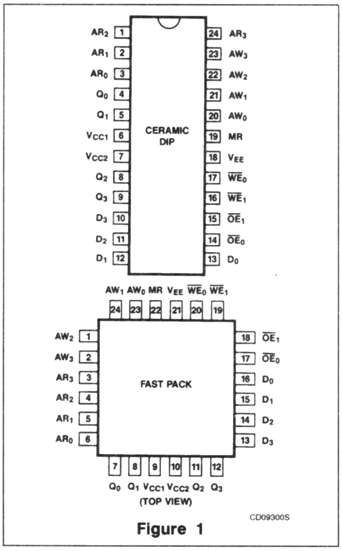
## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} = GND$; $V_{EE} = -4.2V$ to $-4.8V$<br>$T_A = 0°C$ to $+85°C$ |
|---|---|
| Ceramic DIP | 100145F |
| Ceramic Flat Pack | 100145Y |

## PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_0 - D_3$ | Data Inputs |
| $AR_0 - AR_3$ | Read Address Inputs |
| $AW_0 - AW_3$ | Write Address Inputs (Active LOW) |
| $\overline{WE}_0 - \overline{WE}_1$ | Write Enable Inputs |
| $\overline{MR}$ | Master Reset Input |
| $\overline{OE}_1 - \overline{OE}_2$ | Output Enable Inputs |
| $Q_0 - Q_3$ | Data Outputs |

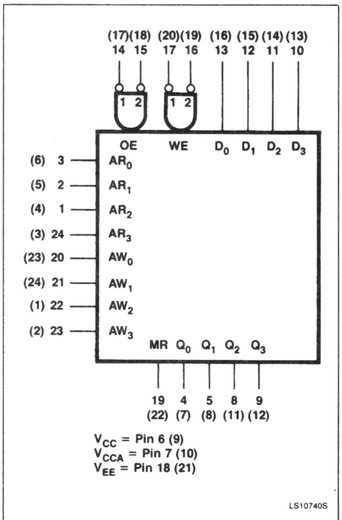
## PIN CONFIGURATION



AR2 1
AR1 2
AR0 3
Q0 4
Q1 5
VCC1 6
VCC2 7
Q2 8
Q3 9
D3 10
D2 11
D1 12
CERAMIC DIP
24 AR3
23 AW3
22 AW2
21 AW1
20 AW0
19 MR
18 VEE
17 WE0
16 WE1
15 OE1
14 OE0
13 D0
AW1 AW0 MR VEE WE0 WE1
24 23 22 21 20 19
AW2 1
AW3 2
AR3 3
AR2 4
AR1 5
AR0 6
FAST PACK
18 OE1
17 OE0
16 D0
15 D1
14 D2
13 D3
7 8 9 10 11 12
Q0 Q1 VCC1 VCC2 Q2 Q3
(TOP VIEW)
CD09300S

Figure 1

## LOGIC SYMBOL



(17)(18) (20)(19) (16) (15) (14) (13)
14 15 17 16 13 12 11 10
1 2
1 2
OE
WE
D0 D1 D2 D3
(6) 3 AR0
(5) 2 AR1
(4) 1 AR2
(3) 24 AR3
(23) 20 AW0
(24) 21 AW1
(1) 22 AW2
(2) 23 AW3
MR Q0 Q1 Q2 Q3
19 4 5 8 9
(22) (7) (8) (11) (12)
VCC = Pin 6 (9)
VCCA = Pin 7 (10)
VEE = Pin 18 (21)
LS10740S

Figure 2

# Read-While-Write Register File 100145

## LOGIC DIAGRAM

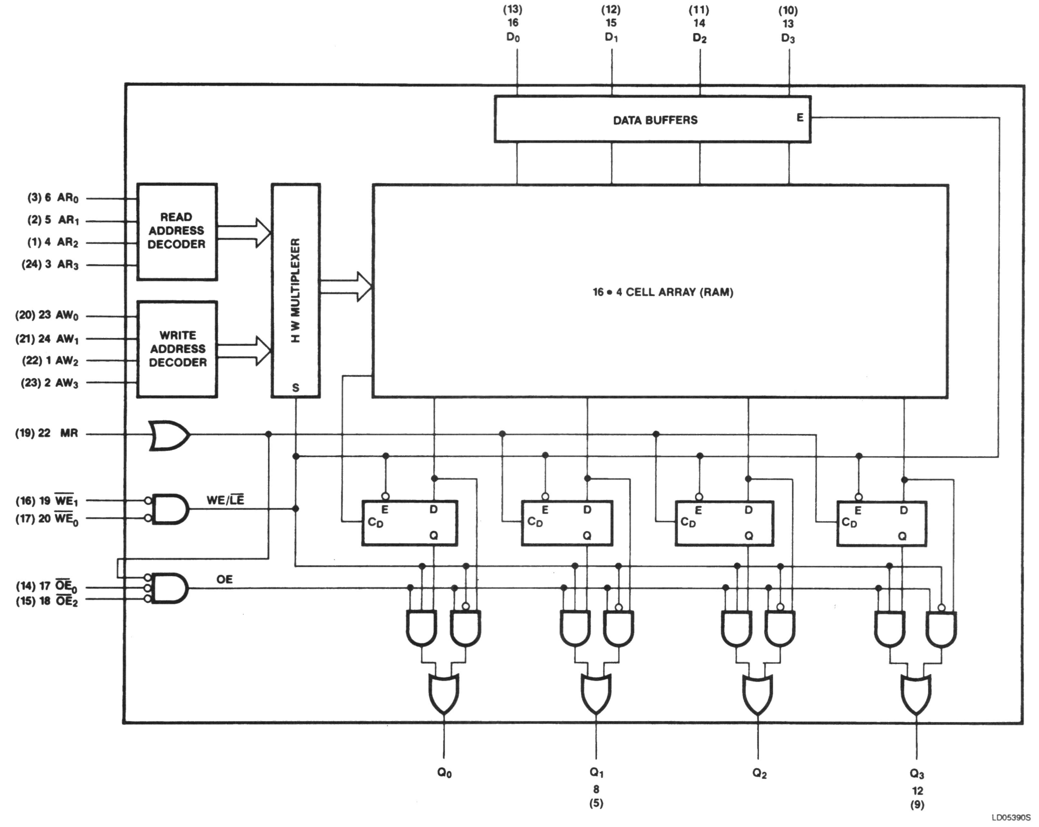

(13) 16 D0
(12) 15 D1
(11) 14 D2
(10) 13 D3
DATA BUFFERS
E
(3) 6 AR0
(2) 5 AR1
(1) 4 AR2
(24) 3 AR3
READ ADDRESS DECODER
(20) 23 AW0
(21) 24 AW1
(22) 1 AW2
(23) 2 AW3
WRITE ADDRESS DECODER
H W MULTIPLEXER
S
16 • 4 CELL ARRAY (RAM)
(19) 22 MR
(16) 19 WE1
(17) 20 WE0
WE/LE
(14) 17 OE0
(15) 18 OE2
OE
E
D
CD
Q
Q0
Q1
8
(5)
Q2
Q3
12
(9)
LD05390S

Figure 3

## FUNCTION TABLE

| INPUTS | | | | | | OUTPUTS | | | | OPERATING MODE | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $D_n$ | $\overline{WE}_0$ | $\overline{WE}_1$ | $\overline{OE}_0$ | $\overline{OE}_1$ | MR | $Q_0$ | $Q_1$ | $Q_2$ | $Q_3$ | | |
| X | L | L | L | L | L | Data from Latches | | | | Write | Hold (previous operation) |
| X | H | X | L | L | L | Read Data | | | | Read | Data are latched |
| X | H | X | X | H | L | L | | | | Read | Data are latched |
| X | H | X | H | X | L | L | | | | Read | Data are latched |
| X | X | H | L | L | L | Read Data | | | | Read | Data are latched |
| X | X | H | X | H | L | L | | | | Read | Data are latched |
| X | X | H | H | X | L | L | | | | Read | Data are latched |
| X | X | X | X | X | H | L | | | | Clears all cells | |

Positive Logic:
H = HIGH state (the more positive voltage level) = 1
L = LOW state (the less positive voltage level) = 0
X = Don't Care

# Read-While-Write Register File

# 100145

**ABSOLUTE MAXIMUM RATINGS** (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | 100K ECL | UNIT |
|---|---|---|---|
| $V_{EE}$ | Supply voltage ($V_{CC1} = V_{CC2} =$ GND) | −7.0 to 0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | $V_{EE}$ to +0.5 | V |
| $I_O$ | Output source current | −55 | mA |
| $T_S$ | Storage temperature | −65 to +150 | °C |
| $T_J$ | Maximum junction temperature | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | | 100K ECL | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | −4.2 | −4.5 | −4.8 | V |
| $V_{EE}$ | Supply voltage (negative) when operating with 10K ECL family | | | | | −5.7 | V |
| $V_{IH}$ | HIGH level input voltage | $V_{CC1} = V_{CC2} =$ GND<br>$T_A = 0°C$ to $+85°C$ | $V_{EE} = -4.2V$ | −1150 | | −880 | mV |
| | | | $V_{EE} = -4.5V$ | −1165 | | | |
| | | | $V_{EE} = -4.8V$ | | | | |
| $V_{IHT}$ | HIGH level input threshold voltage | | $V_{EE} = -4.2V$ | −1150 | | | mV |
| | | | $V_{EE} = -4.5V$ | −1165 | | | mV |
| | | | $V_{EE} = -4.8V$ | | | | |
| $V_{ILT}$ | LOW level input threshold voltage | | $V_{EE} = -4.2V$ | | | −1475 | mV |
| | | | $V_{EE} = -4.5V$ | | | | |
| | | | $V_{EE} = -4.8V$ | | | −1490 | mV |
| $V_{IL}$ | LOW level input voltage | | $V_{EE} = -4.2V$ | −1810 | | −1475 | mV |
| | | | $V_{EE} = -4.5V$ | | | | |
| | | | $V_{EE} = -4.8V$ | | | −1490 | |
| $T_A$ | Operating ambient temperature | | | 0 | +25 | +85 | °C |

**NOTE:**
When operating at other than specified voltages (−4.2V, −4.5V, −4.8V) DC & AC Characteristics will vary slightly from specified values.

# Read-While-Write Register File

# 100145

**DC ELECTRICAL CHARACTERISTICS** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$, $T_A = 0°C$ to $+85°C$ unless otherwise specified[1,3]

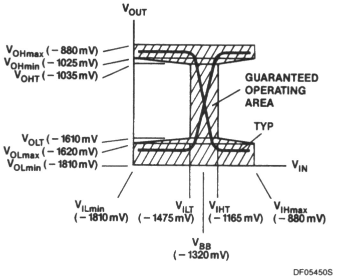
| PARAMETER | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] | |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | $V_{EE} = -4.2V$ | −1025 | | −870 | mV | $V_{IN} = V_{IHmax}$ or $V_{IN} = V_{ILmin}$ | Loading with 50Ω to −2.0V ±0.010V |
| | | $V_{EE} = -4.5V$ | −1025 | −955 | −880 | mV | | |
| | | $V_{EE} = -4.8V$ | −1035 | | −880 | mV | | |
| $V_{OHT}$ | HIGH level output threshold voltage | $V_{EE} = -4.2V$ | −1035 | | | mV | $V_{IN} = V_{IHmin}$ or $V_{IN} = V_{ILmax}$ | |
| | | $V_{EE} = -4.5V$ | −1035 | | | mV | | |
| | | $V_{EE} = -4.8V$ | −1045 | | | mV | | |
| $V_{OLT}$ | LOW level output threshold voltage | $V_{EE} = -4.2V$ | | | −1590 | mV | $V_{IN} = V_{IHmin}$ or $V_{IN} = V_{ILmax}$ | |
| | | $V_{EE} = -4.5V$ | | | −1610 | mV | | |
| | | $V_{EE} = -4.8V$ | | | −1610 | mV | | |
| $V_{OL}$ | LOW level output voltage | $V_{EE} = -4.2V$ | −1810 | | −1600 | mV | $V_{IN} = V_{IHmax}$ or $V_{IN} = V_{ILmin}$ | |
| | | $V_{EE} = -4.5V$ | −1810 | −1705 | −1620 | mV | | |
| | | $V_{EE} = -4.8V$ | −1830 | | −1620 | mV | | |
| $I_{IH}$ | HIGH level input current | | | | 240 | μA | $V_{IN} = V_{IHmax}$ | |
| $I_{IL}$ | LOW level input current | | 0.5 | | | μA | $V_{IN} = V_{ILmin}$ | |
| $-I_{EE}$ | $V_{EE}$ supply current | | 119 | 167 | 247 | mA | Inputs open | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | $V_{EE} = -4.2V$<br>$T_A = +25°C$ | | | 0.025 | V/V | | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | | 0.050 | V/V | | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 4.

## Read-While-Write Register File

## 100145



NOTES:

| | |
|---|---|
| $V_{IHmax}$ | – Maximum HIGH level input voltage (the most positive $V_{IH}$). |
| $V_{IHT}$ | – HIGH level input threshold voltage. |
| $V_{ILT}$ | – LOW level input threshold voltage. |
| $V_{ILmin}$ | – Minimum LOW level input voltage (the most negative $V_{IL}$). |
| $V_{OHmax}$ | – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition. |
| $V_{OHmin}$ | – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition. |
| $V_{OHT}$ | – HIGH level output threshold voltage with the inputs set to their respective threshold levels. |
| $V_{OLT}$ | – LOW level output threshold voltage with the inputs set to their respective threshold levels. |
| $V_{OLmax}$ | – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions. |
| $V_{OLmin}$ | – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions. |
| $V_{BB}$ | – Reference bias voltage. The internally generated reference voltage which is used to set the input and output threshold level. |

**Figure 4. Transfer Characteristics**

## AC ELECTRICAL CHARACTERISTICS

**Ceramic DIP** $V_{CC1} = V_{CC2} =$ GND, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$

| PARAMETER | | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | | |
| Access recovery timing | $t_{AA}$ | Address access $AR_n$ to $Q_n$ | 2.00 | 6.70 | 2.00 | 6.70 | 2.00 | 6.70 | ns | Fig. 5 |
| | $t_{OR}$ | Output recovery $\overline{OE}_n$ to $Q_n$ | 1.00 | 3.10 | 1.00 | 3.10 | 1.00 | 3.10 | ns | Fig. 6 |
| | $t_{OD}$ | Output disable $\overline{OE}$ to $Q_n$ | 1.00 | 3.10 | 1.00 | 3.10 | 1.00 | 3.10 | ns | |
| Read timing | $t_{RSA1}$ | Address setup $\overline{AR}_n$ to WE | 3.20 | | 3.20 | | 3.20 | | ns | Fig. 7 |
| | $t_{WEQ}$ | Output delay $\overline{WE}$ to $Q_n$ | 2.00 | 6.10 | 2.00 | 6.10 | 2.00 | 6.10 | ns | |
| Output latch timing | $t_{RSA2}$ | Address setup $\overline{AR}_n$ to WE | 8.50 | | 8.50 | | 8.50 | | ns | Fig. 8 |
| | $t_{RHA}$ | Address hold $AR_n$ to $\overline{WE}$ | 0.20 | | 0.20 | | 0.20 | | ns | Fig. 9 |
| Write timing | $t_{WSA}$ | Address setup $\overline{AW}_n$ to WE | 3.20 | | 3.20 | | 3.20 | | ns | Fig. 10 |
| | $t_{WHA}$ | Address hold $\overline{WE}$ to $AW_n$ | 0.20 | | 0.20 | | 0.20 | | ns | |
| | $t_{WSD}$ | Data setup $D_n$ to $\overline{WE}$ | 6.20 | | 6.20 | | 6.20 | | ns | |
| | $t_{WHD}$ | Data hold $\overline{WE}$ to $D_n$ | 0.20 | | 0.20 | | 0.20 | | ns | |
| | $t_W$ | Write pulse width, LOW | 5.20 | | 5.20 | | 5.20 | | ns | |
| Master reset timing | $t_M$ | Reset pulse width, LOW | 13.7 | | 13.7 | | 13.7 | | ns | Fig. 11 |
| | $t_{MHW}$ | $\overline{WE}$ hold to write | 18.4 | | 18.4 | | 18.4 | | ns | |
| | $t_{MQ}$ | Output disable MR to $Q_n$ | 3.70 | | 3.70 | | 3.70 | | ns | Fig. 12 |
| $t_{TLH}$<br>$t_{THL}$ | Transition time<br>20% to 80%, 80% to 20% | | 0.50<br>0.50 | 2.30<br>2.30 | 0.50<br>0.50 | 2.30<br>2.30 | 0.50<br>0.50 | 2.30<br>2.30 | ns<br>ns | Figs. 13, 14 |

# Read-While-Write Register File

# 100145

## AC ELECTRICAL CHARACTERISTICS

### Ceramic DIP $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V \pm 5\%$

| PARAMETER | | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | | |
| Access recovery timing | $t_{AA}$ | Address access $AR_n$ to $Q_n$ | 2.00 | 6.70 | 2.00 | 6.70 | 2.00 | 6.70 | ns | Fig. 5 |
| | $t_{OR}$ | Output recovery $\overline{OE}_n$ to $Q_n$ | 1.00 | 3.10 | 1.00 | 3.10 | 1.00 | 3.10 | ns | Fig. 6 |
| | $t_{OD}$ | Output disable $\overline{OE}$ to $Q_n$ | 1.00 | 3.10 | 1.00 | 3.10 | 1.00 | 3.10 | ns | |
| Read timing | $t_{RSA1}$ | Address setup $\overline{AR}_n$ to WE | 3.20 | | 3.20 | | 3.20 | | ns | Fig. 7 |
| | $t_{WEQ}$ | Output delay $\overline{WE}$ to $Q_n$ | 2.00 | 6.10 | 2.00 | 6.10 | 2.00 | 6.10 | ns | |
| Output latch timing | $t_{RSA2}$ | Address setup $\overline{AR}_n$ to WE | 8.50 | | 8.50 | | 8.50 | | ns | Fig. 8 |
| | $t_{RHA}$ | Address hold $AR_n$ to $\overline{WE}$ | 0.20 | | 0.20 | | 0.20 | | ns | Fig. 9 |
| Write timing | $t_{WSA}$ | Address setup $\overline{AW}_n$ to WE | 3.20 | | 3.20 | | 3.20 | | ns | Fig. 10 |
| | $t_{WHA}$ | Address hold $\overline{WE}$ to $AW_n$ | 0.20 | | 0.20 | | 0.20 | | ns | |
| | $t_{WSD}$ | Data setup $D_n$ to $\overline{WE}$ | 6.20 | | 6.20 | | 6.20 | | ns | |
| | $t_{WHD}$ | Data hold $\overline{WE}$ to $D_n$ | 0.20 | | 0.20 | | 0.20 | | ns | |
| | $t_W$ | Write pulse width, LOW | 5.20 | | 5.20 | | 5.20 | | ns | |
| Master reset timing | $t_M$ | Reset pulse width, LOW | 13.7 | | 13.7 | | 13.7 | | ns | Fig. 11 |
| | $t_{MHW}$ | $\overline{WE}$ hold to write | 18.4 | | 18.4 | | 18.4 | | ns | |
| | $t_{MQ}$ | Output disable MR to $Q_n$ | 3.70 | | 3.70 | | 3.70 | | ns | Fig. 12 |
| $t_{TLH}$<br>$t_{THL}$ | | Transition time<br>20% to 80%, 80% to 20% | 0.50<br>0.50 | 2.30<br>2.30 | 0.50<br>0.50 | 2.30<br>2.30 | 0.50<br>0.50 | 2.30<br>2.30 | ns<br>ns | Figs. 13, 14 |

### Flat Pack $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$

| PARAMETER | | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | | |
| Access recovery timing | $t_{AA}$ | Address access $AR_n$ to $Q_n$ | 2.00 | 6.50 | 2.00 | 6.50 | 2.00 | 6.50 | ns | Fig. 5 |
| | $t_{OR}$ | Output recovery $OE_n$ to $Q_n$ | 1.00 | 2.90 | 1.00 | 2.90 | 1.00 | 2.90 | ns | Fig. 6 |
| | $t_{OD}$ | Output disable OE to $Q_n$ | 1.00 | 2.90 | 1.00 | 2.90 | 1.00 | 2.90 | ns | |
| Read timing | $t_{RSA1}$ | Address setup $AR_n$ to WE | 3.00 | | 3.00 | | 3.00 | | ns | Fig. 7 |
| | $t_{WEQ}$ | Output delay WE to $Q_n$ | 2.00 | 5.90 | 2.00 | 5.90 | 2.00 | 5.90 | ns | |
| Output latch timing | $t_{RSA2}$ | Address setup $AR_n$ to WE | 8.30 | | 8.30 | | 8.30 | | ns | Fig. 8 |
| | $t_{RHA}$ | Address hold $AR_n$ to WE | 0.00 | | 0.00 | | 0.00 | | ns | Fig. 9 |
| Write timing | $t_{WSA}$ | Address setup $AW_n$ to WE | 3.00 | | 3.00 | | 3.00 | | ns | Fig. 10 |
| | $t_{WHA}$ | Address hold WE to $AW_n$ | 0.00 | | 0.00 | | 0.00 | | ns | |
| | $t_{WSD}$ | Data setup $D_n$ to WE | 6.00 | | 6.00 | | 6.00 | | ns | |
| | $t_{WHD}$ | Data hold WE to $D_n$ | 0.00 | | 0.00 | | 0.00 | | ns | |
| | $t_W$ | Write pulse width, LOW | 5.00 | | 5.00 | | 5.00 | | ns | |
| Master reset timing | $t_M$ | Reset pulse width, LOW | 13.5 | | 13.5 | | 13.5 | | ns | Fig. 11 |
| | $t_{MHW}$ | WE hold to write | 18.2 | | 18.2 | | 18.2 | | ns | |
| | $t_{MQ}$ | Output disable MR to $Q_n$ | 3.50 | | 3.50 | | 3.50 | | ns | Fig. 12 |
| $t_{TLH}$<br>$t_{THL}$ | | Transition time<br>20% to 80%, 80% to 20% | 0.50<br>0.50 | 2.20<br>2.20 | 0.50<br>0.50 | 2.20<br>2.20 | 0.50<br>0.50 | 2.20<br>2.20 | ns<br>ns | Figs. 13, 14 |

# Read-While-Write Register File

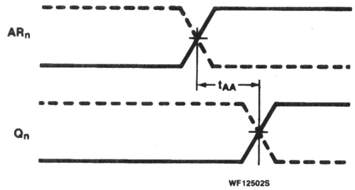
# 100145

## AC ELECTRICAL CHARACTERISTICS

**Flat Pack** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V \pm 5\%$

| PARAMETER | | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | | |
| Access recovery timing | $t_{AA}$ | Address access $AR_n$ to $Q_n$ | 2.00 | 6.50 | 2.00 | 6.50 | 2.00 | 6.50 | ns | Fig. 5 |
| | $t_{OR}$ | Output recovery $OE_n$ to $Q_n$ | 1.00 | 2.90 | 1.00 | 2.90 | 1.00 | 2.90 | ns | Fig. 6 |
| | $t_{OD}$ | Output disable OE to $Q_n$ | 1.00 | 2.90 | 1.00 | 2.90 | 1.00 | 2.90 | ns | |
| Read timing | $t_{RSA1}$ | Address setup $AR_n$ to WE | 3.00 | | 3.00 | | 3.00 | | ns | Fig. 7 |
| | $t_{WEQ}$ | Output delay WE to $Q_n$ | 2.00 | 5.90 | 2.00 | 5.90 | 2.00 | 5.90 | ns | |
| Output latch timing | $t_{RSA2}$ | Address setup $AR_n$ to WE | 8.30 | | 8.30 | | 8.30 | | ns | Fig. 8 |
| | $t_{RHA}$ | Address hold $AR_n$ to WE | 0.00 | | 0.00 | | 0.00 | | ns | Fig. 9 |
| Write timing | $t_{WSA}$ | Address setup $AW_n$ to WE | 3.00 | | 3.00 | | 3.00 | | ns | Fig. 10 |
| | $t_{WHA}$ | Address hold WE to $AW_n$ | 0.00 | | 0.00 | | 0.00 | | ns | |
| | $t_{WSD}$ | Data setup $D_n$ to WE | 6.00 | | 6.00 | | 6.00 | | ns | |
| | $t_{WHD}$ | Data hold WE to $D_n$ | 0.00 | | 0.00 | | 0.00 | | ns | |
| | $t_W$ | Write pulse width, LOW | 5.00 | | 5.00 | | 5.00 | | ns | |
| Master reset timing | $t_M$ | Reset pulse width, LOW | 13.5 | | 13.5 | | 13.5 | | ns | Fig. 11 |
| | $t_{MHW}$ | WE hold to write | 18.2 | | 18.2 | | 18.2 | | ns | |
| | $t_{MQ}$ | Output disable MR to $Q_n$ | 3.50 | | 3.50 | | 3.50 | | ns | Fig. 12 |
| $t_{TLH}$ | | Transition time | 0.50 | 2.20 | 0.50 | 2.20 | 0.50 | 2.20 | ns | Figs. 13, 14 |
| $t_{THL}$ | | 20% to 80%, 80% to 20% | 0.50 | 2.20 | 0.50 | 2.20 | 0.50 | 2.20 | ns | |

## AC WAVEFORMS


AR$_n$
t$_{AA}$
Q$_n$
WF12502S

($\overline{WE}_1$ OR $\overline{WE}_2$ = H, $\overline{OE}_1$ = $\overline{OE}_2$ = L)
Figure 5. Access/Recovery Times

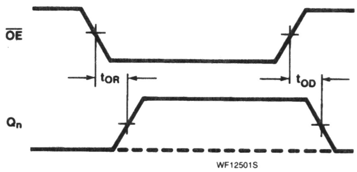

$\overline{OE}$
t$_{OR}$
t$_{OD}$
Q$_n$
WF12501S

Figure 6. Access/Recovery Times

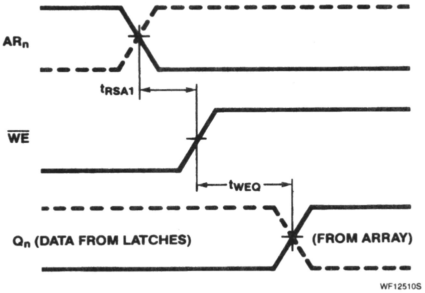

AR$_n$
t$_{RSA1}$
$\overline{WE}$
t$_{WEQ}$
Q$_n$ (DATA FROM LATCHES)
(FROM ARRAY)
WF12510S

Figure 7. Read Timing

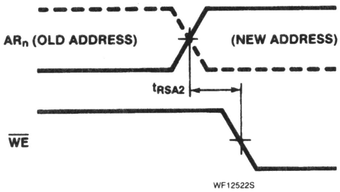

AR$_n$ (OLD ADDRESS)
(NEW ADDRESS)
t$_{RSA2}$
$\overline{WE}$
WF12522S

Figure 8. Output Latch Timing

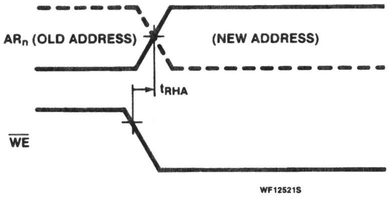

AR$_n$ (OLD ADDRESS)
(NEW ADDRESS)
t$_{RHA}$
$\overline{WE}$
WF12521S

Figure 9. Output Latch Timing

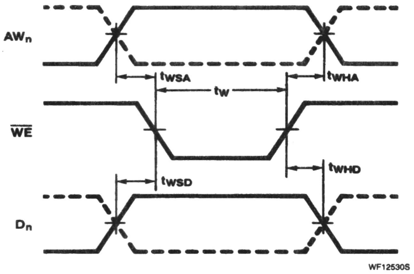

AW$_n$
t$_{WSA}$
t$_W$
t$_{WHA}$
$\overline{WE}$
t$_{WHD}$
t$_{WSD}$
D$_n$
WF12530S

Figure 10. Write Timing

## Read-While-Write Register File 100145

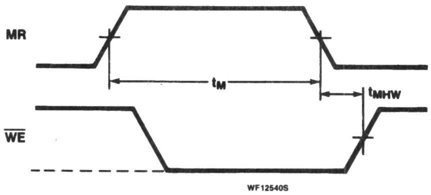

MR
$\overline{WE}$
$t_M$
$t_{MHW}$
WF12540S

Figure 11. Master Reset Timing

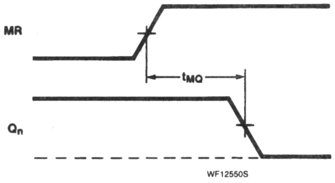
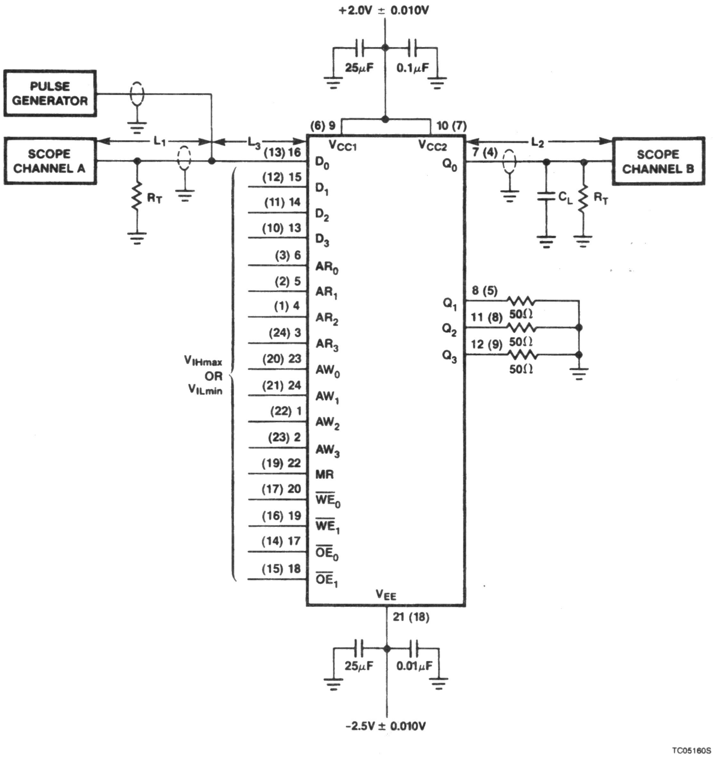

MR
$t_{MQ}$
$Q_n$
WF12550S

Figure 12. Master Reset Timing

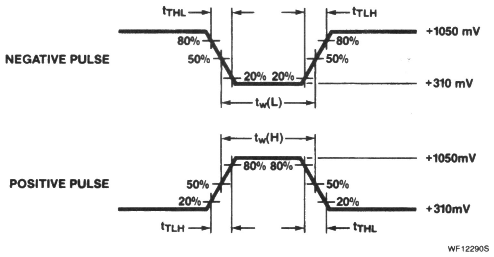
## TEST CIRCUITS AND WAVEFORMS


+2.0V ± 0.010V
25μF
0.1μF
PULSE GENERATOR
SCOPE CHANNEL A
$L_1$
$L_3$
$R_T$
(6) 9
10 (7)
$V_{CC1}$
$V_{CC2}$
(13) 16 $D_0$
(12) 15 $D_1$
(11) 14 $D_2$
(10) 13 $D_3$
(3) 6 $AR_0$
(2) 5 $AR_1$
(1) 4 $AR_2$
(24) 3 $AR_3$
(20) 23 $AW_0$
(21) 24 $AW_1$
(22) 1 $AW_2$
(23) 2 $AW_3$
(19) 22 MR
(17) 20 $\overline{WE}_0$
(16) 19 $\overline{WE}_1$
(14) 17 $\overline{OE}_0$
(15) 18 $\overline{OE}_1$
$V_{IHmax}$ OR $V_{ILmin}$
$Q_0$ 7 (4)
$L_2$
SCOPE CHANNEL B
$C_L$
$R_T$
$Q_1$ 8 (5)
$Q_2$ 11 (8) 50Ω
$Q_3$ 12 (9) 50Ω
50Ω
$V_{EE}$
21 (18)
25μF
0.01μF
-2.5V ± 0.010V
TC05160S

NOTES:

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1μF and 25μF from GND to $V_{CC}$, 0.01μF and 25μF from GND to $V_{EE}$. (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance $\leqslant$ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.
11. Pins connections for Flat Pack and in parentheses for Ceramic DIP.

Figure 13. Test Circuit


tTHL
tTLH
+1050 mV
80%
50%
NEGATIVE PULSE
20% 20%
+310 mV
tw(L)
tw(H)
+1050mV
80% 80%
POSITIVE PULSE
50%
20%
+310mV
tTLH
tTHL
WF12290S

| INPUT PULSE REQUIREMENTS<br>$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -2.5V \pm 0.010V$, $V_T = GND\ (0V)$ | | | | | |
|---|---|---|---|---|---|
| **Family** | **Amplitude** | **Rep Rate** | **Pulse Width** | $t_{TLH}$ | $t_{THL}$ |
| 100K ECL | 740mVp-p | 1MHz | 500ns | 0.7 ±0.1ns | 0.7 ±0.1ns |

Figure 14. Input Pulse Definition

Signetics

# 100150
# Latch

**Hex D-Type Latch**
***Product Specification***

**ECL Products**

## DESCRIPTION

The 100150 contains six D-type latches with true and complement outputs, a pair of common enables ($\overline{E}_a$ and $\overline{E}_b$), and a common Master Reset (MR). A Q output follows its D input when both $\overline{E}_a$ and $\overline{E}_b$ are LOW. When either $\overline{E}_a$ or $\overline{E}_b$ (or both) are HIGH, a latch stores the last valid data present on its D input before $\overline{E}_a$ or $\overline{E}_b$ goes HIGH. The MR input overrides all other inputs and makes the Q output LOW.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 100150 | 1.2ns ($\overline{E}$)/0.85ns (Data) | 102mA |

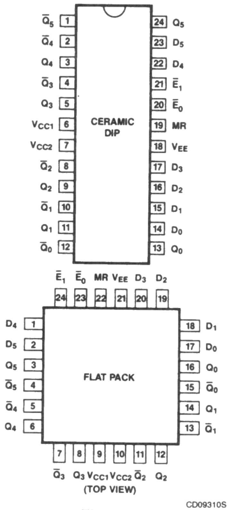
## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} =$ GND; $V_{EE} = -4.2V$ to $-4.8V$<br>$T_A = 0°C$ to $+85°C$ |
|---|---|
| Ceramic DIP | 100150F |
| Ceramic Flat Pack | 100150Y |

## PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_0 - D_5$ | Data Inputs |
| $\overline{E}_a$, $\overline{E}_b$ | Common Enable Inputs |
| MR | Master Reset Input |
| $Q_0 - Q_5$ | Data Outputs |
| $\overline{Q}_0 - \overline{Q}_5$ | Complementary Data Outputs |

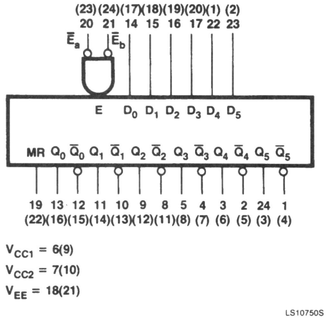
## PIN CONFIGURATION



$\overline{Q}_5$ 1
$\overline{Q}_4$ 2
$Q_4$ 3
$\overline{Q}_3$ 4
$Q_3$ 5
$V_{CC1}$ 6
$V_{CC2}$ 7
$\overline{Q}_2$ 8
$Q_2$ 9
$\overline{Q}_1$ 10
$Q_1$ 11
$\overline{Q}_0$ 12
24 $Q_5$
23 $D_5$
22 $D_4$
21 $\overline{E}_1$
20 $\overline{E}_0$
19 MR
18 $V_{EE}$
17 $D_3$
16 $D_2$
15 $D_1$
14 $D_0$
13 $Q_0$
CERAMIC DIP
$\overline{E}_1$ $\overline{E}_0$ MR $V_{EE}$ $D_3$ $D_2$
24 23 22 21 20 19
$D_4$ 1
$D_5$ 2
$Q_5$ 3
$\overline{Q}_5$ 4
$\overline{Q}_4$ 5
$Q_4$ 6
18 $D_1$
17 $D_0$
16 $Q_0$
15 $\overline{Q}_0$
14 $Q_1$
13 $\overline{Q}_1$
FLAT PACK
7 8 9 10 11 12
$\overline{Q}_3$ $Q_3$ $V_{CC1}$ $V_{CC2}$ $\overline{Q}_2$ $Q_2$
(TOP VIEW)
CD09310S

**Figure 1**

## LOGIC SYMBOL



(23)(24)(17)(18)(19)(20)(1) (2)
20 21 14 15 16 17 22 23
$\overline{E}_a$ $\overline{E}_b$
E $D_0$ $D_1$ $D_2$ $D_3$ $D_4$ $D_5$
MR $Q_0$ $\overline{Q}_0$ $Q_1$ $\overline{Q}_1$ $Q_2$ $\overline{Q}_2$ $Q_3$ $\overline{Q}_3$ $Q_4$ $\overline{Q}_4$ $Q_5$ $\overline{Q}_5$
19 13 12 11 10 9 8 5 4 3 2 24 1
(22)(16)(15)(14)(13)(12)(11)(8) (7) (6) (5) (3) (4)
$V_{CC1}$ = 6(9)
$V_{CC2}$ = 7(10)
$V_{EE}$ = 18(21)
LS10750S

**Figure 2**

## FUNCTION TABLE (Each Latch)

| INPUTS | | | | OUTPUTS | | OPERATING MODE |
|---|---|---|---|---|---|---|
| $D_n$ | $\overline{E}_0$ | $\overline{E}_1$ | MR | $Q_n$ | $\overline{Q}_n$ | |
| H | L | L | L | H | L | Latch |
| L | L | L | L | L | H | |
| X | X | H | L | Latched* | Latched* | |
| X | H | X | L | Latched* | Latched* | |
| X | X | X | H | L | H | Asynchronous |

*Retains data that is present before $\overline{E}$ positive transition

Positive Logic:

H = HIGH state (the more positive voltage) = 1

L = LOW state (the less positive voltage) = 0

X = Don't Care

## ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | 100K ECL | UNIT |
|---|---|---|---|
| $V_{EE}$ | Supply voltage ($V_{CC1}$ = $V_{CC2}$ = GND) | −7.0 to 0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | $V_{EE}$ to +0.5 | V |
| $I_O$ | Output source current | −55 | mA |
| $T_S$ | Storage temperature | −65 to +150 | °C |
| $T_J$ | Maximum junction temperature | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | | 100K ECL | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | −4.2 | −4.5 | −4.8 | V |
| $V_{EE}$ | Supply voltage (negative) when operating with 10K ECL family | | | | | −5.7 | V |
| $V_{IH}$ | HIGH level input voltage | $V_{CC1}$ = $V_{CC2}$ = GND<br>$T_A$ = 0°C to +85°C | $V_{EE}$ = −4.2V | −1150 | | −880 | mV |
| | | | $V_{EE}$ = −4.5V | −1165 | | | |
| | | | $V_{EE}$ = −4.8V | | | | |
| $V_{IHT}$ | HIGH level input threshold voltage | | $V_{EE}$ = −4.2V | −1150 | | | mV |
| | | | $V_{EE}$ = −4.5V | −1165 | | | mV |
| | | | $V_{EE}$ = −4.8V | | | | |
| $V_{ILT}$ | LOW level input threshold voltage | | $V_{EE}$ = −4.2V | | | −1475 | mV |
| | | | $V_{EE}$ = −4.5V | | | | |
| | | | $V_{EE}$ = −4.8V | | | −1490 | mV |
| $V_{IL}$ | LOW level input voltage | | $V_{EE}$ = −4.2V | −1810 | | −1475 | mV |
| | | | $V_{EE}$ = −4.5V | | | | |
| | | | $V_{EE}$ = −4.8V | | | −1490 | |
| $T_A$ | Operating ambient temperature | | | 0 | +25 | +85 | °C |

**NOTE:**

When operating at other than specified voltages (−4.2V, −4.5V, −4.8V) DC & AC Characteristics will vary slightly from specified values.

# Latch

# 100150

**DC ELECTRICAL CHARACTERISTICS** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$, $T_A = 0°C$ to $+85°C$ unless otherwise specified[1,3]

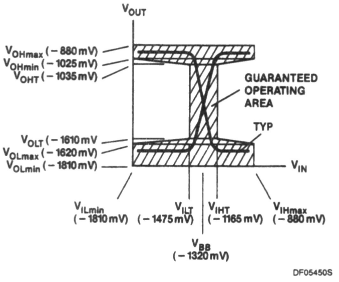
| PARAMETER | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] | |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | $V_{EE} = -4.2V$ | -1025 | | -870 | mV | $V_{IN} = V_{IHmax}$ or $V_{IN} = V_{ILmin}$ | Loading with 50Ω to -2.0V ±0.010V |
| | | $V_{EE} = -4.5V$ | -1025 | -955 | -880 | mV | | |
| | | $V_{EE} = -4.8V$ | -1035 | | -880 | mV | | |
| $V_{OHT}$ | HIGH level output threshold voltage | $V_{EE} = -4.2V$ | -1035 | | | mV | $V_{IN} = V_{IHmin}$ or $V_{IN} = V_{ILmax}$ | |
| | | $V_{EE} = -4.5V$ | -1035 | | | mV | | |
| | | $V_{EE} = -4.8V$ | -1045 | | | mV | | |
| $V_{OLT}$ | LOW level output threshold voltage | $V_{EE} = -4.2V$ | | | -1590 | mV | $V_{IN} = V_{IHmin}$ or $V_{IN} = V_{ILmax}$ | |
| | | $V_{EE} = -4.5V$ | | | -1610 | mV | | |
| | | $V_{EE} = -4.8V$ | | | -1610 | mV | | |
| $V_{OL}$ | LOW level output voltage | $V_{EE} = -4.2V$ | -1810 | | -1600 | mV | $V_{IN} = V_{IHmax}$ or $V_{IN} = V_{ILmin}$ | |
| | | $V_{EE} = -4.5V$ | -1810 | -1705 | -1620 | mV | | |
| | | $V_{EE} = -4.8V$ | -1830 | | -1620 | mV | | |
| $I_{IH}$ | HIGH level input current | R | | | 450 | μA | $V_{IN} = V_{IHmax}$ | |
| | | $D_n$ | | | 340 | μA | | |
| | | $\overline{E}_a$, $\overline{E}_b$ | | | 520 | μA | | |
| $I_{IL}$ | LOW level input current | | 0.5 | | | μA | $V_{IN} = V_{ILmin}$ | |
| $-I_{EE}$ | $V_{EE}$ supply current | | 79 | 102 | 159 | mA | Inputs open | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | $V_{EE} = -4.2V$<br>$T_A = +25°C$ | | | 0.035 | V/V | | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | | 0.070 | V/V | | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 3.

# Latch

# 100150



**NOTES:**

| | |
|---|---|
| $V_{IHmax}$ | – Maximum HIGH level input voltage (the most positive $V_{IH}$). |
| $V_{IHT}$ | – HIGH level input threshold voltage. |
| $V_{ILT}$ | – LOW level input threshold voltage. |
| $V_{ILmin}$ | – Minimum LOW level input voltage (the most negative $V_{IL}$). |
| $V_{OHmax}$ | – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition. |
| $V_{OHmin}$ | – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition. |
| $V_{OHT}$ | – HIGH level output threshold voltage with the inputs set to their respective threshold levels. |
| $V_{OLT}$ | – LOW level output threshold voltage with the inputs set to their respective threshold levels. |
| $V_{OLmax}$ | – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions. |
| $V_{OLmin}$ | – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions. |
| $V_{BB}$ | – Reference bias voltage. The internally generated reference voltage which is used to set the input and output threshold level. |

**Figure 3. Transfer Characteristics**

## AC ELECTRICAL CHARACTERISTICS

**Ceramic DIP** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$

| | PARAMETER | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$D_n$ to $Q_n$ | 0.45<br>0.45 | 1.50<br>1.50 | 0.50<br>0.50 | 1.40<br>1.40 | 0.50<br>0.50 | 1.50<br>1.50 | ns<br>ns | Figs. 4, 7, 8 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$\overline{E}_a$, $\overline{E}_b$ to $Q_n$ | 0.75<br>0.75 | 2.05<br>2.05 | 0.75<br>0.75 | 1.85<br>1.85 | 0.75<br>0.75 | 2.05<br>2.05 | ns<br>ns | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>R to $Q_n$ | 0.80<br>0.80 | 2.40<br>2.40 | 0.90<br>0.90 | 2.40<br>2.40 | 0.90<br>0.90 | 2.60<br>2.60 | ns<br>ns | Figs. 5, 7, 8 |
| $t_{TLH}$<br>$t_{THL}$ | Transition time<br>20% to 80%, 80% to 20% | 0.45<br>0.45 | 1.50<br>1.50 | 0.45<br>0.45 | 1.50<br>1.50 | 0.45<br>0.45 | 1.50<br>1.50 | ns<br>ns | Figs. 4, 7, 8 |
| $t_s$ | Setup time<br>$D_n$ to $\overline{E}_n$ | 0.70<br>0.70 | | 0.70<br>0.70 | | 0.70<br>0.70 | | ns<br>ns | Figs. 6, 8 |
| $t_h$ | Hold time<br>$D_n$ to $\overline{E}_n$ | 0.70<br>0.70 | | 0.70<br>0.70 | | 0.70<br>0.70 | | ns<br>ns | |
| $t_r$ | Release time<br>R to $\overline{E}_n$ | 2.10<br>2.10 | | 2.10<br>2.10 | | 2.10<br>2.10 | | ns<br>ns | Figs. 5, 8 |
| $t_{PW(L)}$ | Pulse width<br>$\overline{E}_a$, $\overline{E}_b$ | 2.50<br>2.50 | | 2.50<br>2.50 | | 2.50<br>2.50 | | ns<br>ns | Figs. 4, 8 |
| $t_{PW(H)}$ | Pulse width<br>$\overline{E}_a$, $\overline{E}_b$ | 2.50<br>2.50 | | 2.50<br>2.50 | | 2.50<br>2.50 | | ns<br>ns | Figs. 4, 8 |

## AC ELECTRICAL CHARACTERISTICS

**Ceramic DIP** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V \pm 5\%$

| | PARAMETER | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 0.45 | 1.50 | 0.50 | 1.40 | 0.50 | 1.50 | ns | Figs. 4, 7, 8 |
| $t_{PHL}$ | $D_n$ to $Q_n$ | 0.45 | 1.50 | 0.50 | 1.40 | 0.50 | 1.50 | ns | |
| $t_{PLH}$ | Propagation delay | 0.75 | 2.05 | 0.75 | 1.85 | 0.75 | 2.05 | ns | |
| $t_{PHL}$ | $\overline{E}_a$, $\overline{E}_b$ to $Q_n$ | 0.75 | 2.05 | 0.75 | 1.85 | 0.75 | 2.05 | ns | |
| $t_{PLH}$ | Propagation delay | 0.80 | 2.40 | 0.90 | 2.40 | 0.90 | 2.60 | ns | Figs. 5, 7, 8 |
| $t_{PHL}$ | R to $Q_n$ | 0.80 | 2.40 | 0.90 | 2.40 | 0.90 | 2.60 | ns | |
| $t_{TLH}$ | Transition time | 0.45 | 1.50 | 0.45 | 1.50 | 0.45 | 1.50 | ns | Figs. 4, 7, 8 |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.50 | 0.45 | 1.50 | 0.45 | 1.50 | ns | |
| $t_s$ | Setup time | 0.70 | | 0.70 | | 0.70 | | ns | Figs. 6, 8 |
| | $D_n$ to $\overline{E}_n$ | 0.70 | | 0.70 | | 0.70 | | ns | |
| $t_h$ | Hold time | 0.70 | | 0.70 | | 0.70 | | ns | |
| | $D_n$ to $\overline{E}_n$ | 0.70 | | 0.70 | | 0.70 | | ns | |
| $t_r$ | Release time | 2.10 | | 2.10 | | 2.10 | | ns | Figs. 5, 8 |
| | R to $\overline{E}_n$ | 2.10 | | 2.10 | | 2.10 | | ns | |
| $t_{PW(L)}$ | Pulse width | 2.50 | | 2.50 | | 2.50 | | ns | Figs. 4, 8 |
| | $\overline{E}_a$, $\overline{E}_b$ | 2.50 | | 2.50 | | 2.50 | | ns | |
| $t_{PW(H)}$ | Pulse width | 2.50 | | 2.50 | | 2.50 | | ns | Figs. 4, 8 |
| | $\overline{E}_a$, $\overline{E}_b$ | 2.50 | | 2.50 | | 2.50 | | ns | |

**Flat Pack** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$

| | PARAMETER | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 0.45 | 1.30 | 0.50 | 1.20 | 0.50 | 1.30 | ns | Figs. 4, 7, 8 |
| $t_{PHL}$ | $D_n$ to $Q_n$ | 0.45 | 1.30 | 0.50 | 1.20 | 0.50 | 1.30 | ns | |
| $t_{PLH}$ | Propagation delay | 0.75 | 1.85 | 0.75 | 1.65 | 0.75 | 1.85 | ns | |
| $t_{PHL}$ | $\overline{E}_a$, $\overline{E}_b$ to $Q_n$ | 0.75 | 1.85 | 0.75 | 1.65 | 0.75 | 1.85 | ns | |
| $t_{PLH}$ | Propagation delay | 0.80 | 2.20 | 0.90 | 2.20 | 0.90 | 2.40 | ns | Figs. 5, 7, 8 |
| $t_{PHL}$ | R to $Q_n$ | 0.80 | 2.20 | 0.90 | 2.20 | 0.90 | 2.40 | ns | |
| $t_{TLH}$ | Transition time | 0.45 | 1.50 | 0.45 | 1.50 | 0.45 | 1.50 | ns | Figs. 4, 7, 8 |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.50 | 0.45 | 1.50 | 0.45 | 1.50 | ns | |
| $t_s$ | Setup time | 0.60 | | 0.60 | | 0.60 | | ns | Figs. 6, 8 |
| | $D_n$ to $\overline{E}_n$ | 0.60 | | 0.60 | | 0.60 | | ns | |
| $t_h$ | Hold time | 0.60 | | 0.60 | | 0.60 | | ns | |
| | $D_n$ to $\overline{E}_n$ | 0.60 | | 0.60 | | 0.60 | | ns | |
| $t_r$ | Release time | 2.00 | | 2.00 | | 2.00 | | ns | Figs. 5, 8 |
| | R to $\overline{E}_n$ | 2.00 | | 2.00 | | 2.00 | | ns | |
| $t_{PW(L)}$ | Pulse width | 2.50 | | 2.50 | | 2.50 | | ns | Figs. 4, 8 |
| | $\overline{E}_a$, $\overline{E}_b$ | 2.50 | | 2.50 | | 2.50 | | ns | |
| $t_{PW(H)}$ | Pulse width | 2.50 | | 2.50 | | 2.50 | | ns | Figs. 4, 8 |
| | $\overline{E}_a$, $\overline{E}_b$ | 2.50 | | 2.50 | | 2.50 | | ns | |

## AC ELECTRICAL CHARACTERISTICS

**Flat Pack** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -4.2V \pm 5\%$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 0.45 | 1.30 | 0.50 | 1.20 | 0.50 | 1.30 | ns | Figs. 4, 7, 8 |
| $t_{PHL}$ | $D_n$ to $Q_n$ | 0.45 | 1.30 | 0.50 | 1.20 | 0.50 | 1.30 | ns | |
| $t_{PLH}$ | Propagation delay | 0.75 | 1.85 | 0.75 | 1.65 | 0.75 | 1.85 | ns | |
| $t_{PHL}$ | $\overline{E}_a$, $\overline{E}_b$ to $Q_n$ | 0.75 | 1.85 | 0.75 | 1.65 | 0.75 | 1.85 | ns | |
| $t_{PLH}$ | Propagation delay | 0.80 | 2.20 | 0.90 | 2.20 | 0.90 | 2.40 | ns | Figs. 5, 7, 8 |
| $t_{PHL}$ | R to $Q_n$ | 0.80 | 2.20 | 0.90 | 2.20 | 0.90 | 2.40 | ns | |
| $t_{TLH}$ | Transition time | 0.45 | 1.50 | 0.45 | 1.50 | 0.45 | 1.50 | ns | Figs. 4, 7, 8 |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.50 | 0.45 | 1.50 | 0.45 | 1.50 | ns | |
| $t_s$ | Setup time | 0.60 | | 0.60 | | 0.60 | | ns | Figs. 6, 8 |
| | $D_n$ to $\overline{E}_n$ | 0.60 | | 0.60 | | 0.60 | | ns | |
| $t_h$ | Hold time | 0.60 | | 0.60 | | 0.60 | | ns | |
| | $D_n$ to $\overline{E}_n$ | 0.60 | | 0.60 | | 0.60 | | ns | |
| $t_r$ | Release time | 2.00 | | 2.00 | | 2.00 | | ns | Figs. 5, 8 |
| | R to $\overline{E}_n$ | 2.00 | | 2.00 | | 2.00 | | ns | |
| $t_{PW(L)}$ | Pulse width | 2.50 | | 2.50 | | 2.50 | | ns | Figs. 4, 8 |
| | $\overline{E}_a$, $\overline{E}_b$ | 2.50 | | 2.50 | | 2.50 | | ns | |
| $t_{PW(H)}$ | Pulse width | 2.50 | | 2.50 | | 2.50 | | ns | Figs. 4, 8 |
| | $\overline{E}_a$, $\overline{E}_b$ | 2.50 | | 2.50 | | 2.50 | | ns | |

## AC WAVEFORMS

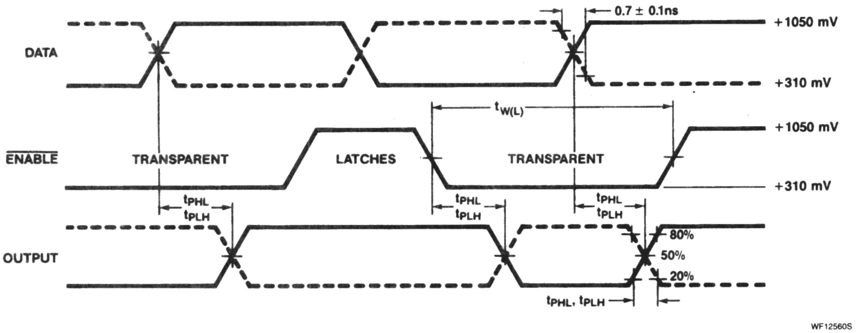

0.7 ± 0.1ns
+1050 mV
DATA
+310 mV
$t_{W(L)}$
+1050 mV
ENABLE
TRANSPARENT
LATCHES
TRANSPARENT
+310 mV
$t_{PHL}$
$t_{PLH}$
$t_{PHL}$
$t_{PLH}$
$t_{PHL}$
$t_{PLH}$
80%
OUTPUT
50%
20%
$t_{PHL}$, $t_{PLH}$
WF12560S

Figure 4. Enable Timing

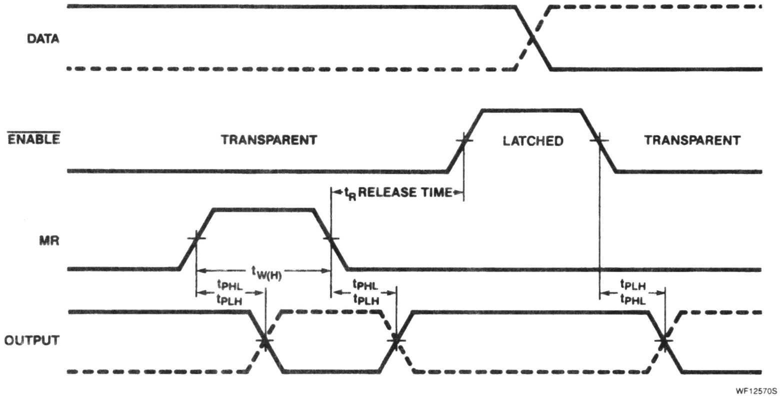

DATA
ENABLE
TRANSPARENT
LATCHED
TRANSPARENT
$t_R$ RELEASE TIME
MR
$t_{W(H)}$
$t_{PHL}$
$t_{PLH}$
$t_{PHL}$
$t_{PLH}$
$t_{PLH}$
$t_{PHL}$
OUTPUT
WF12570S

Figure 5. Reset Timing

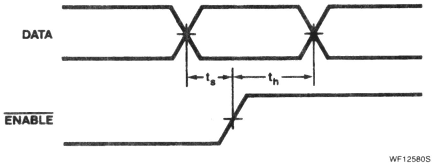
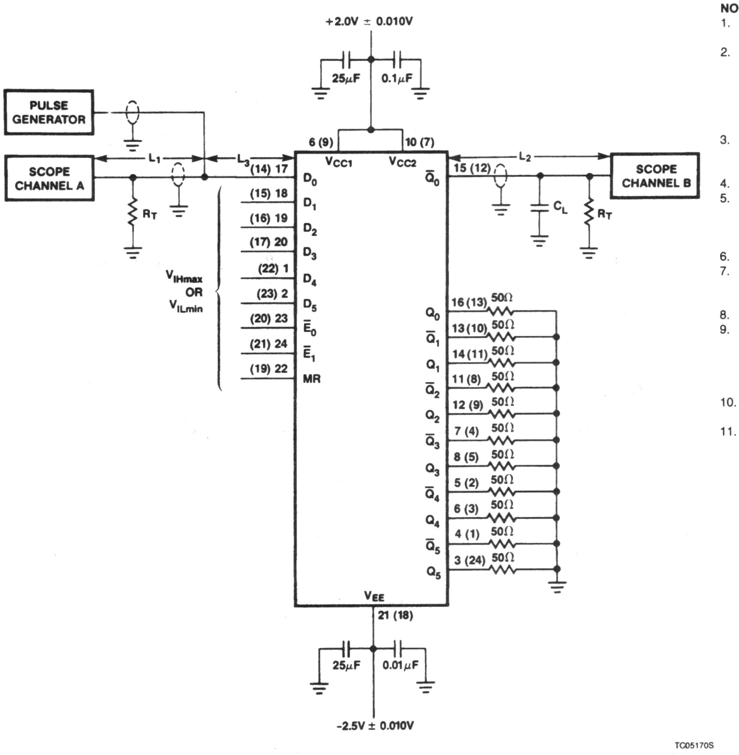

DATA
$t_s$
$t_h$
ENABLE
WF12580S

Figure 6. Data Setup and Hold Time

# Latch

# 100150

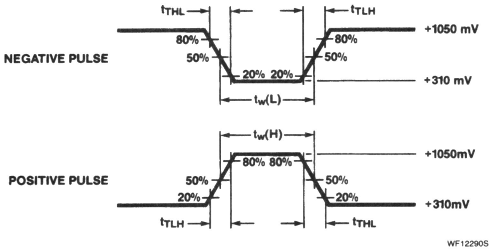
## TEST CIRCUITS AND WAVEFORMS


+2.0V ± 0.010V
25μF
0.1μF
PULSE GENERATOR
SCOPE CHANNEL A
L1
L3
RT
6 (9)
10 (7)
VCC1
VCC2
(14) 17
(15) 18
(16) 19
(17) 20
(22) 1
(23) 2
(20) 23
(21) 24
(19) 22
D0
D1
D2
D3
D4
D5
E̅0
E̅1
MR
VIHmax OR VILmin
15 (12)
Q̅0
L2
SCOPE CHANNEL B
CL
RT
16 (13)
13 (10)
14 (11)
11 (8)
12 (9)
7 (4)
8 (5)
5 (2)
6 (3)
4 (1)
3 (24)
50Ω
Q0
Q̅1
Q1
Q̅2
Q2
Q̅3
Q3
Q̅4
Q4
Q̅5
Q5
VEE
21 (18)
25μF
0.01μF
-2.5V ± 0.010V
TC05170S

NOTES:

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1μF and 25μF from GND to $V_{CC}$, 0.01μF and 25μF from GND to $V_{EE}$. (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance ≤ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.
11. Pin connections are for Flat Pack and in parentheses for Ceramic DIP.

Figure 7. Test Circuit


NEGATIVE PULSE
tTHL
tTLH
80%
50%
20% 20%
tw(L)
+1050 mV
+310 mV
POSITIVE PULSE
tw(H)
80% 80%
50%
20%
+1050mV
+310mV
WF12290S

| INPUT PULSE REQUIREMENTS<br>$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -2.5V \pm 0.010V$, $V_T$ = GND (0V) | | | | | |
|---|---|---|---|---|---|
| Family | Amplitude | Rep Rate | Pulse Width | $t_{TLH}$ | $t_{THL}$ |
| 100K ECL | 740mVp-p | 1MHz | 500ns | 0.7 ±0.1ns | 0.7 ±0.1ns |

Figure 8. Input Pulse Definition

**Signetics**

# 100151
## Flip-Flop

**Hex D-Type Master-Slave Flip-Flop**
***Product Specification***

**ECL Products**

### DESCRIPTION

The 100151 contains six flip-flops with complement and data outputs, a master reset (MR) and a pair of common clock inputs. Data enter the flip-flop on the LOW-to-HIGH transition of one of two clock inputs.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 100151 | 1.7ns | 137mA |

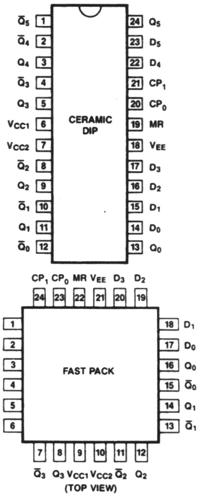
### ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} = \text{GND}$; $V_{EE} = -4.2V$ to $-4.8V$<br>$T_A = 0°C$ to $+85°C$ |
|---|---|
| Ceramic DIP | 100151F |
| Ceramic Flat Pack | 100151Y |

### PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_0 - D_4$ | Data Inputs |
| $CP_a$, $CP_b$ | Common Clock Inputs |
| MR | Master Reset Input |
| $Q_0 - Q_4$ | Data Outputs |
| $\overline{Q}_0 - \overline{Q}_4$ | Complementary Data Outputs |

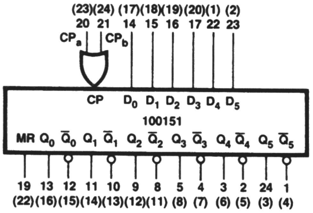
### PIN CONFIGURATION


$\overline{Q}_5$ 1
$\overline{Q}_4$ 2
$Q_4$ 3
$\overline{Q}_3$ 4
$Q_3$ 5
$V_{CC1}$ 6
$V_{CC2}$ 7
$\overline{Q}_2$ 8
$Q_2$ 9
$\overline{Q}_1$ 10
$Q_1$ 11
$\overline{Q}_0$ 12
24 $Q_5$
23 $D_5$
22 $D_4$
21 $CP_1$
20 $CP_0$
19 MR
18 $V_{EE}$
17 $D_3$
16 $D_2$
15 $D_1$
14 $D_0$
13 $Q_0$
CERAMIC DIP
$CP_1$ $CP_0$ MR $V_{EE}$ $D_3$ $D_2$
24 23 22 21 20 19
$D_4$ 1
$D_5$ 2
$Q_5$ 3
$\overline{Q}_5$ 4
$\overline{Q}_4$ 5
$Q_4$ 6
18 $D_1$
17 $D_0$
16 $Q_0$
15 $\overline{Q}_0$
14 $Q_1$
13 $\overline{Q}_1$
FAST PACK
7 8 9 10 11 12
$\overline{Q}_3$ $Q_3$ $V_{CC1}$ $V_{CC2}$ $\overline{Q}_2$ $Q_2$
(TOP VIEW)

CD09320S

Figure 1

### LOGIC SYMBOL


(23)(24) (17)(18)(19)(20)(1) (2)
20 21 14 15 16 17 22 23
$CP_a$ $CP_b$
CP $D_0$ $D_1$ $D_2$ $D_3$ $D_4$ $D_5$
100151
MR $Q_0$ $\overline{Q}_0$ $Q_1$ $\overline{Q}_1$ $Q_2$ $\overline{Q}_2$ $Q_3$ $\overline{Q}_3$ $Q_4$ $\overline{Q}_4$ $Q_5$ $\overline{Q}_5$
19 13 12 11 10 9 8 5 4 3 2 24 1
(22)(16)(15)(14)(13)(12)(11) (8) (7) (6) (5) (3) (4)

$V_{CC1}$ = Pin 6 (9)
$V_{CC2}$ = Pin 7 (10)
$V_{EE}$ = Pin 18 (21)

LS10760S

Figure 2

## Flip-Flop

## 100151

### LOGIC DIAGRAM

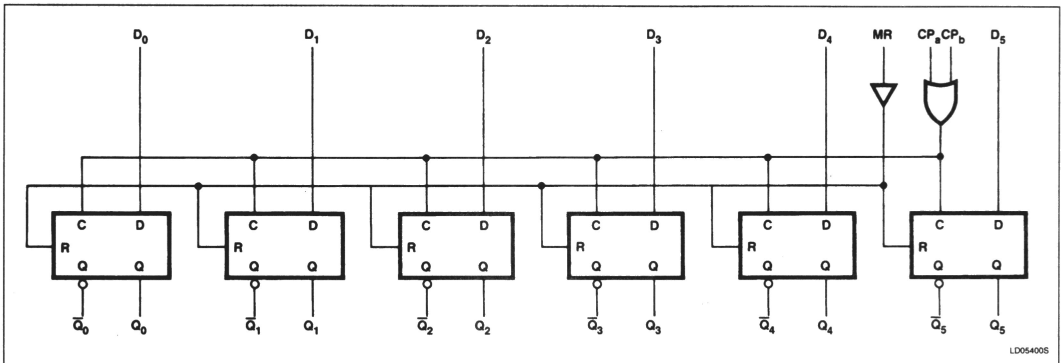

D$_0$
D$_1$
D$_2$
D$_3$
D$_4$
MR
CP$_a$CP$_b$
D$_5$
C
D
R
Q
$\overline{Q}_0$
Q$_0$
$\overline{Q}_1$
Q$_1$
$\overline{Q}_2$
Q$_2$
$\overline{Q}_3$
Q$_3$
$\overline{Q}_4$
Q$_4$
$\overline{Q}_5$
Q$_5$
LD05400S

Figure 3

### FUNCTION TABLE

| INPUTS | | | | OUTPUTS | |
|---|---|---|---|---|---|
| D | CP$_a$ | CP$_b$ | R | $\overline{Q}$ | Q |
| H | L | ↑ | L | L | H |
| L | L | ↑ | L | H | L |
| H | ↑ | L | L | L | H |
| L | ↑ | L | L | H | L |
| X | X | H | L | No change | |
| X | H | X | L | No change | |
| X | X | X | H | H | L |
| X | L | L | L | No change | |

Positive Logic:
H = HIGH state (more positive voltage) = 1
L = LOW state (less positive voltage) = 0
X = Don't Care
↑ = LOW-to-HIGH transition.

## ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | 100K ECL | UNIT |
|---|---|---|---|
| $V_{EE}$ | Supply voltage ($V_{CC1}$ = $V_{CC2}$ = GND) | −7.0 to 0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | $V_{EE}$ to +0.5 | V |
| $I_O$ | Output source current | −55 | mA |
| $T_S$ | Storage temperature | −65 to +150 | °C |
| $T_J$ | Maximum junction temperature | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | | 100K ECL | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | −4.2 | −4.5 | −4.8 | V |
| $V_{EE}$ | Supply voltage (negative) when operating with 10K ECL family | | | | | −5.7 | V |
| $V_{IH}$ | HIGH level input voltage | $V_{CC1}$ = $V_{CC2}$ = GND<br>$T_A$ = 0°C to +85°C | $V_{EE}$ = −4.2V | −1150 | | −880 | mV |
| | | | $V_{EE}$ = −4.5V | −1165 | | | |
| | | | $V_{EE}$ = −4.8V | | | | |
| $V_{IHT}$ | HIGH level input threshold voltage | | $V_{EE}$ = −4.2V | −1150 | | | mV |
| | | | $V_{EE}$ = −4.5V | −1165 | | | mV |
| | | | $V_{EE}$ = −4.8V | | | | |
| $V_{ILT}$ | LOW level input threshold voltage | | $V_{EE}$ = −4.2V | | | −1475 | mV |
| | | | $V_{EE}$ = −4.5V | | | | |
| | | | $V_{EE}$ = −4.8V | | | −1490 | mV |
| $V_{IL}$ | LOW level input voltage | | $V_{EE}$ = −4.2V | −1810 | | −1475 | mV |
| | | | $V_{EE}$ = −4.5V | | | | |
| | | | $V_{EE}$ = −4.8V | | | −1490 | |
| $T_A$ | Operating ambient temperature | | | 0 | +25 | +85 | °C |

**NOTE:**
When operating at other than specified voltages (−4.2V, −4.5V, −4.8V) DC & AC Characteristics will vary slightly from specified values.

## DC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$, $T_A = 0°C$ to $+85°C$ unless otherwise specified[1, 3]

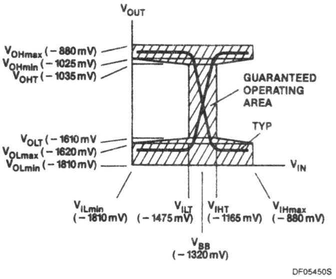
| PARAMETER | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] | |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | $V_{EE} = -4.2V$ | −1025 | | −870 | mV | $V_{IN} = V_{IHmax}$ or $V_{IN} = V_{ILmin}$ | Loading with 50Ω to −2.0V ±0.010V |
| | | $V_{EE} = -4.5V$ | −1025 | −955 | −880 | mV | | |
| | | $V_{EE} = -4.8V$ | −1035 | | −880 | mV | | |
| $V_{OHT}$ | HIGH level output threshold voltage | $V_{EE} = -4.2V$ | −1035 | | | mV | $V_{IN} = V_{IHmin}$ or $V_{IN} = V_{ILmax}$ | |
| | | $V_{EE} = -4.5V$ | −1035 | | | mV | | |
| | | $V_{EE} = -4.8V$ | −1045 | | | mV | | |
| $V_{OLT}$ | LOW level output threshold voltage | $V_{EE} = -4.2V$ | | | −1590 | mV | $V_{IN} = V_{IHmin}$ or $V_{IN} = V_{ILmax}$ | |
| | | $V_{EE} = -4.5V$ | | | −1610 | mV | | |
| | | $V_{EE} = -4.8V$ | | | −1610 | mV | | |
| $V_{OL}$ | LOW level output voltage | $V_{EE} = -4.2V$ | −1810 | | −1600 | mV | $V_{IN} = V_{IHmax}$ or $V_{IN} = V_{ILmin}$ | |
| | | $V_{EE} = -4.5V$ | −1810 | −1705 | −1620 | mV | | |
| | | $V_{EE} = -4.8V$ | −1830 | | −1620 | mV | | |
| $I_{IH}$ | HIGH level input current | R | | | 450 | μA | $V_{IN} = V_{IHmax}$ | |
| | | $D_n$ | | | 225 | μA | | |
| | | $CP_a$, $CP_b$ | | | 520 | μA | | |
| $I_{IL}$ | LOW level input current | | 0.5 | | | μA | $V_{IN} = V_{ILmin}$ | |
| $-I_{EE}$ | $V_{EE}$ supply current | | 98 | 137 | 210 | mA | Inputs open | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | $V_{EE} = -4.2V$<br>$T_A = +25°C$ | | | 0.035 | V/V | | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | | 0.070 | V/V | | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 4.

## Flip-Flop

## 100151



**NOTES:**

$V_{IHmax}$ – Maximum HIGH level input voltage (the most positive $V_{IH}$).
$V_{IHT}$ – HIGH level input threshold voltage.
$V_{ILT}$ – LOW level input threshold voltage.
$V_{ILmin}$ – Minimum LOW level input voltage (the most negative $V_{IL}$).
$V_{OHmax}$ – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition.
$V_{OHmin}$ – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition.
$V_{OHT}$ – HIGH level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLT}$ – LOW level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLmax}$ – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions.
$V_{OLmin}$ -- Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions.
$V_{BB}$ – Reference bias voltage. The internally generated reference voltage which is used to set the input and output threshold level.

**Figure 4. Transfer Characteristics**

## AC ELECTRICAL CHARACTERISTICS

**Ceramic DIP** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $f_{max}$ | Toggle frequency | 375 | | 375 | | 375 | | MHz | Figs. 4, 8, 9 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$CP_a$, $CP_b$ to $Q_n$ | 0.80<br>0.80 | 2.20<br>2.20 | 0.80<br>0.80 | 2.20<br>2.20 | 0.90<br>0.90 | 2.40<br>2.40 | ns<br>ns | Figs. 4, 7, 9 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>MR to $Q_n$ | 1.20<br>1.20 | 2.90<br>2.90 | 1.30<br>1.30 | 3.00<br>3.00 | 1.20<br>1.20 | 3.10<br>3.10 | ns<br>ns | Figs. 4, 7, 9 |
| $t_{TLH}$<br>$t_{THL}$ | Transition time<br>20% to 80%, 80% to 20% | 0.45<br>0.45 | 1.70<br>1.70 | 0.45<br>0.45 | 1.60<br>1.60 | 0.45<br>0.45 | 1.70<br>1.70 | ns<br>ns | Figs. 4, 7, 9 |
| $t_s$ | Setup time<br>$D_n$ to $CP_n$ | 0.95 | | 0.90 | | 0.95 | | ns | Figs. 6, 9 |
| $t_h$ | Hold time<br>$D_n$ to $CP_n$ | 0.70 | | 0.70 | | 0.70 | | ns | |
| $t_r$ | Release time<br>MR to $CP_n$ | 2.30 | | 2.30 | | 2.30 | | ns | Figs. 5, 9 |
| $t_w(H)$ | Pulse width<br>$CP_a$, $CP_b$, MR | 2.50 | | 2.50 | | 2.50 | | ns | Figs. 4, 5, 9 |

## AC ELECTRICAL CHARACTERISTICS

**Ceramic DIP** $V_{CC1} = V_{CC2} = \text{GND}$, $V_{EE} = -5.2V \pm 5\%$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $f_{max}$ | Toggle frequency | 375 | | 375 | | 375 | | MHz | Figs. 5, 9, 10 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$CP_a$, $CP_b$ to $Q_n$ | 0.80<br>0.80 | 2.20<br>2.20 | 0.80<br>0.80 | 2.20<br>2.20 | 0.90<br>0.90 | 2.40<br>2.40 | ns<br>ns | Figs. 5, 8, 10 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>MR to $Q_n$ | 1.20<br>1.20 | 2.90<br>2.90 | 1.30<br>1.30 | 3.00<br>3.00 | 1.20<br>1.20 | 3.10<br>3.10 | ns<br>ns | Figs. 5, 8, 10 |
| $t_{TLH}$<br>$t_{THL}$ | Transition time<br>20% to 80%, 80% to 20% | 0.45<br>0.45 | 1.70<br>1.70 | 0.45<br>0.45 | 1.60<br>1.60 | 0.45<br>0.45 | 1.70<br>1.70 | ns<br>ns | Figs. 5, 8, 10 |
| $t_s$ | Setup time<br>$D_n$ to $CP_n$ | 0.95 | | 0.90 | | 0.95 | | ns | Figs. 7, 10 |
| $t_h$ | Hold time<br>$D_n$ to $CP_n$ | 0.70 | | 0.70 | | 0.70 | | ns | |
| $t_r$ | Release time<br>MR to $CP_n$ | 2.30 | | 2.30 | | 2.30 | | ns | Figs. 6, 10 |
| $t_w(H)$ | Pulse width<br>$CP_a$, $CP_b$, MR | 2.50 | | 2.50 | | 2.50 | | ns | Figs. 5, 6, 10 |

**Flat Pack** $V_{CC1} = V_{CC2} = \text{GND}$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $f_{max}$ | Toggle frequency | 375 | | 375 | | 375 | | MHz | Figs. 5, 7, 10 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$CP_a$, $CP_b$ to $Q_n$ | 0.80<br>0.80 | 2.00<br>2.00 | 0.80<br>0.80 | 2.00<br>2.00 | 0.90<br>0.90 | 2.20<br>2.20 | ns<br>ns | Figs. 5, 8, 10 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>MR to $Q_n$ | 1.20<br>1.20 | 2.70<br>2.70 | 1.30<br>1.30 | 2.80<br>2.80 | 1.20<br>1.20 | 2.90<br>2.90 | ns<br>ns | Figs. 5, 8, 10 |
| $t_{TLH}$<br>$t_{THL}$ | Transition time<br>20% to 80%, 80% to 20% | 0.45<br>0.45 | 1.70<br>1.70 | 0.45<br>0.45 | 1.60<br>1.60 | 0.45<br>0.45 | 1.70<br>1.70 | ns<br>ns | Figs. 5, 8, 10 |
| $t_s$ | Setup time<br>$D_n$ to $CP_n$ | 0.75 | | 0.70 | | 0.75 | | ns | Figs. 7, 10 |
| $t_h$ | Hold time<br>$D_n$ to $CP_n$ | 0.60 | | 0.60 | | 0.60 | | ns | |
| $t_r$ | Release time<br>MR to $CP_n$ | 2.20 | | 2.20 | | 2.50 | | ns | Figs. 6, 10 |
| $t_w(H)$ | Pulse width<br>$CP_a$, $CP_b$, MR | 2.50 | | 2.50 | | 2.50 | | ns | Figs. 5, 6, 10 |

## Flip-Flop 100151

### AC ELECTRICAL CHARACTERISTICS

**Flat Pack** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V \pm 5\%$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $f_{max}$ | Toggle frequency | 375 | | 375 | | 375 | | MHz | Figs. 5, 9, 10 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$CP_a$, $CP_b$ to $Q_n$ | 0.80<br>0.80 | 2.00<br>2.00 | 0.80<br>0.80 | 2.00<br>2.00 | 0.90<br>0.90 | 2.20<br>2.20 | ns<br>ns | Figs. 5, 8, 10 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>MR to $Q_n$ | 1.20<br>1.20 | 2.70<br>2.70 | 1.30<br>1.30 | 2.80<br>2.80 | 1.20<br>1.20 | 2.90<br>2.90 | ns<br>ns | Figs. 5, 8, 10 |
| $t_{TLH}$<br>$t_{THL}$ | Transition time<br>20% to 80%, 80% to 20% | 0.45<br>0.45 | 1.70<br>1.70 | 0.45<br>0.45 | 1.60<br>1.60 | 0.45<br>0.45 | 1.70<br>1.70 | ns<br>ns | Figs. 5, 8, 10 |
| $t_s$ | Setup time<br>$D_n$ to $CP_n$ | 0.75 | | 0.70 | | 0.75 | | ns | Figs. 7, 10 |
| $t_h$ | Hold time<br>$D_n$ to $CP_n$ | 0.60 | | 0.60 | | 0.60 | | ns | |
| $t_r$ | Release time<br>MR to $CP_n$ | 2.20 | | 2.20 | | 2.50 | | ns | Figs. 6, 10 |
| $t_w(H)$ | Pulse width<br>$CP_a$, $CP_b$, MR | 2.50 | | 2.50 | | 2.50 | | ns | Figs. 5, 6, 10 |

## AC WAVEFORMS

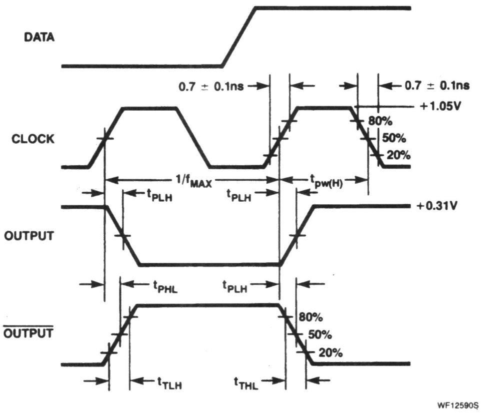

DATA
0.7 ± 0.1ns
0.7 ± 0.1ns
+1.05V
CLOCK
80%
50%
20%
1/fMAX
tpw(H)
tPLH
tPLH
+0.31V
OUTPUT
tPHL
tPLH
OUTPUT
80%
50%
20%
tTLH
tTHL
WF12590S

Figure 5. Propagation Delay for Clock to Outputs and Transition Time

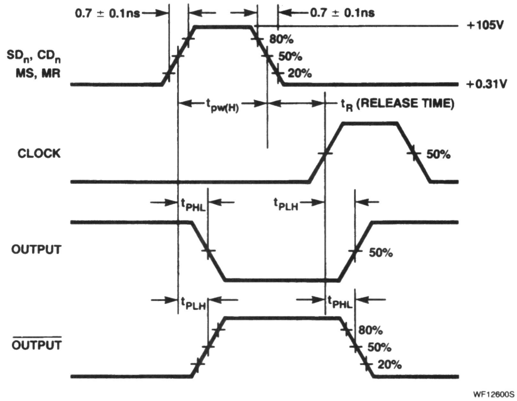

0.7 ± 0.1ns
0.7 ± 0.1ns
+105V
SDn, CDn
MS, MR
80%
50%
20%
+0.31V
tpw(H)
tR (RELEASE TIME)
CLOCK
50%
tPHL
tPLH
OUTPUT
50%
tPLH
tPHL
OUTPUT
80%
50%
20%
WF12600S

Figure 6. Propagation Delay for Sets and Resets to Outputs

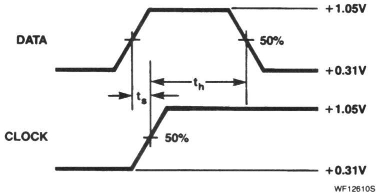
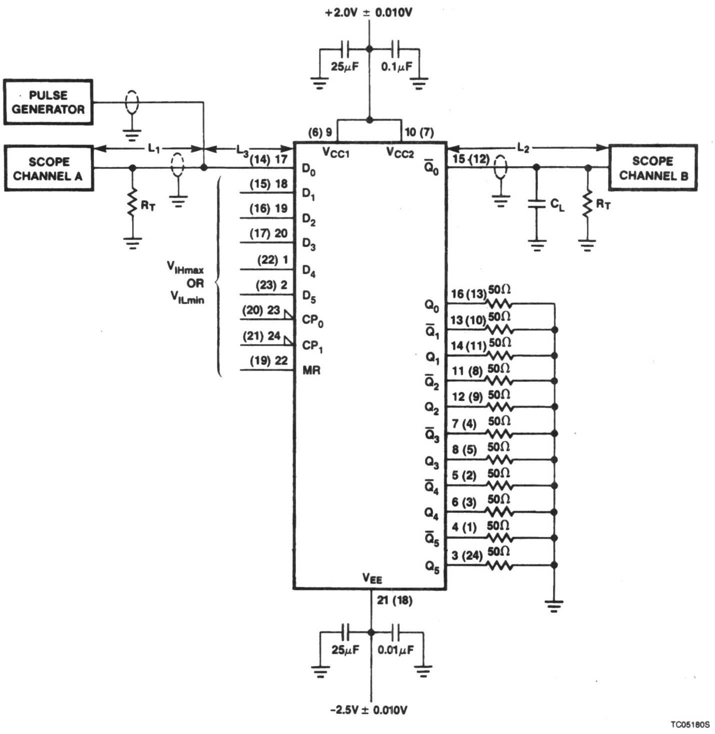

+1.05V
DATA
50%
+0.31V
th
ts
+1.05V
CLOCK
50%
+0.31V
WF12610S

Figure 7. Data Setup and Hold Time

## TEST CIRCUITS AND WAVEFORMS


+2.0V ± 0.010V
25µF
0.1µF
PULSE GENERATOR
SCOPE CHANNEL A
L1
L3
R_T
(6) 9
10 (7)
VCC1
VCC2
(14) 17
(15) 18
(16) 19
(17) 20
(22) 1
(23) 2
(20) 23
(21) 24
(19) 22
D0
D1
D2
D3
D4
D5
CP0
CP1
MR
VIHmax OR VILmin
Q̄0
15 (12)
L2
SCOPE CHANNEL B
CL
RT
Q0
Q̄1
Q1
Q̄2
Q2
Q̄3
Q3
Q̄4
Q4
Q̄5
Q5
16 (13)
13 (10)
14 (11)
11 (8)
12 (9)
7 (4)
8 (5)
5 (2)
6 (3)
4 (1)
3 (24)
50Ω
VEE
21 (18)
25µF
0.01µF
-2.5V ± 0.010V
TC05180S

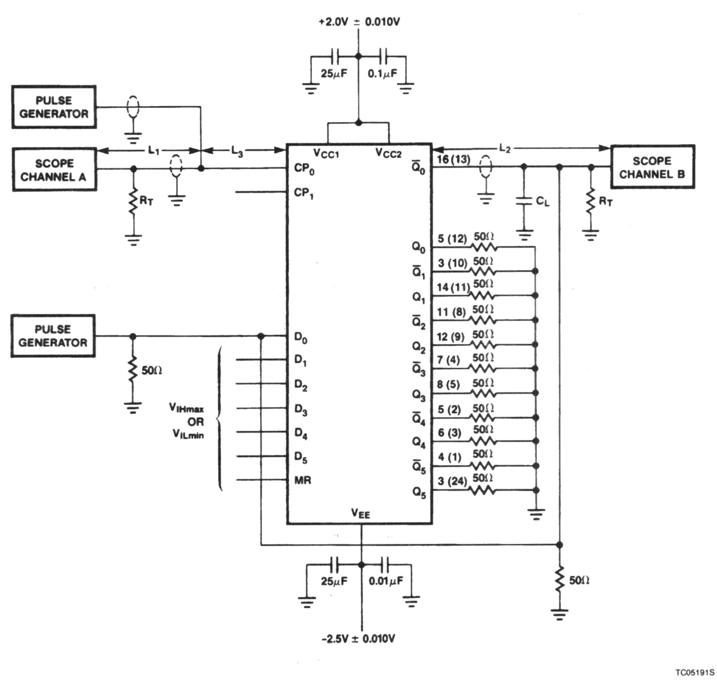
**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1µF and 25µF from GND to $V_{CC}$, 0.01µF and 25µF from GND to $V_{EE}$. (0.01 and 0.1µF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines . $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T = 50\Omega$ terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance $\leqslant$ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.
11. Pin connections are for Flat Pack and in parentheses for Ceramic DIP.

Figure 8. AC Test Circuit

# Flip-Flop

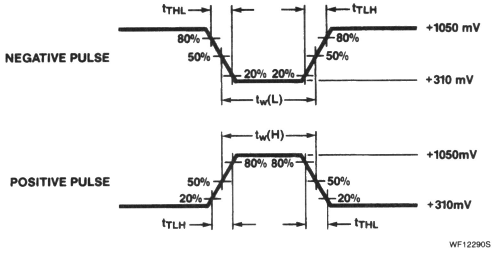
# 100151


+2.0V ± 0.010V
25μF
0.1μF
PULSE GENERATOR
SCOPE CHANNEL A
L1
L3
L2
RT
VCC1
VCC2
CP0
CP1
Q̄0
16 (13)
SCOPE CHANNEL B
CL
RT
Q0
Q̄1
Q1
Q̄2
Q2
Q̄3
Q3
Q̄4
Q4
Q̄5
Q5
5 (12)
3 (10)
14 (11)
11 (8)
12 (9)
7 (4)
8 (5)
5 (2)
6 (3)
4 (1)
3 (24)
50Ω
PULSE GENERATOR
50Ω
D0
D1
D2
D3
D4
D5
MR
VIHmax OR VILmin
VEE
25μF
0.01μF
-2.5V ± 0.010V
50Ω
TC05191S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1μF and 25μF from GND to $V_{CC}$, 0.01μF and 25μF from GND to $V_{EE}$. (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance ≤ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.
11. Pin connections are for Flat Pack and in parentheses for Ceramic DIP.

Figure 9. Toggle Frequency Test Circuit


NEGATIVE PULSE
tTHL
tTLH
80%
50%
20%
20%
80%
50%
+1050 mV
+310 mV
tw(L)
tw(H)
POSITIVE PULSE
80%
80%
50%
20%
50%
20%
+1050mV
+310mV
tTLH
tTHL
WF12290S

**INPUT PULSE REQUIREMENTS**
$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -2.5V \pm 0.010V$, $V_T$ = GND (0V)

| Family | Amplitude | Rep Rate | Pulse Width | $t_{TLH}$ | $t_{THL}$ |
|---|---|---|---|---|---|
| 100K ECL | 740mVp-p | 1MHz | 500ns | 0.7 ±0.1ns | 0.7 ±0.1ns |

Figure 10. Input Pulse Definition

**Signetics**

# 100155
## Multiplexer-Latch

**Quad 2-Way Multiplexer/Latch**
***Product Specification***

**ECL Products**

### DESCRIPTION

The 100155 has four flip-flops with complement and data outputs, a common reset, and a common clock, fed by a 2-input negative AND gate, data inputs from a 2-way multiplexer. Each multiplexer has two data inputs selected by two common address inputs ($S_0$, $S_1$). One address input is complemented, so address inputs can be tied together to form a single select input.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 100155 | 1.1ns | 93mA |

### ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC1} = V_{CC2} = GND$; $V_{EE} = -4.2V$ to $-4.8V$ $T_A = 0°C$ to $+85°C$ |
|---|---|
| Ceramic DIP | 100155F |
| Ceramic Flat Pack | 100155Y |

### PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_0 - D_7$ | Data Inputs |
| $\overline{E}_0$, $\overline{E}_1$ | Enable Inputs |
| $\overline{S}_0$, $S_1$ | Select Inputs |
| MR | Master Reset Input |
| $Q_0 - Q_3$ | Data Outputs |
| $\overline{Q}_0 - \overline{Q}_3$ | Complementary Data Outputs |

### PIN CONFIGURATION

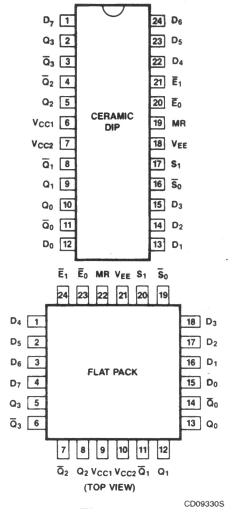

D7 1
Q3 2
Q̄3 3
Q̄2 4
Q2 5
VCC1 6
VCC2 7
Q̄1 8
Q1 9
Q0 10
Q̄0 11
D0 12
24 D6
23 D5
22 D4
21 Ē1
20 Ē0
19 MR
18 VEE
17 S1
16 S̄0
15 D3
14 D2
13 D1
CERAMIC DIP
Ē1 Ē0 MR VEE S1 S̄0
24 23 22 21 20 19
D4 1
D5 2
D6 3
D7 4
Q3 5
Q̄3 6
18 D3
17 D2
16 D1
15 D0
14 Q̄0
13 Q0
FLAT PACK
7 8 9 10 11 12
Q̄2 Q2 VCC1 VCC2 Q̄1 Q1
(TOP VIEW)
CD09330S

Figure 1

### LOGIC SYMBOL

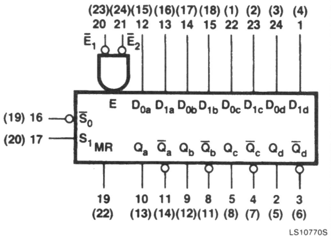

(23)(24)(15)(16)(17)(18) (1) (2) (3) (4)
20 21 12 13 14 15 22 23 24 1
Ē1 Ē2
E D0a D1a D0b D1b D0c D1c D0d D1d
(19) 16 S̄0
(20) 17 S1
MR Qa Q̄a Qb Q̄b Qc Q̄c Qd Q̄d
19 10 11 9 8 5 4 2 3
(22) (13)(14)(12)(11) (8) (7) (5) (6)
LS10770S

Figure 2

## Multiplexer-Latch

## 100155

### LOGIC DIAGRAM

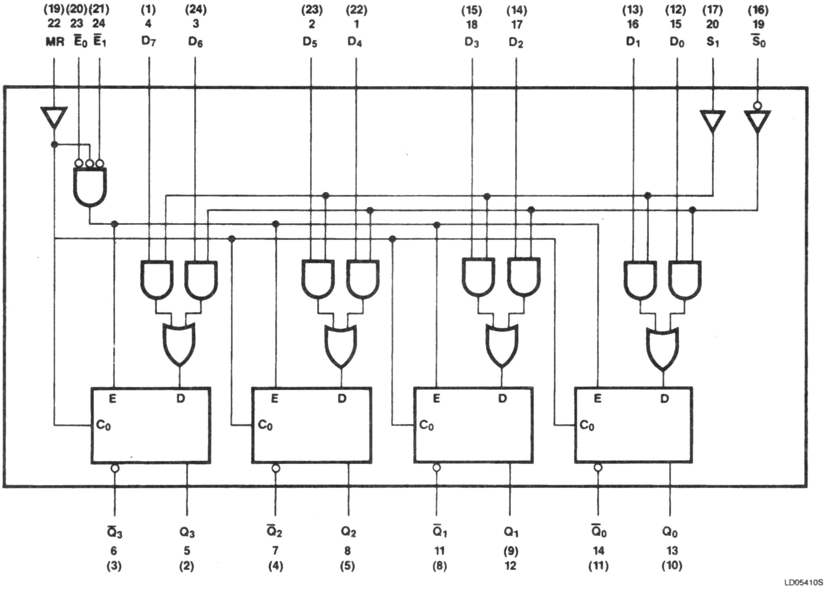

(19)(20)(21)
22 23 24
MR $\overline{E}_0$ $\overline{E}_1$
(1) 4 $D_7$
(24) 3 $D_6$
(23) 2 $D_5$
(22) 1 $D_4$
(15) 18 $D_3$
(14) 17 $D_2$
(13) 16 $D_1$
(12) 15 $D_0$
(17) 20 $S_1$
(16) 19 $\overline{S}_0$
E
D
$C_0$
$\overline{Q}_3$ 6 (3)
$Q_3$ 5 (2)
$\overline{Q}_2$ 7 (4)
$Q_2$ 8 (5)
$\overline{Q}_1$ 11 (8)
$Q_1$ (9) 12
$\overline{Q}_0$ 14 (11)
$Q_0$ 13 (10)
LD05410S

Figure 3

### FUNCTION TABLE

| INPUTS | | | | | | | OUTPUTS | |
|---|---|---|---|---|---|---|---|---|
| Reset | Enable | | Address | | Data | | $\overline{Q}$ | Q |
| H | X | X | X | X | X | X | H | L |
| L | L | L | H | H | H | X | L | H |
| L | L | L | H | H | L | X | H | L |
| L | L | L | L | L | X | H | L | H |
| L | L | L | L | L | X | L | H | L |
| L | L | L | L | H | X | X | H | L |
| L | L | L | H | L | H | X | L | H |
| L | L | L | H | L | X | H | L | H |
| L | L | L | H | L | L | L | H | L |
| L | H | X | X | X | X | X | No change | |
| L | X | H | X | X | X | X | No change | |

Positive Logic:
H = HIGH state (more positive voltage) = 1
L = LOW state (less positive voltage) = 0
X = Don't Care

# Multiplexer-Latch 100155

**ABSOLUTE MAXIMUM RATINGS** (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | 100K ECL | UNIT |
|---|---|---|---|
| $V_{EE}$ | Supply voltage ($V_{CC1} = V_{CC2}$ = GND) | −7.0 to 0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | $V_{EE}$ to +0.5 | V |
| $I_O$ | Output source current | −55 | mA |
| $T_S$ | Storage temperature | −65 to +150 | °C |
| $T_J$ | Maximum junction temperature | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | | 100K ECL | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | −4.2 | −4.5 | −4.8 | V |
| $V_{EE}$ | Supply voltage (negative) when operating with 10K ECL family | | | | | −5.7 | V |
| $V_{IH}$ | HIGH level input voltage | $V_{CC1} = V_{CC2}$ = GND<br>$T_A$ = 0°C to +85°C | $V_{EE}$ = −4.2V | −1150 | | −880 | mV |
| | | | $V_{EE}$ = −4.5V | −1165 | | | |
| | | | $V_{EE}$ = −4.8V | | | | |
| $V_{IHT}$ | HIGH level input threshold voltage | | $V_{EE}$ = −4.2V | −1150 | | | mV |
| | | | $V_{EE}$ = −4.5V | −1165 | | | mV |
| | | | $V_{EE}$ = −4.8V | | | | |
| $V_{ILT}$ | LOW level input threshold voltage | | $V_{EE}$ = −4.2V | | | −1475 | mV |
| | | | $V_{EE}$ = −4.5V | | | | |
| | | | $V_{EE}$ = −4.8V | | | −1490 | mV |
| $V_{IL}$ | LOW level input voltage | | $V_{EE}$ = −4.2V | −1810 | | −1475 | mV |
| | | | $V_{EE}$ = −4.5V | | | | |
| | | | $V_{EE}$ = −4.8V | | | −1490 | |
| $T_A$ | Operating ambient temperature | | | 0 | +25 | +85 | °C |

**NOTE:**
When operating at other than specified voltages (−4.2V, −4.5V, −4.8V) DC & AC Characteristics will vary slightly from specified values.

## Multiplexer-Latch

## 100155

**DC ELECTRICAL CHARACTERISTICS** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$, $T_A = 0°C$ to $+85°C$ unless otherwise specified[1,3]

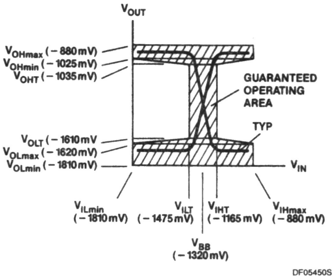
| PARAMETER | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] | |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | $V_{EE} = -4.2V$ | −1025 | | −870 | mV | $V_{IN} = V_{IHmax}$ or $V_{IN} = V_{ILmin}$ | Loading with 50Ω to −2.0V ±0.010V |
| | | $V_{EE} = -4.5V$ | −1025 | −955 | −880 | mV | | |
| | | $V_{EE} = -4.8V$ | −1035 | | −880 | mV | | |
| $V_{OHT}$ | HIGH level output threshold voltage | $V_{EE} = -4.2V$ | −1035 | | | mV | $V_{IN} = V_{IHmin}$ or $V_{IN} = V_{ILmax}$ | |
| | | $V_{EE} = -4.5V$ | −1035 | | | mV | | |
| | | $V_{EE} = -4.8V$ | −1045 | | | mV | | |
| $V_{OLT}$ | LOW level output threshold voltage | $V_{EE} = -4.2V$ | | | −1590 | mV | $V_{IN} = V_{IHmin}$ or $V_{IN} = V_{ILmax}$ | |
| | | $V_{EE} = -4.5V$ | | | −1610 | mV | | |
| | | $V_{EE} = -4.8V$ | | | −1610 | mV | | |
| $V_{OL}$ | LOW level output voltage | $V_{EE} = -4.2V$ | −1810 | | −1600 | mV | $V_{IN} = V_{IHmax}$ or $V_{IN} = V_{ILmin}$ | |
| | | $V_{EE} = -4.5V$ | −1810 | −1705 | −1620 | mV | | |
| | | $V_{EE} = -4.8V$ | −1830 | | −1620 | mV | | |
| $I_{IH}$ | HIGH level input current | $\overline{S}_0$, $S_1$ | | | 220 | µA | $V_{IN} = V_{IHmax}$ | |
| | | $\overline{E}_1$, $\overline{E}_2$ | | | 350 | µA | | |
| | | $D_n$ | | | 340 | µA | | |
| | | MR | | | 430 | µA | | |
| $I_{IL}$ | LOW level input current | | 0.5 | | | µA | $V_{IN} = V_{ILmin}$ | |
| $-I_{EE}$ | $V_{EE}$ supply current | | 66 | 93 | 133 | mA | Inputs open | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | $V_{EE} = -4.2V$<br>$T_A = +25°C$ | | | 0.035 | V/V | | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | | 0.070 | V/V | | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 4.

# Multiplexer-Latch

# 100155



**NOTES:**

| | |
|---|---|
| $V_{IHmax}$ | – Maximum HIGH level input voltage (the most positive $V_{IH}$). |
| $V_{IHT}$ | – HIGH level input threshold voltage. |
| $V_{ILT}$ | – LOW level input threshold voltage. |
| $V_{ILmin}$ | – Minimum LOW level input voltage (the most negative $V_{IL}$). |
| $V_{OHmax}$ | – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition. |
| $V_{OHmin}$ | – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition. |
| $V_{OHT}$ | – HIGH level output threshold voltage with the inputs set to their respective threshold levels. |
| $V_{OLT}$ | – LOW level output threshold voltage with the inputs set to their respective threshold levels. |
| $V_{OLmax}$ | – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions. |
| $V_{OLmin}$ | – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions. |
| $V_{BB}$ | – Reference bias voltage. The internally generated reference voltage which is used to set the input and output threshold level. |

**Figure 4. Transfer Characteristics**

## AC ELECTRICAL CHARACTERISTICS

**Ceramic DIP** $V_{CC1} = V_{CC2} =$ GND, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 0.50 | 1.90 | 0.60 | 1.85 | 0.50 | 1.90 | ns | Figs. 5, 8, 9 |
| $t_{PHL}$ | $D_n$ to $Q_n$ | 0.50 | 1.90 | 0.60 | 1.85 | 0.50 | 1.90 | ns | |
| $t_{PLH}$ | Propagation delay | 1.50 | 3.50 | 1.50 | 3.40 | 1.50 | 3.50 | ns | |
| $t_{PHL}$ | $\overline{S}_0$, $S_1$ to $Q_n$ | 1.50 | 3.50 | 1.50 | 3.40 | 1.50 | 3.50 | ns | |
| $t_{PLH}$ | Propagation delay | 0.90 | 2.50 | 1.00 | 2.40 | 1.00 | 2.50 | ns | |
| $t_{PHL}$ | $\overline{E}_0$, $\overline{E}_1$ to $Q_n$ | 0.90 | 2.50 | 1.00 | 2.40 | 1.00 | 2.50 | ns | |
| $t_{PLH}$ | Propagation delay | 0.90 | 3.00 | 0.90 | 2.90 | 0.90 | 3.00 | ns | Figs. 6, 8, 9 |
| $t_{PHL}$ | MR to $Q_n$ | 0.90 | 3.00 | 0.90 | 2.90 | 0.90 | 3.00 | ns | |
| $t_{TLH}$ | Transition time | 0.60 | 2.20 | 0.60 | 2.10 | 0.45 | 2.20 | ns | Figs. 5, 8, 9 |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.60 | 2.20 | 0.60 | 2.10 | 0.45 | 2.20 | ns | |
| $t_s$ | Setup time $D_n$ to $\overline{E}_n$ | 0.90 | | 0.90 | | 0.90 | | ns | Figs. 7, 9 |
| $t_h$ | Hold time $D_n$ to $\overline{E}_n$ | 0.40 | | 0.40 | | 0.40 | | ns | |
| $t_s$ | Setup time $S_0$, $S_1$ to $D_n$ | 2.40 | | 2.40 | | 2.70 | | ns | |
| $t_h$ | Hold time $S_0$, $S_1$ to $D_n$ | −0.6 | | −0.6 | | −0.6 | | ns | |
| $t_r$ | Release time MR to $\overline{E}_n$ | 1.50 | | 1.50 | | 1.50 | | ns | Figs. 6, 9 |
| $t_w(H)$ | Pulse width MR | 2.50 | | 2.50 | | 2.50 | | ns | Figs. 6, 9 |
| $t_w(L)$ | Pulse width $\overline{E}_0$, $\overline{E}_1$ | 2.50 | | 2.50 | | 2.50 | | ns | Figs. 5, 9 |

# Multiplexer-Latch

# 100155

## AC ELECTRICAL CHARACTERISTICS

**Ceramic DIP** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V \pm 5\%$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 0.50 | 1.90 | 0.60 | 1.85 | 0.50 | 1.90 | ns | Figs. 5, 8, 9 |
| $t_{PHL}$ | $D_n$ to $Q_n$ | 0.50 | 1.90 | 0.60 | 1.85 | 0.50 | 1.90 | ns | |
| $t_{PLH}$ | Propagation delay | 1.50 | 3.50 | 1.50 | 3.40 | 1.50 | 3.50 | ns | |
| $t_{PHL}$ | $\overline{S}_0$, $S_1$ to $Q_n$ | 1.50 | 3.50 | 1.50 | 3.40 | 1.50 | 3.50 | ns | |
| $t_{PLH}$ | Propagation delay | 0.90 | 2.50 | 1.00 | 2.40 | 1.00 | 2.50 | ns | |
| $t_{PHL}$ | $\overline{E}_0$, $\overline{E}_1$ to $Q_n$ | 0.90 | 2.50 | 1.00 | 2.40 | 1.00 | 2.50 | ns | |
| $t_{PLH}$ | Propagation delay | 0.90 | 3.00 | 0.90 | 2.90 | 0.90 | 3.00 | ns | Figs. 6, 8, 9 |
| $t_{PHL}$ | MR to $Q_n$ | 0.90 | 3.00 | 0.90 | 2.90 | 0.90 | 3.00 | ns | |
| $t_{TLH}$ | Transition time | 0.60 | 2.20 | 0.60 | 2.10 | 0.45 | 2.20 | ns | Figs. 5, 8, 9 |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.60 | 2.20 | 0.60 | 2.10 | 0.45 | 2.20 | ns | |
| $t_s$ | Setup time<br>$D_n$ to $\overline{E}_n$ | 0.90 | | 0.90 | | 0.90 | | ns | Figs. 7, 9 |
| $t_h$ | Hold time<br>$D_n$ to $\overline{E}_n$ | 0.40 | | 0.40 | | 0.40 | | ns | |
| $t_s$ | Setup time<br>$S_0$, $S_1$ to $D_n$ | 2.40 | | 2.40 | | 2.70 | | ns | |
| $t_h$ | Hold time<br>$S_0$, $S_1$ to $D_n$ | −0.6 | | −0.6 | | −0.6 | | ns | |
| $t_r$ | Release time<br>MR to $\overline{E}_n$ | 1.50 | | 1.50 | | 1.50 | | ns | Figs. 6, 9 |
| $t_w(H)$ | Pulse width MR | 2.50 | | 2.50 | | 2.50 | | ns | Figs. 6, 9 |
| $t_w(L)$ | Pulse width $\overline{E}_0$, $\overline{E}_1$ | 2.50 | | 2.50 | | 2.50 | | ns | Figs. 5, 9 |

**Flat Pack** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 0.50 | 1.70 | 0.60 | 1.65 | 0.50 | 1.70 | ns | Figs. 5, 8, 9 |
| $t_{PHL}$ | $D_n$ to $Q_n$ | 0.50 | 1.70 | 0.60 | 1.65 | 0.50 | 1.70 | ns | |
| $t_{PLH}$ | Propagation delay | 1.50 | 3.30 | 1.50 | 3.20 | 1.50 | 3.30 | ns | |
| $t_{PHL}$ | $\overline{S}_0$, $S_1$ to $Q_n$ | 1.50 | 3.30 | 1.50 | 3.20 | 1.50 | 3.30 | ns | |
| $t_{PLH}$ | Propagation delay | 0.90 | 2.30 | 1.00 | 2.20 | 1.00 | 2.30 | ns | |
| $t_{PHL}$ | $\overline{E}_0$, $\overline{E}_0$ to $Q_n$ | 0.90 | 2.30 | 1.00 | 2.20 | 1.00 | 2.30 | ns | |
| $t_{PLH}$ | Propagation delay | 0.90 | 2.80 | 0.90 | 2.70 | 0.90 | 2.80 | ns | Figs. 6, 8, 9 |
| $t_{PHL}$ | MR to $Q_n$ | 0.90 | 2.80 | 0.90 | 2.70 | 0.90 | 2.80 | ns | |
| $t_{TLH}$ | Transition time | 0.60 | 2.20 | 0.60 | 2.10 | 0.45 | 2.20 | ns | Figs. 5, 8, 9 |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.60 | 2.20 | 0.60 | 2.10 | 0.45 | 2.20 | ns | |
| $t_s$ | Setup time<br>$D_n$ to $\overline{E}_n$ | 0.80 | | 0.80 | | 0.80 | | ns | Figs. 7, 9 |
| $t_h$ | Hold time<br>$D_n$ to $\overline{E}_n$ | 0.30 | | 0.30 | | 0.30 | | ns | |
| $t_s$ | Setup time<br>$\overline{S}_0$, $S_1$ to $D_n$ | 2.60 | | 2.60 | | 2.60 | | ns | |
| $t_h$ | Hold time<br>$\overline{S}_0$, $S_1$ to $D_n$ | −0.8 | | −0.8 | | −0.8 | | ns | |
| $t_r$ | Release time<br>MR to $\overline{E}_n$ | 1.40 | | 1.40 | | 1.40 | | ns | Figs. 6, 9 |
| $t_w(H)$ | Pulse width MR | 2.50 | | 2.50 | | 2.50 | | ns | Figs. 6, 9 |
| $t_w(L)$ | Pulse width $\overline{E}_0$, $\overline{E}_1$ | 2.50 | | 2.50 | | 2.50 | | ns | Figs. 5, 9 |

## AC ELECTRICAL CHARACTERISTICS

**Flat Pack** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V \pm 5\%$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | | |
| $t_{PLH}$ | Propagation delay | 0.50 | 1.70 | 0.60 | 1.65 | 0.50 | 1.70 | ns | Figs. 5, 8, 9 |
| $t_{PHL}$ | $D_n$ to $Q_n$ | 0.50 | 1.70 | 0.60 | 1.65 | 0.50 | 1.70 | ns | |
| $t_{PLH}$ | Propagation delay | 1.50 | 3.30 | 1.50 | 3.20 | 1.50 | 3.30 | ns | |
| $t_{PHL}$ | $\overline{S}_0$, $S_1$ to $Q_n$ | 1.50 | 3.30 | 1.50 | 3.20 | 1.50 | 3.30 | ns | |
| $t_{PLH}$ | Propagation delay | 0.90 | 2.30 | 1.00 | 2.20 | 1.00 | 2.30 | ns | |
| $t_{PHL}$ | $\overline{E}_0$, $\overline{E}_0$ to $Q_n$ | 0.90 | 2.30 | 1.00 | 2.20 | 1.00 | 2.30 | ns | |
| $t_{PLH}$ | Propagation delay | 0.90 | 2.80 | 0.90 | 2.70 | 0.90 | 2.80 | ns | Figs. 6, 8, 9 |
| $t_{PHL}$ | MR to $Q_n$ | 0.90 | 2.80 | 0.90 | 2.70 | 0.90 | 2.80 | ns | |
| $t_{TLH}$ | Transition time | 0.60 | 2.20 | 0.60 | 2.10 | 0.45 | 2.20 | ns | Figs. 5, 8, 9 |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.60 | 2.20 | 0.60 | 2.10 | 0.45 | 2.20 | ns | |
| $t_s$ | Setup time<br>$D_n$ to $\overline{E}_n$ | 0.80 | | 0.80 | | 0.80 | | ns | Figs. 7, 9 |
| $t_h$ | Hold time<br>$D_n$ to $\overline{E}_n$ | 0.30 | | 0.30 | | 0.30 | | ns | |
| $t_s$ | Setup time<br>$\overline{S}_0$, $S_1$ to $D_n$ | 2.60 | | 2.60 | | 2.60 | | ns | |
| $t_h$ | Hold time<br>$\overline{S}_0$, $S_1$ to $D_n$ | −0.8 | | −0.8 | | −0.8 | | ns | |
| $t_r$ | Release time<br>MR to $\overline{E}_n$ | 1.40 | | 1.40 | | 1.40 | | ns | Figs. 6, 9 |
| $t_w(H)$ | Pulse width MR | 2.50 | | 2.50 | | 2.50 | | ns | Figs. 6, 9 |
| $t_w(L)$ | Pulse width $\overline{E}_0$, $\overline{E}_1$ | 2.50 | | 2.50 | | 2.50 | | ns | Figs. 5, 9 |

## AC WAVEFORMS

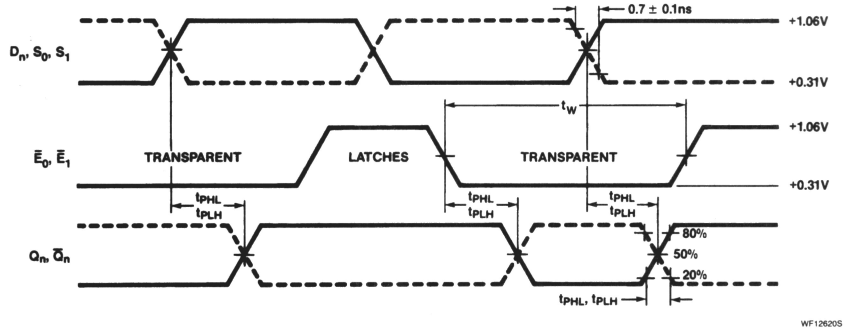

0.7 ± 0.1ns
Dn, S0, S1
+1.06V
+0.31V
tW
Ē0, Ē1
TRANSPARENT
LATCHES
TRANSPARENT
+1.06V
+0.31V
tPHL
tPLH
tPHL
tPLH
tPHL
tPLH
Qn, Q̄n
80%
50%
20%
tPHL, tPLH
WF12620S

Figure 5. Enable Timing

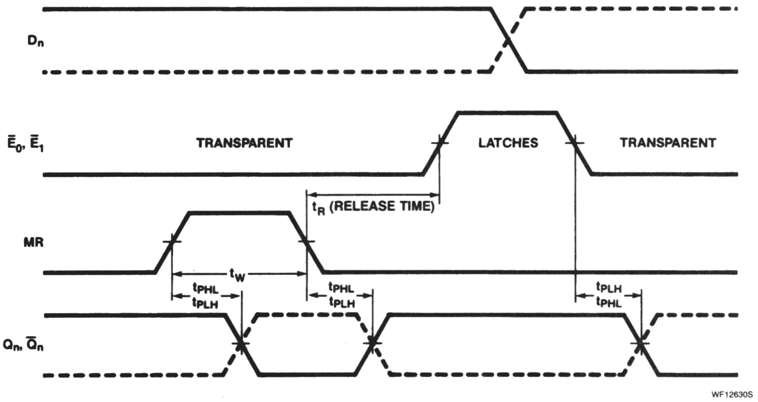

Dn
Ē0, Ē1
TRANSPARENT
LATCHES
TRANSPARENT
tR (RELEASE TIME)
MR
tW
tPHL
tPLH
tPHL
tPLH
tPLH
tPHL
Qn, Q̄n
WF12630S

Figure 6. Reset Timing

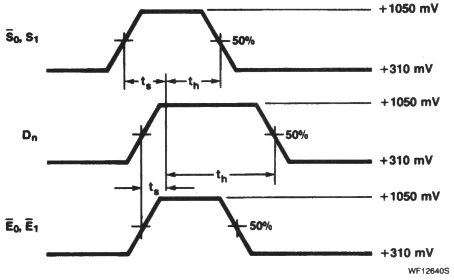
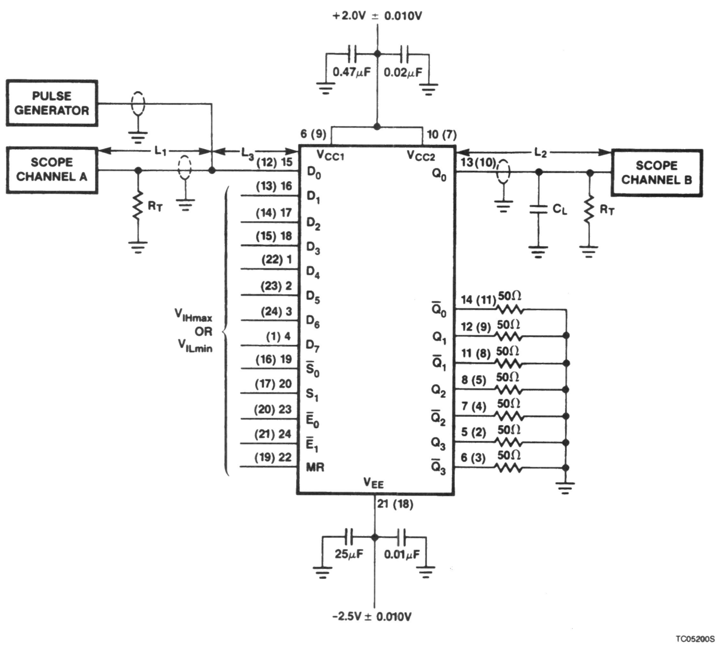

S̄0, S1
+1050 mV
50%
+310 mV
ts
th
+1050 mV
Dn
50%
+310 mV
th
ts
+1050 mV
Ē0, Ē1
50%
+310 mV
WF12640S

Figure 7. Setup and Hold Times

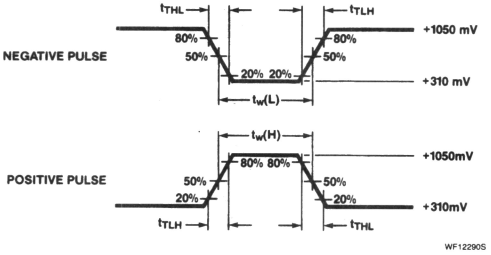
## TEST CIRCUITS AND WAVEFORMS


+2.0V ± 0.010V
0.47μF
0.02μF
PULSE GENERATOR
SCOPE CHANNEL A
L1
L3
RT
6 (9)
10 (7)
VCC1
VCC2
(12) 15 D0
(13) 16 D1
(14) 17 D2
(15) 18 D3
(22) 1 D4
(23) 2 D5
(24) 3 D6
(1) 4 D7
(16) 19 S̄0
(17) 20 S1
(20) 23 Ē0
(21) 24 Ē1
(19) 22 MR
VIHmax OR VILmin
Q0 13(10)
L2
SCOPE CHANNEL B
CL
RT
Q̄0 14 (11) 50Ω
Q1 12 (9) 50Ω
Q̄1 11 (8) 50Ω
Q2 8 (5) 50Ω
Q̄2 7 (4) 50Ω
Q3 5 (2) 50Ω
Q̄3 6 (3) 50Ω
VEE
21 (18)
25μF
0.01μF
-2.5V ± 0.010V
TC05200S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1μF and 25μF from GND to $V_{CC}$, 0.01μF and 25μF from GND to $V_{EE}$. (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance ≤ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.
11. Pin connections are for Flat Pack and in parentheses for Ceramic DIP.

**Figure 8. Test Circuit**


NEGATIVE PULSE
tTHL
tTLH
80%
50%
20% 20%
tw(L)
+1050 mV
+310 mV
POSITIVE PULSE
tw(H)
80% 80%
50%
20%
tTLH
tTHL
+1050mV
+310mV
WF12290S

**INPUT PULSE REQUIREMENTS**

**$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -2.5V \pm 0.010V$, $V_T$ = GND (0V)**

| Family | Amplitude | Rep Rate | Pulse Width | $t_{TLH}$ | $t_{THL}$ |
|---|---|---|---|---|---|
| 100K ECL | 740mVp-p | 1MHz | 500ns | 0.7 ±0.1ns | 0.7 ±0.1ns |

**Figure 9. Input Pulse Definition**

Signetics

# 100158
## Shift Matrix

**8-Bit Shift Matrix**
***Product Specification***

**ECL Products**

## DESCRIPTION

The 100158 contains a combinatorial network which performs the function of an 8-bit Shift Matrix. Three control lines ($S_n$) are internally decoded and define the number of places which an 8-bit word present at the inputs ($D_n$) is shifted to the left and presented at the outputs ($Q_n$). A Mode Control is provided which, if LOW, forces LOW all outputs to the right of the one that contains $D_7$. This operation is sometimes referred to as LOW backfill. If M is HIGH, an end-around shift is performed such that $D_0$ appears at the output to the right of the one that contains $D_7$. This operation is commonly referred to as barrel shifting.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 100158 | 1.9ns | 118mA |

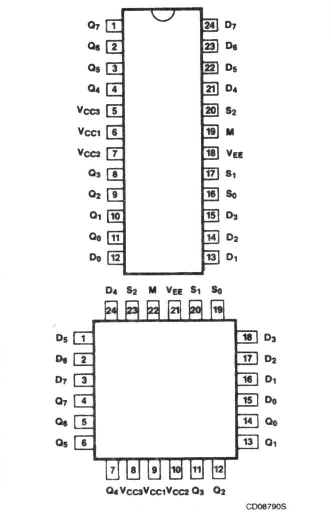
## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} = GND$; $V_{EE} = -4.2V$ to $-4.8V$<br>$T_A = 0°C$ to $+85°C$ |
|---|---|
| Ceramic DIP | 100158F |
| Ceramic Flat Pack | 100158Y |

## PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_0 - D_7$ | Data Inputs |
| $S_0 - S_2$ | Select Inputs |
| M | Mode Control Input |
| $Q_0 - Q_7$ | Data Output |

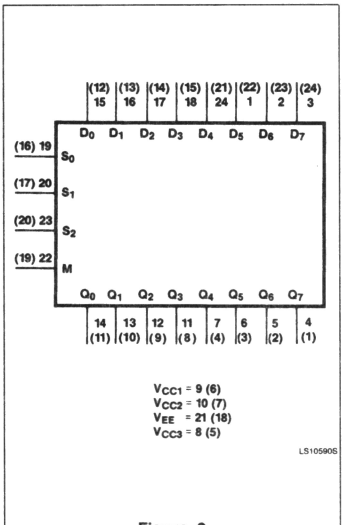
## PIN CONFIGURATION



Q7 1
Q6 2
Q5 3
Q4 4
VCC3 5
VCC1 6
VCC2 7
Q3 8
Q2 9
Q1 10
Q0 11
D0 12
24 D7
23 D6
22 D5
21 D4
20 S2
19 M
18 VEE
17 S1
16 S0
15 D3
14 D2
13 D1
D4 S2 M VEE S1 S0
24 23 22 21 20 19
D5 1
D6 2
D7 3
Q7 4
Q6 5
Q5 6
18 D3
17 D2
16 D1
15 D0
14 Q0
13 Q1
7 8 9 10 11 12
Q4 VCC3 VCC1 VCC2 Q3 Q2
CD08790S

Figure 1

## LOGIC SYMBOL



(12) 15
(13) 16
(14) 17
(15) 18
(21) 24
(22) 1
(23) 2
(24) 3
D0 D1 D2 D3 D4 D5 D6 D7
(16) 19 S0
(17) 20 S1
(20) 23 S2
(19) 22 M
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
14 (11)
13 (10)
12 (9)
11 (8)
7 (4)
6 (3)
5 (2)
4 (1)
VCC1 = 9 (6)
VCC2 = 10 (7)
VEE = 21 (18)
VCC3 = 8 (5)
LS10590S

Figure 2

# Shift Matrix 100158

## LOGIC DIAGRAM

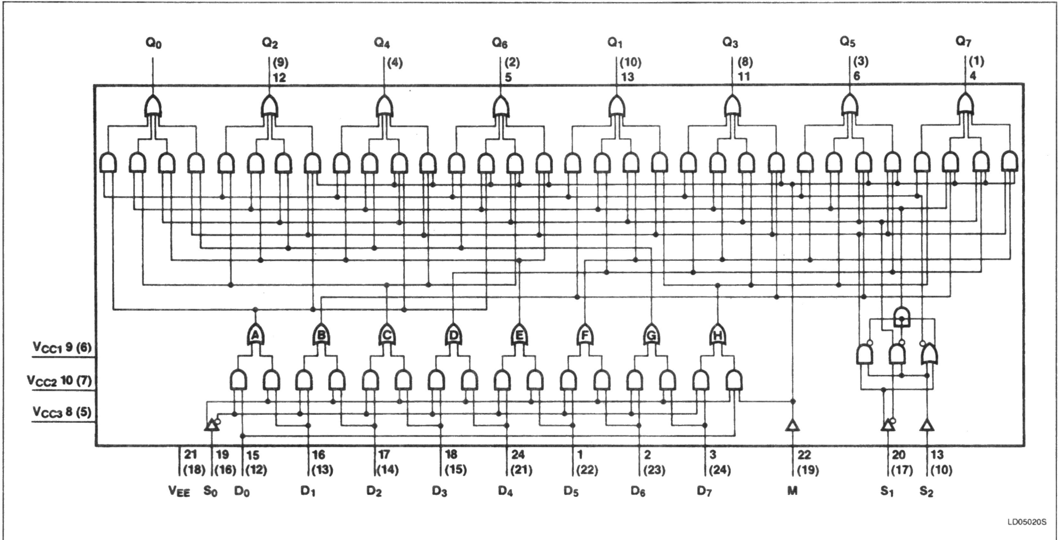

Q0
Q2 (9) 12
Q4 (4)
Q6 (2) 5
Q1 (10) 13
Q3 (8) 11
Q5 (3) 6
Q7 (1) 4
VCC1 9 (6)
VCC2 10 (7)
VCC3 8 (5)
A
B
C
D
E
F
G
H
21 (18) VEE
19 (16) S0
15 (12) D0
16 (13) D1
17 (14) D2
18 (15) D3
24 (21) D4
1 (22) D5
2 (23) D6
3 (24) D7
22 (19) M
20 (17) S1
13 (10) S2
LD05020S

Figure 3

## FUNCTION TABLE

| | INPUTS | | | | OUTPUTS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | M | $S_2$ | $S_1$ | $S_0$ | $Q_7$ | $Q_6$ | $Q_5$ | $Q_4$ | $Q_3$ | $Q_2$ | $Q_1$ | $Q_0$ |
| No shift | X | L | L | L | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
| Left shift | L | L | L | H | L | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ |
| | L | L | H | L | L | L | $D_7$ | $D_6$ | | | | |
| | L | L | H | H | L | L | L | $D_7$ | $D_6$ | | | |
| | L | H | L | L | L | L | L | L | $D_7$ | $D_6$ | | |
| | L | H | L | H | L | L | L | L | L | $D_7$ | $D_6$ | |
| | L | H | H | L | L | L | L | L | L | L | $D_7$ | $D_6$ |
| | L | H | H | L | L | L | L | L | L | L | L | $D_7$ |
| End around carry | H | L | L | H | $D_0$ | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ |
| | H | L | H | L | $D_1$ | $D_0$ | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ |
| | H | L | H | H | $D_2$ | $D_1$ | $D_0$ | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ |
| | H | H | L | L | $D_3$ | $D_2$ | $D_1$ | $D_0$ | $D_7$ | $D_6$ | $D_5$ | $D_4$ |
| | H | H | L | H | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ | $D_7$ | $D_6$ | $D_5$ |
| | H | H | H | L | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ | $D_7$ | $D_6$ |
| | H | H | H | H | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ | $D_7$ |

Positive Logic:
H = HIGH state (more positive voltage) = 1
L = LOW state (less positive voltage) = 0
Blank = Don't Care

## Shift Matrix 100158

**ABSOLUTE MAXIMUM RATINGS** (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | 100K ECL | UNIT |
|---|---|---|---|
| $V_{EE}$ | Supply voltage ($V_{CC1} = V_{CC2} = GND$) | −7.0 to 0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | $V_{EE}$ to +0.5 | V |
| $I_O$ | Output source current | −55 | mA |
| $T_S$ | Storage temperature | −65 to +150 | °C |
| $T_J$ | Maximum junction temperature | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | | 100K ECL | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | −4.2 | −4.5 | −4.8 | V |
| $V_{EE}$ | Supply voltage (negative) when operating with 10K ECL family | | | | | −5.7 | V |
| $V_{IH}$ | HIGH level input voltage | $V_{CC1} = V_{CC2} = GND$<br>$T_A = 0°C$ to $+85°C$ | $V_{EE} = -4.2V$ | −1150 | | −880 | mV |
| | | | $V_{EE} = -4.5V$ | −1165 | | | |
| | | | $V_{EE} = -4.8V$ | | | | |
| $V_{IHT}$ | HIGH level input threshold voltage | | $V_{EE} = -4.2V$ | −1150 | | | mV |
| | | | $V_{EE} = -4.5V$ | −1165 | | | mV |
| | | | $V_{EE} = -4.8V$ | | | | |
| $V_{ILT}$ | LOW level input threshold voltage | | $V_{EE} = -4.2V$ | | | −1475 | mV |
| | | | $V_{EE} = -4.5V$ | | | | |
| | | | $V_{EE} = -4.8V$ | | | −1490 | mV |
| $V_{IL}$ | LOW level input voltage | | $V_{EE} = -4.2V$ | −1810 | | −1475 | mV |
| | | | $V_{EE} = -4.5V$ | | | | |
| | | | $V_{EE} = -4.8V$ | | | −1490 | |
| $T_A$ | Operating ambient temperature | | | 0 | +25 | +85 | °C |

**NOTE:**
When operating at other than specified voltages (−4.2V, −4.5V, −4.8V) DC & AC Characteristics will vary slightly from specified values.

## Shift Matrix 100158

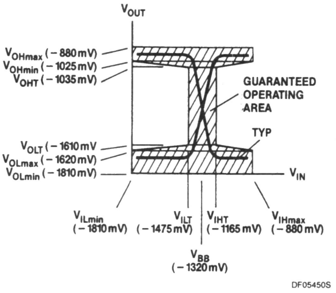
**DC ELECTRICAL CHARACTERISTICS** $V_{CC1} = V_{CC2}$ = GND, $V_{EE}$ = −4.2V ±0.010V to −4.8V ±0.010V, $T_A$ = 0°C to +85°C unless otherwise specified[1,3]

| PARAMETER | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] | |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | $V_{EE}$ = −4.2V | −1025 | | −870 | mV | $V_{IN} = V_{IHmax}$ or $V_{IN} = V_{ILmin}$ | Loading with 50Ω to −2.0V ±0.010V |
| | | $V_{EE}$ = −4.5V | −1025 | −955 | −880 | mV | | |
| | | $V_{EE}$ = −4.8V | −1035 | | −880 | mV | | |
| $V_{OHT}$ | HIGH level output threshold voltage | $V_{EE}$ = −4.2V | −1035 | | | mV | $V_{IN} = V_{IHmin}$ or $V_{IN} = V_{ILmax}$ | |
| | | $V_{EE}$ = −4.5V | −1035 | | | mV | | |
| | | $V_{EE}$ = −4.8V | −1045 | | | mV | | |
| $V_{OLT}$ | LOW level output threshold voltage | $V_{EE}$ = −4.2V | | | −1590 | mV | $V_{IN} = V_{IHmin}$ or $V_{IN} = V_{ILmax}$ | |
| | | $V_{EE}$ = −4.5V | | | −1610 | mV | | |
| | | $V_{EE}$ = −4.8V | | | −1610 | mV | | |
| $V_{OL}$ | LOW level output voltage | $V_{EE}$ = −4.2V | −1810 | | −1600 | mV | $V_{IN} = V_{IHmax}$ or $V_{IN} = V_{ILmin}$ | |
| | | $V_{EE}$ = −4.5V | −1810 | −1705 | −1620 | mV | | |
| | | $V_{EE}$ = −4.8V | −1830 | | −1620 | mV | | |
| $I_{IH}$ | HIGH level input current | | | | 220 | μA | $V_{IN} = V_{IHmax}$ | |
| $I_{IL}$ | LOW level input current | | 0.5 | | | μA | $V_{IN} = V_{ILmin}$ | |
| $-I_{EE}$ | $V_{EE}$ supply current | | 84 | 118 | 205 | mA | Inputs open | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | $V_{EE}$ = −4.2V<br>$T_A$ = +25°C | | | 0.025 | V/V | | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | | 0.050 | V/V | | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 4.

## Shift Matrix 100158



**NOTES:**

| | |
|---|---|
| $V_{IHmax}$ | – Maximum HIGH level input voltage (the most positive $V_{IH}$). |
| $V_{IHT}$ | – HIGH level input threshold voltage. |
| $V_{ILT}$ | – LOW level input threshold voltage. |
| $V_{ILmin}$ | – Minimum LOW level input voltage (the most negative $V_{IL}$). |
| $V_{OHmax}$ | – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition. |
| $V_{OHmin}$ | – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition. |
| $V_{OHT}$ | – HIGH level output threshold voltage with the inputs set to their respective threshold levels. |
| $V_{OLT}$ | – LOW level output threshold voltage with the inputs set to their respective threshold levels. |
| $V_{OLmax}$ | – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions. |
| $V_{OLmin}$ | – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions. |
| $V_{BB}$ | – Reference bias voltage. The internally generated reference voltage which is used to set the input and output threshold level. |

Figure 4. Transfer Characteristics

## AC ELECTRICAL CHARACTERISTICS

**Ceramic DIP** $V_{CC1} = V_{CC2}$ = GND, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$

| PARAMETER | | $T_A$ = 0°C | | $T_A$ = +25°C | | $T_A$ = +85°C | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$D_n$ to $Q_n$ | 1.10<br>1.10 | 3.00<br>3.00 | 1.10<br>1.10 | 2.90<br>2.90 | 1.10<br>1.10 | 3.10<br>3.10 | ns<br>ns | Figs. 5, 6, 7 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>M to $Q_n$ | 1.15<br>1.15 | 4.40<br>4.40 | 1.25<br>1.25 | 4.40<br>4.40 | 1.15<br>1.15 | 4.70<br>4.70 | ns<br>ns | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$S_n$ to $Q_n$ | 1.70<br>1.70 | 4.50<br>4.50 | 1.70<br>1.70 | 4.50<br>4.50 | 1.70<br>1.70 | 4.80<br>4.80 | ns<br>ns | |
| $t_{TLH}$<br>$t_{THL}$ | Transition time<br>20% to 80%, 80% to 20% | 0.50<br>0.50 | 2.20<br>2.20 | 0.50<br>0.50 | 2.20<br>2.20 | 0.50<br>0.50 | 2.20<br>2.20 | ns<br>ns | |

**Ceramic DIP** $V_{CC1} = V_{CC2}$ = GND, $V_{EE} = -5.2V \pm 5\%$

| PARAMETER | | $T_A$ = 0°C | | $T_A$ = +25°C | | $T_A$ = +85°C | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$D_n$ to $Q_n$ | 1.10<br>1.10 | 3.00<br>3.00 | 1.10<br>1.10 | 2.90<br>2.90 | 1.10<br>1.10 | 3.10<br>3.10 | ns<br>ns | Figs. 5, 6, 7 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>M to $Q_n$ | 1.15<br>1.15 | 4.40<br>4.40 | 1.25<br>1.25 | 4.40<br>4.40 | 1.15<br>1.15 | 4.70<br>4.70 | ns<br>ns | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$S_n$ to $Q_n$ | 1.70<br>1.70 | 4.50<br>4.50 | 1.70<br>1.70 | 4.50<br>4.50 | 1.70<br>1.70 | 4.80<br>4.80 | ns<br>ns | |
| $t_{TLH}$<br>$t_{THL}$ | Transition time<br>20% to 80%, 80% to 20% | 0.50<br>0.50 | 2.20<br>2.20 | 0.50<br>0.50 | 2.20<br>2.20 | 0.50<br>0.50 | 2.20<br>2.20 | ns<br>ns | |

## AC ELECTRICAL CHARACTERISTICS

**Flat Pack** $V_{CC1} = V_{CC2} = \text{GND}$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 1.10 | 2.80 | 1.10 | 2.70 | 1.10 | 2.90 | ns | Figs. 5, 6, 7 |
| $t_{PHL}$ | $D_n$ to $Q_n$ | 1.10 | 2.80 | 1.10 | 2.70 | 1.10 | 2.90 | ns | |
| $t_{PLH}$ | Propagation delay | 1.15 | 4.20 | 1.25 | 4.20 | 1.15 | 4.50 | ns | |
| $t_{PHL}$ | M to $Q_n$ | 1.15 | 4.20 | 1.25 | 4.20 | 1.15 | 4.50 | ns | |
| $t_{PLH}$ | Propagation delay | 1.70 | 4.30 | 1.70 | 4.30 | 1.70 | 4.60 | ns | |
| $t_{PHL}$ | $S_n$ to $Q_n$ | 1.70 | 4.30 | 1.70 | 4.30 | 1.70 | 4.60 | ns | |
| $t_{TLH}$ | Transition time | 0.50 | 2.20 | 0.50 | 2.20 | 0.50 | 2.20 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.50 | 2.20 | 0.50 | 2.20 | 0.50 | 2.20 | ns | |

**Flat Pack** $V_{CC1} = V_{CC2} = \text{GND}$, $V_{EE} = -5.2V \pm 5\%$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 1.10 | 2.80 | 1.10 | 2.70 | 1.10 | 2.90 | ns | Figs. 5, 6, 7 |
| $t_{PHL}$ | $D_n$ to $Q_n$ | 1.10 | 2.80 | 1.10 | 2.70 | 1.10 | 2.90 | ns | |
| $t_{PLH}$ | Propagation delay | 1.15 | 4.20 | 1.25 | 4.20 | 1.15 | 4.50 | ns | |
| $t_{PHL}$ | M to $Q_n$ | 1.15 | 4.20 | 1.25 | 4.20 | 1.15 | 4.50 | ns | |
| $t_{PLH}$ | Propagation delay | 1.70 | 4.30 | 1.70 | 4.30 | 1.70 | 4.60 | ns | |
| $t_{PHL}$ | $S_n$ to $Q_n$ | 1.70 | 4.30 | 1.70 | 4.30 | 1.70 | 4.60 | ns | |
| $t_{TLH}$ | Transition time | 0.50 | 2.20 | 0.50 | 2.20 | 0.50 | 2.20 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.50 | 2.20 | 0.50 | 2.20 | 0.50 | 2.20 | ns | |

## AC WAVEFORMS

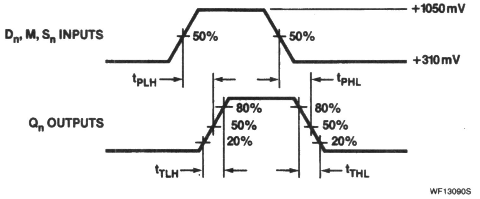
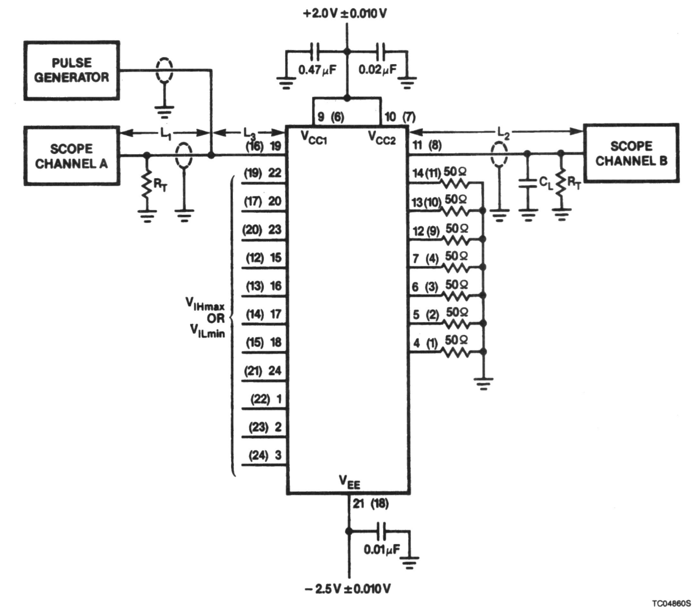


Figure 5. Propagation Delay and Transition Times

## Shift Matrix 100158

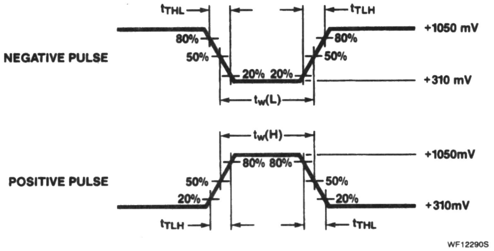
### TEST CIRCUITS AND WAVEFORMS


+2.0V ±0.010V
0.47μF
0.02μF
PULSE GENERATOR
SCOPE CHANNEL A
$L_1$
$L_3$
$R_T$
9 (6)
10 (7)
$V_{CC1}$
$V_{CC2}$
(16) 19
(19) 22
(17) 20
(20) 23
(12) 15
(13) 16
(14) 17
(15) 18
(21) 24
(22) 1
(23) 2
(24) 3
$V_{IHmax}$ OR $V_{ILmin}$
11 (8)
14 (11) 50Ω
13 (10) 50Ω
12 (9) 50Ω
7 (4) 50Ω
6 (3) 50Ω
5 (2) 50Ω
4 (1) 50Ω
$L_2$
$C_L$
$R_T$
SCOPE CHANNEL B
$V_{EE}$
21 (18)
0.01μF
−2.5V ±0.010V
TC04860S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1μF and 25μF from GND to $V_{CC}$, 0.01μF and 25μF from GND to $V_{EE}$. (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance ≤ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.
11. Pin connections are for Flat Pack and in parentheses for Ceramic DIP.

Figure 6. Test Circuit


NEGATIVE PULSE
$t_{THL}$
$t_{TLH}$
80%
50%
20%
20%
80%
50%
+1050 mV
+310 mV
$t_w(L)$
$t_w(H)$
POSITIVE PULSE
80%
80%
50%
20%
50%
20%
+1050mV
+310mV
$t_{TLH}$
$t_{THL}$
WF12290S

| INPUT PULSE REQUIREMENTS<br>$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -2.5V \pm 0.010V$, $V_T$ = GND (0V) | | | | | |
|---|---|---|---|---|---|
| Family | Amplitude | Rep Rate | Pulse Width | $t_{TLH}$ | $t_{THL}$ |
| 100K ECL | 740mVp-p | 1MHz | 500ns | 0.7 ±0.1ns | 0.7 ±0.1ns |

Figure 7. Input Pulse Definition

Signetics

# 100160
# Parity Generator/Comparator

**Dual 9-Bit Parity Generator/8-Bit Comparator**
***Product Specification***

**ECL Products**

## DESCRIPTION

The 100160 is a dual 9-bit Parity Generator. It generates high parity outputs for an even number of high inputs on respective 9-bit input groups. The circuit also compares 8 pairs of inputs and has an active LOW output ($\overline{C}$), if all 8 pairs are equal.

The input $D_a$, $D_b$ have the shorter throughput delay and can serve for generating parity for 16 or more bits.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 100160 | 1.8ns | 78mA |

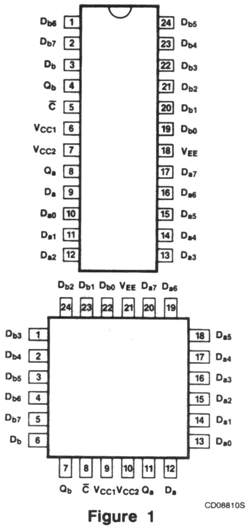
## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} = GND$; $V_{EE} = -4.2V$ to $-4.8V$<br>$T_A = 0°C$ to $+85°C$ |
|---|---|
| Ceramic DIP | 100160F |
| Ceramic Flat Pack | 100160Y |

## PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_a$, $D_b$ | Parity Inputs |
| $D_{a0} - D_{a7}$, $D_{b0} - D_{b7}$ | Data Inputs |
| $\overline{C}$ | Compare Output |
| $Q_a$, $Q_b$ | Parity Odd Output |

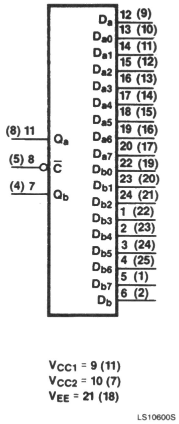
## PIN CONFIGURATION



Db6 1, Db7 2, Db 3, Qb 4, C̄ 5, VCC1 6, VCC2 7, Qa 8, Da 9, Da0 10, Da1 11, Da2 12
24 Db5, 23 Db4, 22 Db3, 21 Db2, 20 Db1, 19 Db0, 18 VEE, 17 Da7, 16 Da6, 15 Da5, 14 Da4, 13 Da3
Db2 24, Db1 23, Db0 22, VEE 21, Da7 20, Da6 19
Db3 1, Db4 2, Db5 3, Db6 4, Db7 5, Db 6
18 Da5, 17 Da4, 16 Da3, 15 Da2, 14 Da1, 13 Da0
7 Qb, 8 C̄, 9 VCC1, 10 VCC2, 11 Qa, 12 Da
CD08810S

Figure 1

## LOGIC SYMBOL



Da 12 (9)
Da0 13 (10)
Da1 14 (11)
Da2 15 (12)
Da3 16 (13)
Da4 17 (14)
Da5 18 (15)
Da6 19 (16)
Da7 20 (17)
Db0 22 (19)
Db1 23 (20)
Db2 24 (21)
Db3 1 (22)
Db4 2 (23)
Db5 3 (24)
Db6 4 (25)
Db7 5 (1)
Db 6 (2)
(8) 11 Qa
(5) 8 C̄
(4) 7 Qb
VCC1 = 9 (11)
VCC2 = 10 (7)
VEE = 21 (18)
LS10600S

Figure 2

# Parity Generator/Comparator 100160

## LOGIC DIAGRAM

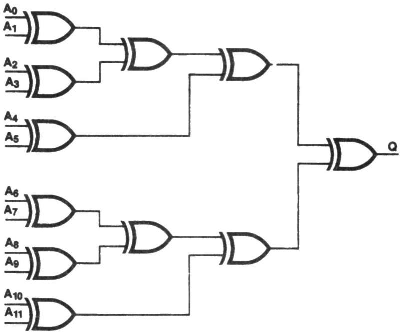


Figure 3

## FUNCTION TABLE

| INPUTS | | OUTPUTS | | |
|---|---|---|---|---|
| $D_a$, $D_{a0}$, $D_{a1}$, $D_{a2}$, $D_{a3}$, $D_{a4}$, $D_{a5}$, $D_{a6}$, $D_{a7}$ | $D_a$, $D_{b0}$, $D_{b1}$, $D_{b2}$, $D_{b3}$, $D_{b4}$, $D_{b5}$, $D_{b6}$, $D_{b7}$ | $Q_a$ | $Q_b$ | $\overline{C}$ |
| Sum of HIGH bits ODD | | L | | |
| Sum of HIGH bits EVEN | | H | | |
| | Sum of HIGH bits ODD | | L | |
| | Sum of HIGH bits EVEN | | H | |
| $D_{a0} = D_{b0}$, $D_{a1} = D_{b1}$, $D_{a2} = D_{b2}$, $D_{a3} = D_{b3}$, $D_{a4} = D_{b4}$, $D_{a5} = D_{b5}$, $D_{a6} = D_{b6}$, $D_{a7} = D_{b7}$ | | | | L |
| All other combinations | | | | H |

Positive Logic:
H = HIGH state (the more positive voltage) = 1
L = LOW state (the less positive voltage) = 0

## Parity Generator/Comparator 100160

**ABSOLUTE MAXIMUM RATINGS** (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | 100K ECL | UNIT |
|---|---|---|---|
| $V_{EE}$ | Supply voltage ($V_{CC1} = V_{CC2} = GND$) | −7.0 to 0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | $V_{EE}$ to +0.5 | V |
| $I_O$ | Output source current | −55 | mA |
| $T_S$ | Storage temperature | −65 to +150 | °C |
| $T_J$ | Maximum junction temperature | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | | 100K ECL | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | −4.2 | −4.5 | −4.8 | V |
| $V_{EE}$ | Supply voltage (negative) when operating with 10K ECL family | | | | | −5.7 | V |
| $V_{IH}$ | HIGH level input voltage | $V_{CC1} = V_{CC2} = GND$<br>$T_A = 0°C$ to $+85°C$ | $V_{EE} = -4.2V$ | −1150 | | −880 | mV |
| | | | $V_{EE} = -4.5V$ | −1165 | | | |
| | | | $V_{EE} = -4.8V$ | | | | |
| $V_{IHT}$ | HIGH level input threshold voltage | | $V_{EE} = -4.2V$ | −1150 | | | mV |
| | | | $V_{EE} = -4.5V$ | −1165 | | | mV |
| | | | $V_{EE} = -4.8V$ | | | | |
| $V_{ILT}$ | LOW level input threshold voltage | | $V_{EE} = -4.2V$ | | | −1475 | mV |
| | | | $V_{EE} = -4.5V$ | | | | |
| | | | $V_{EE} = -4.8V$ | | | −1490 | mV |
| $V_{IL}$ | LOW level input voltage | | $V_{EE} = -4.2V$ | −1810 | | −1475 | mV |
| | | | $V_{EE} = -4.5V$ | | | | |
| | | | $V_{EE} = -4.8V$ | | | −1490 | |
| $T_A$ | Operating ambient temperature | | | 0 | +25 | +85 | °C |

**NOTE:**
When operating at other than specified voltages (−4.2V, −4.5V, −4.8V) DC & AC Characteristics will vary slightly from specified values.

## Parity Generator/Comparator 100160

**DC ELECTRICAL CHARACTERISTICS** $V_{CC1} = V_{CC2} =$ GND, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$, $T_A = 0°C$ to $+85°C$ unless otherwise specified[1,3]

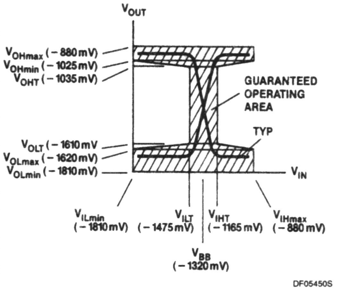
| PARAMETER | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] | |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | $V_{EE} = -4.2V$ | -1025 | | -870 | mV | $V_{IN} = V_{IHmax}$ or $V_{IN} = V_{ILmin}$ | Loading with 50Ω to -2.0V ±0.010V |
| | | $V_{EE} = -4.5V$ | -1025 | -955 | -880 | mV | | |
| | | $V_{EE} = -4.8V$ | -1035 | | -880 | mV | | |
| $V_{OHT}$ | HIGH level output threshold voltage | $V_{EE} = -4.2V$ | -1035 | | | mV | $V_{IN} = V_{IHmin}$ or $V_{IN} = V_{ILmax}$ | |
| | | $V_{EE} = -4.5V$ | -1035 | | | mV | | |
| | | $V_{EE} = -4.8V$ | -1045 | | | mV | | |
| $V_{OLT}$ | LOW level output threshold voltage | $V_{EE} = -4.2V$ | | | -1590 | mV | $V_{IN} = V_{IHmin}$ or $V_{IN} = V_{ILmax}$ | |
| | | $V_{EE} = -4.5V$ | | | -1610 | mV | | |
| | | $V_{EE} = -4.8V$ | | | -1610 | mV | | |
| $V_{OL}$ | LOW level output voltage | $V_{EE} = -4.2V$ | -1810 | | -1600 | mV | $V_{IN} = V_{IHmax}$ or $V_{IN} = V_{ILmin}$ | |
| | | $V_{EE} = -4.5V$ | -1810 | -1705 | -1620 | mV | | |
| | | $V_{EE} = -4.8V$ | -1830 | | -1620 | mV | | |
| $I_{IH}$ | HIGH level input current | $D_a$, $D_b$ | | | 340 | µA | $V_{IN} = V_{IHmax}$ | |
| | | $D_{an}$, $D_{bn}$ | | | 340 | µA | | |
| $I_{IL}$ | LOW level input current | | 0.5 | | | µA | $V_{IN} = V_{ILmin}$ | |
| $-I_{EE}$ | $V_{EE}$ supply current | | 57 | 78 | 115 | mA | Inputs open | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | $V_{EE} = -4.2V$<br>$T_A = +25°C$ | | | 0.025 | V/V | | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | | 0.050 | V/V | | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 4.

# Parity Generator/Comparator

# 100160



**NOTES:**

$V_{IHmax}$ – Maximum HIGH level input voltage (the most positive $V_{IH}$).
$V_{IHT}$ – HIGH level input threshold voltage.
$V_{ILT}$ – LOW level input threshold voltage.
$V_{ILmin}$ – Minimum LOW level input voltage (the most negative $V_{IL}$).
$V_{OHmax}$ – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition.
$V_{OHmin}$ – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition.
$V_{OHT}$ – HIGH level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLT}$ – LOW level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLmax}$ – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions.
$V_{OLmin}$ – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions.
$V_{BB}$ – Reference bias voltage (the internally generated reference voltage which is used to set the input and output threshold level).

**Figure 4. Transfer Characteristics**

## AC ELECTRICAL CHARACTERISTICS

**Ceramic DIP** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 1.30 | 4.30 | 1.30 | 4.10 | 1.30 | 4.30 | ns | Figs. 5, 6, 7 |
| $t_{PHL}$ | $D_{an}$, $D_{bn}$ to $Q_a$, $Q_b$ | 1.30 | 4.30 | 1.30 | 4.10 | 1.30 | 4.30 | ns | |
| $t_{PLH}$ | Propagation delay | 0.50 | 1.60 | 0.50 | 1.60 | 0.50 | 1.60 | ns | |
| $t_{PHL}$ | $D_a$, $D_b$ to $Q_a$, $Q_b$ | 0.50 | 1.60 | 0.50 | 1.60 | 0.50 | 1.60 | ns | |
| $t_{PLH}$ | Propagation delay | 1.20 | 3.30 | 1.20 | 3.10 | 1.20 | 3.30 | ns | |
| $t_{PHL}$ | $D_{an}$, $D_{bn}$ to $\overline{C}$ | 1.20 | 3.30 | 1.20 | 3.10 | 1.20 | 3.30 | ns | |
| $t_{TLH}$ | Transition time | 0.40 | 1.70 | 0.40 | 1.65 | 0.40 | 1.65 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.40 | 1.70 | 0.40 | 1.65 | 0.40 | 1.65 | ns | |

**Ceramic DIP** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V \pm 5\%$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 1.30 | 4.30 | 1.30 | 4.10 | 1.30 | 4.30 | ns | Figs. 5, 6, 7 |
| $t_{PHL}$ | $D_{an}$, $D_{bn}$ to $Q_a$, $Q_b$ | 1.30 | 4.30 | 1.30 | 4.10 | 1.30 | 4.30 | ns | |
| $t_{PLH}$ | Propagation delay | 0.50 | 1.60 | 0.50 | 1.60 | 0.50 | 1.60 | ns | |
| $t_{PHL}$ | $D_a$, $D_b$ to $Q_a$, $Q_b$ | 0.50 | 1.60 | 0.50 | 1.60 | 0.50 | 1.60 | ns | |
| $t_{PLH}$ | Propagation delay | 1.20 | 3.30 | 1.20 | 3.10 | 1.20 | 3.30 | ns | |
| $t_{PHL}$ | $D_{an}$, $D_{bn}$ to $\overline{C}$ | 1.20 | 3.30 | 1.20 | 3.10 | 1.20 | 3.30 | ns | |
| $t_{TLH}$ | Transition time | 0.40 | 1.70 | 0.40 | 1.65 | 0.40 | 1.65 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.40 | 1.70 | 0.40 | 1.65 | 0.40 | 1.65 | ns | |

## Parity Generator/Comparator

## 100160

### AC ELECTRICAL CHARACTERISTICS

**Flat Pack** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$

| | PARAMETER | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$D_{an}$, $D_{bn}$ to $Q_a$, $Q_b$ | 1.30<br>1.30 | 4.10<br>4.10 | 1.30<br>1.30 | 3.90<br>3.90 | 1.30<br>1.30 | 4.10<br>4.10 | ns<br>ns | Figs. 5, 6, 7 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$D_a$, $D_b$ to $Q_a$, $Q_b$ | 0.50<br>0.50 | 1.40<br>1.40 | 0.50<br>0.50 | 1.40<br>1.40 | 0.50<br>0.50 | 1.40<br>1.40 | ns<br>ns | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$D_{an}$, $D_{bn}$ to $\overline{C}$ | 1.20<br>1.20 | 3.10<br>3.10 | 1.20<br>1.20 | 2.90<br>2.90 | 1.20<br>1.20 | 3.10<br>3.10 | ns<br>ns | |
| $t_{TLH}$<br>$t_{THL}$ | Transition time<br>20% to 80%, 80% to 20% | 0.40<br>0.40 | 1.70<br>1.70 | 0.40<br>0.40 | 1.65<br>1.65 | 0.40<br>0.40 | 1.65<br>1.65 | ns<br>ns | |

**Flat Pack** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V \pm 5\%$

| | PARAMETER | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$D_{an}$, $D_{bn}$ to $Q_a$, $Q_b$ | 1.30<br>1.30 | 4.10<br>4.10 | 1.30<br>1.30 | 3.90<br>3.90 | 1.30<br>1.30 | 4.10<br>4.10 | ns<br>ns | Figs. 5, 6, 7 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$D_a$, $D_b$ to $Q_a$, $Q_b$ | 0.50<br>0.50 | 1.40<br>1.40 | 0.50<br>0.50 | 1.40<br>1.40 | 0.50<br>0.50 | 1.40<br>1.40 | ns<br>ns | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$D_{an}$, $D_{bn}$ to $\overline{C}$ | 1.20<br>1.20 | 3.10<br>3.10 | 1.20<br>1.20 | 2.90<br>2.90 | 1.20<br>1.20 | 3.10<br>3.10 | ns<br>ns | |
| $t_{TLH}$<br>$t_{THL}$ | Transition time<br>20% to 80%, 80% to 20% | 0.40<br>0.40 | 1.70<br>1.70 | 0.40<br>0.40 | 1.65<br>1.65 | 0.40<br>0.40 | 1.65<br>1.65 | ns<br>ns | |

### AC WAVEFORMS

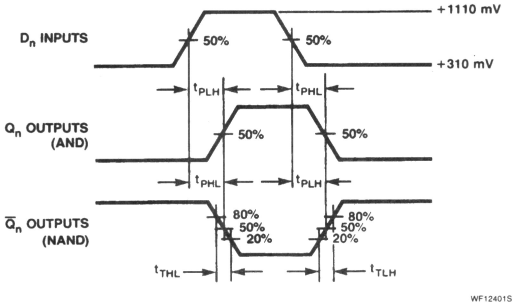
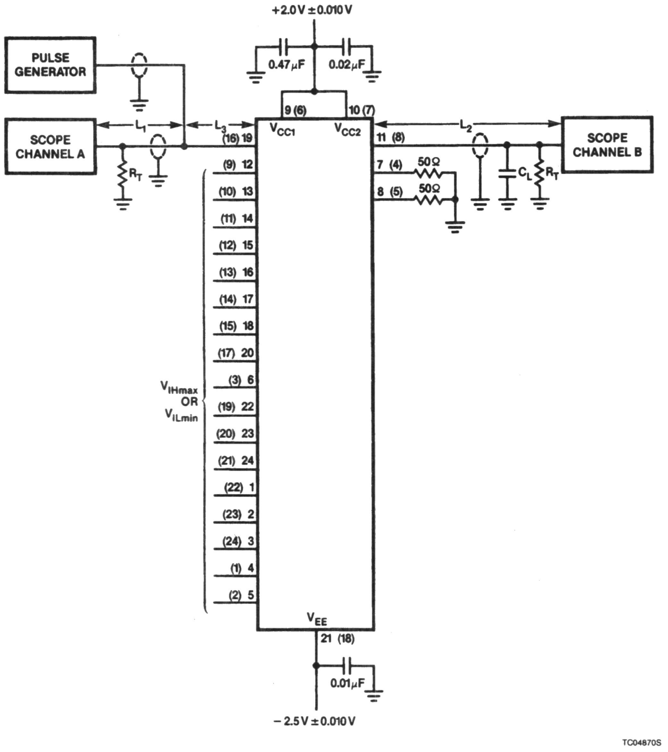


Figure 5. Propagation Delay and Transition Times

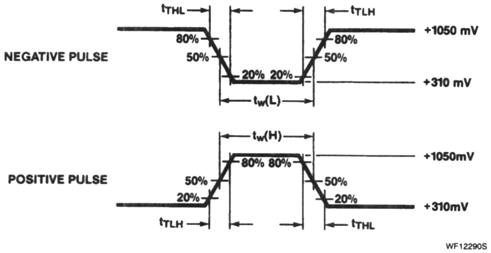
## TEST CIRCUITS AND WAVEFORMS


+2.0V ±0.010V
0.47μF
0.02μF
PULSE GENERATOR
SCOPE CHANNEL A
$L_1$
$L_3$
$R_T$
9 (6)
10 (7)
$V_{CC1}$
$V_{CC2}$
(16) 19
(9) 12
(10) 13
(11) 14
(12) 15
(13) 16
(14) 17
(15) 18
(17) 20
(3) 6
(19) 22
(20) 23
(21) 24
(22) 1
(23) 2
(24) 3
(1) 4
(2) 5
$V_{IHmax}$ OR $V_{ILmin}$
11 (8)
7 (4)
8 (5)
50Ω
50Ω
$L_2$
$C_L$
$R_T$
SCOPE CHANNEL B
$V_{EE}$
21 (18)
0.01μF
−2.5V ±0.010V
TC04870S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1μF and 25μF from GND to $V_{CC}$. 0.01μF and 25μF from GND to $V_{EE}$. (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance ≤ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ±1% or better.
11. Pin connections are for Flat Pack and in parentheses for Ceramic DIP.

Figure 6. Test Circuit


NEGATIVE PULSE
$t_{THL}$
$t_{TLH}$
80%
50%
20%
20%
80%
50%
+1050 mV
+310 mV
$t_w(L)$
POSITIVE PULSE
$t_w(H)$
80%
80%
50%
20%
50%
20%
+1050mV
+310mV
$t_{TLH}$
$t_{THL}$
WF12290S

| INPUT PULSE REQUIREMENTS<br>$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -2.5V \pm 0.010V$, $V_T$ = GND (0V) | | | | | |
|---|---|---|---|---|---|
| Family | Amplitude | Rep Rate | Pulse Width | $t_{TLH}$ | $t_{THL}$ |
| 100K ECL | 740mVp-p | 1MHz | 500ns | 0.7 ±0.1ns | 0.7 ±0.1ns |

Figure 7. Input Pulse Definition

# Signetics

# 100163
## Multiplexer

**Dual 8-Input Multiplexer**
***Product Specification***

**ECL Products**

### DESCRIPTION

The 100163 circuit is a dual 8-input multiplexer fed by 3 common address inputs. The 3-bit address selects one of eight data lines in each multiplexer, which is gated to the output.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 100163 | 1.25ns | 125mA |

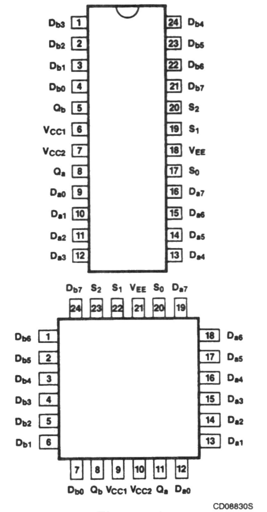
### ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} = GND$; $V_{EE} = -4.2V$ to $-4.8V$<br>$T_A = 0°C$ to $+85°C$ |
|---|---|
| Ceramic DIP | 100163F |
| Ceramic Flat Pack | 100163Y |

### PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_{a0} - D_{a7}$ | Data Inputs |
| $D_{b0} - D_{b7}$ | Data Inputs |
| $S_0$, $S_1$, $S_2$ | Data Select Inputs |
| $Q_a$, $Q_b$ | Data Outputs |

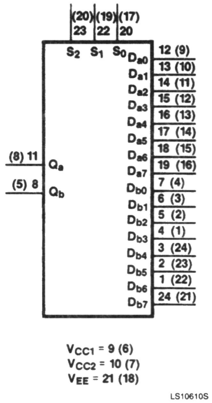
### PIN CONFIGURATION



Db3 1
Db2 2
Db1 3
Db0 4
Qb 5
VCC1 6
VCC2 7
Qa 8
Da0 9
Da1 10
Da2 11
Da3 12
24 Db4
23 Db5
22 Db6
21 Db7
20 S2
19 S1
18 VEE
17 S0
16 Da7
15 Da6
14 Da5
13 Da4
Db7 S2 S1 VEE S0 Da7
24 23 22 21 20 19
Db6 1
Db5 2
Db4 3
Db3 4
Db2 5
Db1 6
18 Da6
17 Da5
16 Da4
15 Da3
14 Da2
13 Da1
7 8 9 10 11 12
Db0 Qb VCC1 VCC2 Qa Da0
CD08830S

Figure 1

### LOGIC SYMBOL



(20) 23
(19) 22
(17) 20
S2
S1
S0
Da0 12 (9)
Da1 13 (10)
Da2 14 (11)
Da3 15 (12)
Da4 16 (13)
Da5 17 (14)
Da6 18 (15)
Da7 19 (16)
Db0 7 (4)
Db1 6 (3)
Db2 5 (2)
Db3 4 (1)
Db4 3 (24)
Db5 2 (23)
Db6 1 (22)
Db7 24 (21)
(8) 11 Qa
(5) 8 Qb
VCC1 = 9 (6)
VCC2 = 10 (7)
VEE = 21 (18)
LS10610S

Figure 2

## LOGIC DIAGRAM

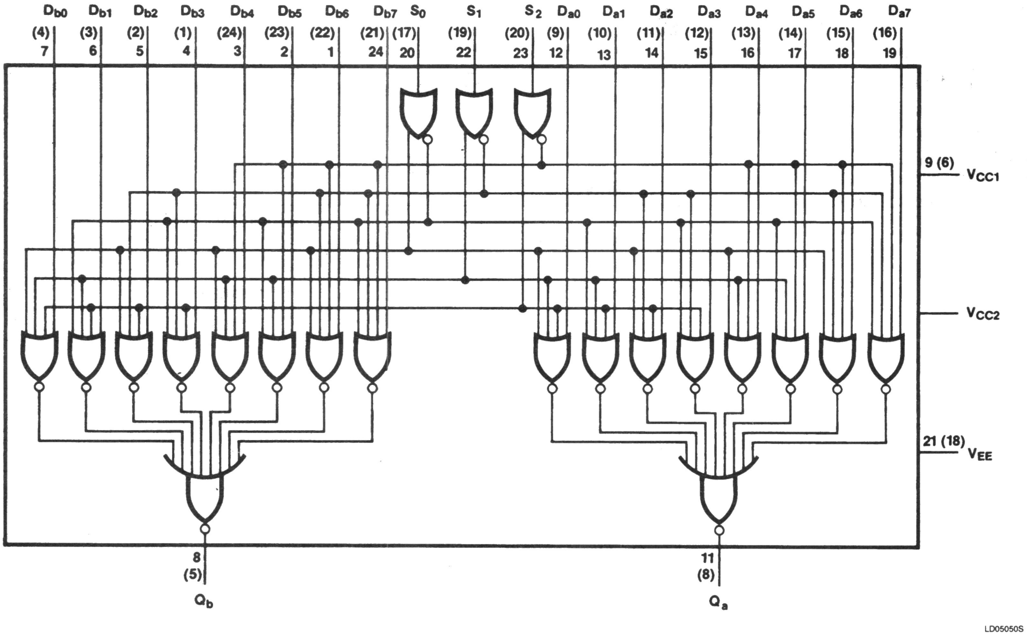

D_b0 (4) 7
D_b1 (3) 6
D_b2 (2) 5
D_b3 (1) 4
D_b4 (24) 3
D_b5 (23) 2
D_b6 (22) 1
D_b7 (21) 24
S_0 (17) 20
S_1 (19) 22
S_2 (20) 23
D_a0 (9) 12
D_a1 (10) 13
D_a2 (11) 14
D_a3 (12) 15
D_a4 (13) 16
D_a5 (14) 17
D_a6 (15) 18
D_a7 (16) 19
9 (6) V_CC1
V_CC2
21 (18) V_EE
8 (5) Q_b
11 (8) Q_a
LD05050S

Figure 3

## FUNCTION TABLE

| INPUTS | | | OUTPUT | |
|---|---|---|---|---|
| $S_0$ | $S_1$ | $S_2$ | $Q_a$ | $Q_b$ |
| L | L | L | $D_{a0}$ | $D_{b0}$ |
| H | L | L | $D_{a1}$ | $D_{b1}$ |
| L | H | L | $D_{a2}$ | $D_{b2}$ |
| H | H | L | $D_{a3}$ | $D_{b3}$ |
| L | L | L | $D_{a4}$ | $D_{b4}$ |
| H | L | L | $D_{a5}$ | $D_{b5}$ |
| L | H | L | $D_{a6}$ | $D_{b6}$ |
| H | H | L | $D_{a7}$ | $D_{b7}$ |

Positive Logic:
H = HIGH state (the more positive voltage) = 1
L = LOW state (the less positive voltage) = 0
X = Don't Care

## Multiplexer 100163

**ABSOLUTE MAXIMUM RATINGS** (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | 100K ECL | UNIT |
|---|---|---|---|
| $V_{EE}$ | Supply voltage ($V_{CC1} = V_{CC2} =$ GND) | −7.0 to 0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | $V_{EE}$ to +0.5 | V |
| $I_O$ | Output source current | −55 | mA |
| $T_S$ | Storage temperature | −65 to +150 | °C |
| $T_J$ | Maximum junction temperature | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | | 100K ECL | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | −4.2 | −4.5 | −4.8 | V |
| $V_{EE}$ | Supply voltage (negative) when operating with 10K ECL family | | | | | −5.7 | V |
| $V_{IH}$ | HIGH level input voltage | $V_{CC1} = V_{CC2} =$ GND<br>$T_A = 0°C$ to $+85°C$ | $V_{EE} = -4.2V$ | −1150 | | −880 | mV |
| | | | $V_{EE} = -4.5V$ | −1165 | | | |
| | | | $V_{EE} = -4.8V$ | | | | |
| $V_{IHT}$ | HIGH level input threshold voltage | | $V_{EE} = -4.2V$ | −1150 | | | mV |
| | | | $V_{EE} = -4.5V$ | −1165 | | | mV |
| | | | $V_{EE} = -4.8V$ | | | | |
| $V_{ILT}$ | LOW level input threshold voltage | | $V_{EE} = -4.2V$ | | | −1475 | mV |
| | | | $V_{EE} = -4.5V$ | | | | |
| | | | $V_{EE} = -4.8V$ | | | −1490 | mV |
| $V_{IL}$ | LOW level input voltage | | $V_{EE} = -4.2V$ | −1810 | | −1475 | mV |
| | | | $V_{EE} = -4.5V$ | | | | |
| | | | $V_{EE} = -4.8V$ | | | −1490 | |
| $T_A$ | Operating ambient temperature | | | 0 | +25 | +85 | °C |

**NOTE:**
When operating at other than specified voltages (−4.2V, −4.5V, −4.8V) DC & AC Characteristics will vary slightly from specified values.

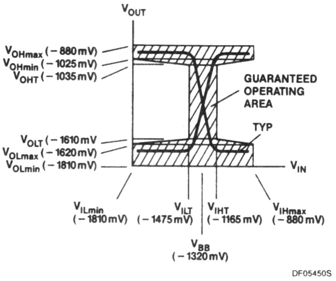
## DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2} = GND$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$, $T_A = 0°C$ to $+85°C$ unless otherwise specified[1, 3]

| PARAMETER | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] | |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | $V_{EE} = -4.2V$ | -1025 | | -870 | mV | $V_{IN} = V_{IHmax}$<br>or<br>$V_{IN} = V_{ILmin}$ | Loading with 50Ω to -2.0V ±0.010V |
| | | $V_{EE} = -4.5V$ | -1025 | -955 | -880 | mV | | |
| | | $V_{EE} = -4.8V$ | -1035 | | -880 | mV | | |
| $V_{OHT}$ | HIGH level output threshold voltage | $V_{EE} = -4.2V$ | -1035 | | | mV | $V_{IN} = V_{IHmin}$<br>or<br>$V_{IN} = V_{ILmax}$ | |
| | | $V_{EE} = -4.5V$ | -1035 | | | mV | | |
| | | $V_{EE} = -4.8V$ | -1045 | | | mV | | |
| $V_{OLT}$ | LOW level output threshold voltage | $V_{EE} = -4.2V$ | | | -1590 | mV | $V_{IN} = V_{IHmin}$<br>or<br>$V_{IN} = V_{ILmax}$ | |
| | | $V_{EE} = -4.5V$ | | | -1610 | mV | | |
| | | $V_{EE} = -4.8V$ | | | -1610 | mV | | |
| $V_{OL}$ | LOW level output voltage | $V_{EE} = -4.2V$ | -1810 | | -1600 | mV | $V_{IN} = V_{IHmax}$<br>or<br>$V_{IN} = V_{ILmin}$ | |
| | | $V_{EE} = -4.5V$ | -1810 | -1705 | -1620 | mV | | |
| | | $V_{EE} = -4.8V$ | -1830 | | -1620 | mV | | |
| $I_{IH}$ | HIGH level input current | $S_n$ | | | 265 | µA | $V_{IN} = V_{IHmax}$ | |
| | | $D_{an}$, $D_{bn}$ | | | 340 | µA | | |
| $I_{IL}$ | LOW level input current | | 0.5 | | | µA | $V_{IN} = V_{ILmin}$ | |
| $-I_{EE}$ | $V_{EE}$ supply current | | 76 | 125 | 161 | mA | Inputs open | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | $V_{EE} = -4.2V$<br>$T_A = +25°C$ | | | 0.025 | V/V | | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | | 0.050 | V/V | | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 4.



**NOTES:**

$V_{IHmax}$ – Maximum HIGH level input voltage (the most positive $V_{IH}$).
$V_{IHT}$ – HIGH level input threshold voltage.
$V_{ILT}$ – LOW level input threshold voltage.
$V_{ILmin}$ – Minimum LOW level input voltage (the most negative $V_{IL}$).
$V_{OHmax}$ – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition.
$V_{OHmin}$ – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition.
$V_{OHT}$ – HIGH level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLT}$ – LOW level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLmax}$ – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions.
$V_{OLmin}$ – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions.
$V_{BB}$ – Reference bias voltage. The internally generated reference voltage which is used to set the input and output threshold level.

Figure 4. Transfer Characteristics

## AC ELECTRICAL CHARACTERISTICS

### Ceramic DIP $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 0.55 | 1.90 | 0.60 | 1.90 | 0.65 | 2.00 | ns | Figs. 5, 6, 7 |
| $t_{PHL}$ | $D_{an}$, $D_{bn}$ to $Q_a$, $Q_b$ | 0.55 | 1.90 | 0.60 | 1.90 | 0.65 | 2.00 | ns | |
| $t_{PLH}$ | Propagation delay | 1.10 | 2.80 | 1.10 | 2.80 | 1.20 | 3.10 | ns | |
| $t_{PHL}$ | $S_n$ to $Q_a$, $Q_b$ | 1.10 | 2.80 | 1.10 | 2.80 | 1.20 | 3.10 | ns | |
| $t_{TLH}$ | Transition time | 0.50 | 1.75 | 0.50 | 1.70 | 0.50 | 1.70 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.50 | 1.75 | 0.50 | 1.70 | 0.50 | 1.70 | ns | |

### Ceramic DIP $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V \pm 5\%$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 0.55 | 1.90 | 0.60 | 1.90 | 0.65 | 2.00 | ns | Figs. 5, 6, 7 |
| $t_{PHL}$ | $D_{an}$, $D_{bn}$ to $Q_a$, $Q_b$ | 0.55 | 1.90 | 0.60 | 1.90 | 0.65 | 2.00 | ns | |
| $t_{PLH}$ | Propagation delay | 1.10 | 2.80 | 1.10 | 2.80 | 1.20 | 3.10 | ns | |
| $t_{PHL}$ | $S_n$ to $Q_a$, $Q_b$ | 1.10 | 2.80 | 1.10 | 2.80 | 1.20 | 3.10 | ns | |
| $t_{TLH}$ | Transition time | 0.50 | 1.75 | 0.50 | 1.70 | 0.50 | 1.70 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.50 | 1.75 | 0.50 | 1.70 | 0.50 | 1.70 | ns | |

### Flat Pack $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 0.55 | 1.70 | 0.60 | 1.70 | 0.65 | 1.80 | ns | Figs. 5, 6, 7 |
| $t_{PHL}$ | $D_{an}$, $D_{bn}$ to $Q_a$, $Q_b$ | 0.55 | 1.70 | 0.60 | 1.70 | 0.65 | 1.80 | ns | |
| $t_{PLH}$ | Propagation delay | 1.10 | 2.60 | 1.10 | 2.60 | 1.20 | 2.90 | ns | |
| $t_{PHL}$ | $S_n$ to $Q_a$, $Q_b$ | 1.10 | 2.60 | 1.10 | 2.60 | 1.20 | 2.90 | ns | |
| $t_{TLH}$ | Transition time | 0.50 | 1.75 | 0.50 | 1.70 | 0.50 | 1.70 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.50 | 1.75 | 0.50 | 1.70 | 0.50 | 1.70 | ns | |

## AC ELECTRICAL CHARACTERISTICS

**Flat Pack** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V \pm 5\%$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$D_{an}$, $D_{bn}$ to $Q_a$, $Q_b$ | 0.55<br>0.55 | 1.70<br>1.70 | 0.60<br>0.60 | 1.70<br>1.70 | 0.65<br>0.65 | 1.80<br>1.80 | ns<br>ns | Figs. 5, 6, 7 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$S_n$ to $Q_a$, $Q_b$ | 1.10<br>1.10 | 2.60<br>2.60 | 1.10<br>1.10 | 2.60<br>2.60 | 1.20<br>1.20 | 2.90<br>2.90 | ns<br>ns | |
| $t_{TLH}$<br>$t_{THL}$ | Transition time<br>20% to 80%, 80% to 20% | 0.50<br>0.50 | 1.75<br>1.75 | 0.50<br>0.50 | 1.70<br>1.70 | 0.50<br>0.50 | 1.70<br>1.70 | ns<br>ns | |

## AC WAVEFORMS

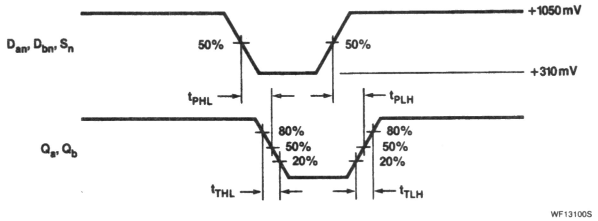
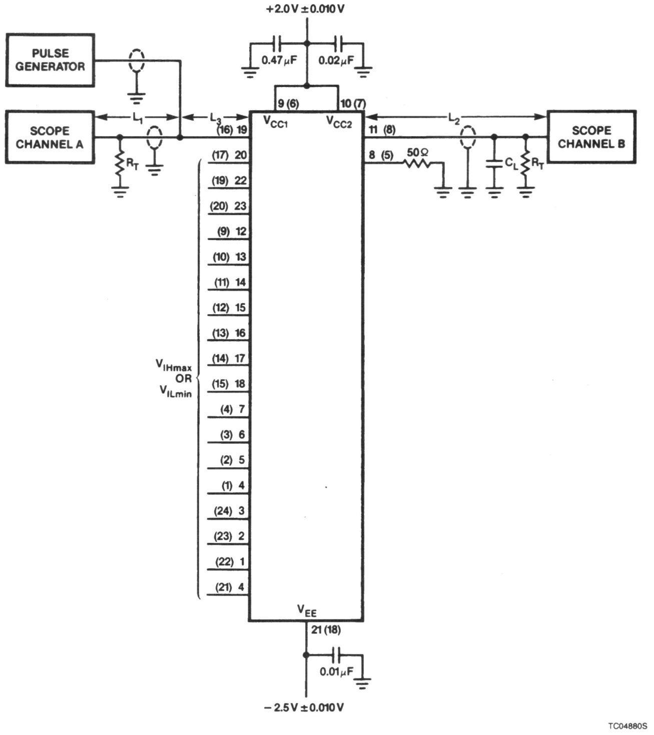

$D_{an}$, $D_{bn}$, $S_n$
50%
50%
+1050mV
+310mV
$t_{PHL}$
$t_{PLH}$
$Q_a$, $Q_b$
80%
50%
20%
80%
50%
20%
$t_{THL}$
$t_{TLH}$
WF13100S

**Figure 5. Propagation Delay For Data and Select Inputs to Output**

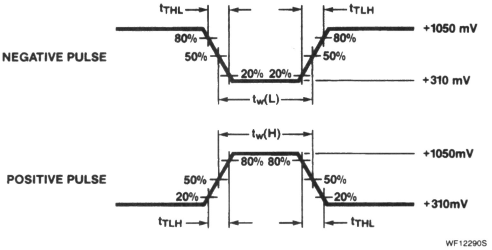
## TEST CIRCUITS AND WAVEFORMS


+2.0V ±0.010V
0.47μF
0.02μF
PULSE GENERATOR
SCOPE CHANNEL A
L1
L3
RT
9 (6)
10 (7)
VCC1
VCC2
(16) 19
(17) 20
(19) 22
(20) 23
(9) 12
(10) 13
(11) 14
(12) 15
(13) 16
(14) 17
(15) 18
(4) 7
(3) 6
(2) 5
(1) 4
(24) 3
(23) 2
(22) 1
(21) 4
VIHmax OR VILmin
11 (8)
8 (5)
50Ω
L2
CL
RT
SCOPE CHANNEL B
VEE
21 (18)
0.01μF
−2.5V ±0.010V
TC04880S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1μF and 25μF from GND to $V_{CC}$, 0.01μF and 25μF from GND to $V_{EE}$. (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance $\leq$ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ±1% or better.
11. Pin connections are for Flat Pack and in parentheses for Ceramic DIP.

Figure 6. Test Circuit


tTHL
tTLH
NEGATIVE PULSE
80%
50%
20%
20%
80%
50%
+1050 mV
+310 mV
tw(L)
tw(H)
POSITIVE PULSE
50%
20%
80%
80%
50%
20%
+1050mV
+310mV
tTLH
tTHL
WF12290S

**INPUT PULSE REQUIREMENTS**
$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -2.5V \pm 0.010V$, $V_T$ = GND (0V)

| Family | Amplitude | Rep Rate | Pulse Width | $t_{TLH}$ | $t_{THL}$ |
|---|---|---|---|---|---|
| 100K ECL | 740mVp-p | 1MHz | 500ns | 0.7 ±0.1ns | 0.7 ±0.1ns |

Figure 7. Input Pulse Definition

Signetics

# 100164
# Multiplexer

**16-Input Multiplexer**
***Product Specification***

**ECL Products**

## DESCRIPTION

The 100164 is a 16-way multiplexer for one bit. Four address inputs select one of the 16 input bits which is gated to the output.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 100164 | 1.60ns | 71mA |

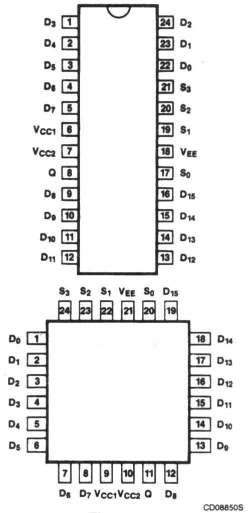
## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC1} = V_{CC2} = GND$; $V_{EE} = -4.2V$ to $-4.8V$ $T_A = 0°C$ to $+85°C$ |
|---|---|
| Ceramic DIP | 100164F |
| Ceramic Flat Pack | 100164Y |

## PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_0 - D_{15}$ | Data Inputs |
| $S_0 - S_3$ | Data Select Inputs |
| Q | Data Output |

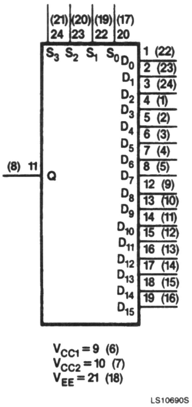
## PIN CONFIGURATION



D3 1
D4 2
D5 3
D6 4
D7 5
VCC1 6
VCC2 7
Q 8
D8 9
D9 10
D10 11
D11 12
24 D2
23 D1
22 D0
21 S3
20 S2
19 S1
18 VEE
17 S0
16 D15
15 D14
14 D13
13 D12
S3 S2 S1 VEE S0 D15
24 23 22 21 20 19
D0 1
D1 2
D2 3
D3 4
D4 5
D5 6
18 D14
17 D13
16 D12
15 D11
14 D10
13 D9
7 8 9 10 11 12
D6 D7 VCC1 VCC2 Q D8
CD08850S

Figure 1

## LOGIC SYMBOL



(21) 24
(20) 23
(19) 22
(17) 20
S3 S2 S1 S0
D0 1 (22)
D1 2 (23)
D2 3 (24)
D3 4 (1)
D4 5 (2)
D5 6 (3)
D6 7 (4)
D7 8 (5)
D8 12 (9)
D9 13 (10)
D10 14 (11)
D11 15 (12)
D12 16 (13)
D13 17 (14)
D14 18 (15)
D15 19 (16)
(8) 11 Q
VCC1 = 9 (6)
VCC2 = 10 (7)
VEE = 21 (18)
LS10690S

Figure 2

# Multiplexer

# 100164

## LOGIC DIAGRAM

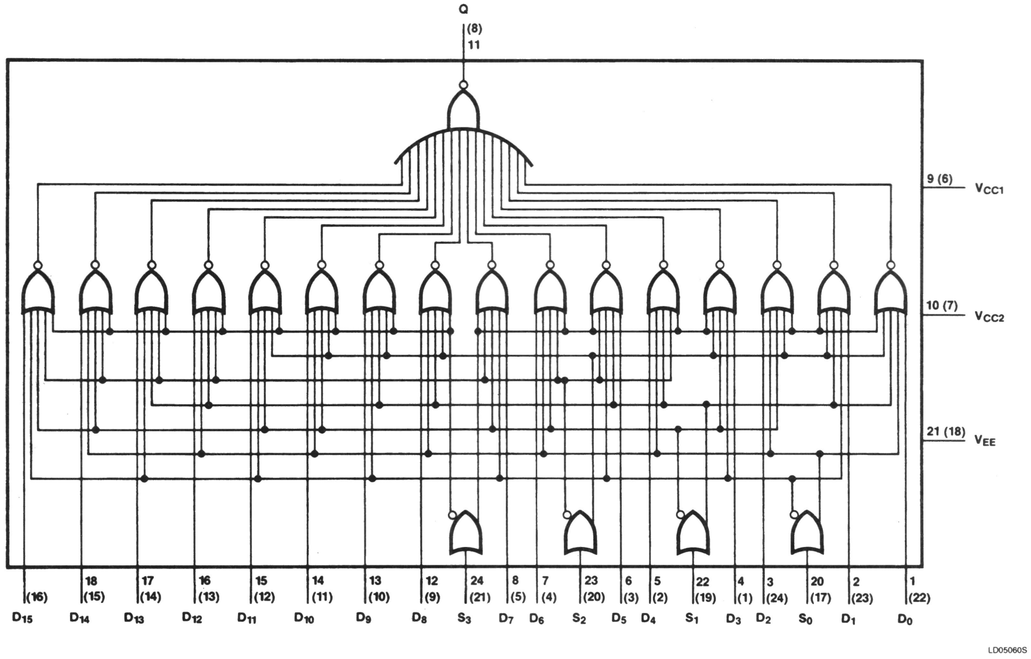

Q
(8)
11
9 (6)
VCC1
10 (7)
VCC2
21 (18)
VEE
(16)
D15
18
(15)
D14
17
(14)
D13
16
(13)
D12
15
(12)
D11
14
(11)
D10
13
(10)
D9
12
(9)
D8
24
(21)
S3
8
(5)
D7
7
(4)
D6
23
(20)
S2
6
(3)
D5
5
(2)
D4
22
(19)
S1
4
(1)
D3
3
(24)
D2
20
(17)
S0
2
(23)
D1
1
(22)
D0
LD05060S

Figure 3

## FUNCTION TABLE

| INPUTS | | | | OUTPUT |
|---|---|---|---|---|
| $S_3$ | $S_2$ | $S_1$ | $S_0$ | Q |
| L | L | L | L | $D_0$ |
| L | L | L | H | $D_1$ |
| L | L | H | L | $D_2$ |
| L | L | H | H | $D_3$ |
| L | H | L | L | $D_4$ |
| L | H | L | H | $D_5$ |
| L | H | H | L | $D_6$ |
| L | H | H | H | $D_7$ |
| H | L | L | L | $D_8$ |
| H | L | L | H | $D_9$ |
| H | L | H | L | $D_{10}$ |
| H | L | H | H | $D_{11}$ |
| H | H | L | L | $D_{12}$ |
| H | H | L | H | $D_{13}$ |
| H | H | H | L | $D_{14}$ |
| H | H | H | H | $D_{15}$ |

Positive Logic:
H = HIGH state (the more positive voltage) = 1
L = LOW state (the less positive voltage) = 0

# Multiplexer

# 100164

## ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | 100K ECL | UNIT |
|---|---|---|---|
| $V_{EE}$ | Supply voltage ($V_{CC1} = V_{CC2}$ = GND) | -7.0 to 0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | $V_{EE}$ to +0.5 | V |
| $I_O$ | Output source current | -55 | mA |
| $T_S$ | Storage temperature | -65 to +150 | °C |
| $T_J$ | Maximum junction temperature | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | | 100K ECL | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | -4.2 | -4.5 | -4.8 | V |
| $V_{EE}$ | Supply voltage (negative) when operating with 10K ECL family | | | | | -5.7 | V |
| $V_{IH}$ | HIGH level input voltage | $V_{CC1} = V_{CC2}$ = GND<br>$T_A$ = 0°C to +85°C | $V_{EE} = -4.2V$ | -1150 | | -880 | mV |
| | | | $V_{EE} = -4.5V$ | -1165 | | | |
| | | | $V_{EE} = -4.8V$ | | | | |
| $V_{IHT}$ | HIGH level input threshold voltage | | $V_{EE} = -4.2V$ | -1150 | | | mV |
| | | | $V_{EE} = -4.5V$ | -1165 | | | mV |
| | | | $V_{EE} = -4.8V$ | | | | |
| $V_{ILT}$ | LOW level input threshold voltage | | $V_{EE} = -4.2V$ | | | -1475 | mV |
| | | | $V_{EE} = -4.5V$ | | | | |
| | | | $V_{EE} = -4.8V$ | | | -1490 | mV |
| $V_{IL}$ | LOW level input voltage | | $V_{EE} = -4.2V$ | -1810 | | -1475 | mV |
| | | | $V_{EE} = -4.5V$ | | | | |
| | | | $V_{EE} = -4.8V$ | | | -1490 | |
| $T_A$ | Operating ambient temperature | | | 0 | +25 | +85 | °C |

**NOTE:**
When operating at other than specified voltages (-4.2V, -4.5V, -4.8V) DC & AC Characteristics will vary slightly from specified values.

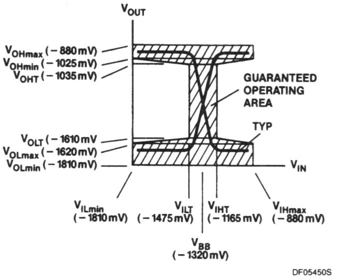
## DC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} =$ GND, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$, $T_A = 0°C$ to $+85°C$ unless otherwise specified[1,3]

| PARAMETER | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] | |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | $V_{EE} = -4.2V$ | −1025 | | −870 | mV | $V_{IN} = V_{IHmax}$ or $V_{IN} = V_{ILmin}$ | Loading with 50Ω to −2.0V ±0.010V |
| | | $V_{EE} = -4.5V$ | −1025 | −955 | −880 | mV | | |
| | | $V_{EE} = -4.8V$ | −1035 | | −880 | mV | | |
| $V_{OHT}$ | HIGH level output threshold voltage | $V_{EE} = -4.2V$ | −1035 | | | mV | $V_{IN} = V_{IHmin}$ or $V_{IN} = V_{ILmax}$ | |
| | | $V_{EE} = -4.5V$ | −1035 | | | mV | | |
| | | $V_{EE} = -4.8V$ | −1045 | | | mV | | |
| $V_{OLT}$ | LOW level output threshold voltage | $V_{EE} = -4.2V$ | | | −1590 | mV | $V_{IN} = V_{IHmin}$ or $V_{IN} = V_{ILmax}$ | |
| | | $V_{EE} = -4.5V$ | | | −1610 | mV | | |
| | | $V_{EE} = -4.8V$ | | | −1610 | mV | | |
| $V_{OL}$ | LOW level output voltage | $V_{EE} = -4.2V$ | −1810 | | −1600 | mV | $V_{IN} = V_{IHmax}$ or $V_{IN} = V_{ILmin}$ | |
| | | $V_{EE} = -4.5V$ | −1810 | −1705 | −1620 | mV | | |
| | | $V_{EE} = -4.8V$ | −1830 | | −1620 | mV | | |
| $I_{IH}$ | HIGH level input current | $D_n$ | | | 280 | µA | $V_{IN} = V_{IHmax}$ | |
| | | $S_0$, $S_1$ | | | 240 | µA | | |
| | | $S_2$, $S_3$ | | | 240 | µA | | |
| $I_{IL}$ | LOW level input current | | 0.5 | | | µA | $V_{IN} = V_{ILmin}$ | |
| $-I_{EE}$ | $V_{EE}$ supply current | | 49 | 71 | 105 | mA | Inputs open | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | $V_{EE} = -4.2V$<br>$T_A = +25°C$ | | | 0.025 | V/V | | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | | 0.050 | V/V | | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 4.

# Multiplexer 100164



**NOTES:**

| | |
|---|---|
| $V_{IHmax}$ | – Maximum HIGH level input voltage (the most positive $V_{IH}$). |
| $V_{IHT}$ | – HIGH level input threshold voltage. |
| $V_{ILT}$ | – LOW level input threshold voltage. |
| $V_{ILmin}$ | – Minimum LOW level input voltage (the most negative $V_{IL}$). |
| $V_{OHmax}$ | – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition. |
| $V_{OHmin}$ | – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition. |
| $V_{OHT}$ | – HIGH level output threshold voltage with the inputs set to their respective threshold levels. |
| $V_{OLT}$ | – LOW level output threshold voltage with the inputs set to their respective threshold levels. |
| $V_{OLmax}$ | – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions. |
| $V_{OLmin}$ | – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions. |
| $V_{BB}$ | – Reference bias voltage. The internally generated reference voltage which is used to set the input and output threshold level. |

Figure 4. Transfer Characteristics

## AC ELECTRICAL CHARACTERISTICS

**Ceramic DIP** $V_{CC1} = V_{CC2} =$ GND, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 0.80 | 2.20 | 0.90 | 2.35 | 0.90 | 2.55 | ns | Figs. 5, 6, 7 |
| $t_{PHL}$ | $D_n$ to $Q_n$ | 0.80 | 2.20 | 0.90 | 2.35 | 0.90 | 2.55 | ns | |
| $t_{PLH}$ | Propagation delay | 1.45 | 3.20 | 1.45 | 3.20 | 1.45 | 3.60 | ns | |
| $t_{PHL}$ | $S_0$, $S_1$ to $Q_n$ | 1.45 | 3.20 | 1.45 | 3.20 | 1.45 | 3.60 | ns | |
| $t_{PLH}$ | Propagation delay | 1.10 | 2.50 | 1.10 | 2.50 | 1.10 | 2.80 | ns | |
| $t_{PHL}$ | $S_2$, $S_3$ to $Q_n$ | 1.10 | 2.50 | 1.10 | 2.50 | 1.10 | 2.80 | ns | |
| $t_{TLH}$ | Transition time | 0.45 | 1.60 | 0.45 | 1.60 | 0.45 | 1.60 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.60 | 0.45 | 1.60 | 0.45 | 1.60 | ns | |

**Ceramic DIP** $V_{CC1} = V_{CC2} =$ GND, $V_{EE} = -5.2V \pm 5\%$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 0.80 | 2.20 | 0.90 | 2.35 | 0.90 | 2.55 | ns | Figs. 5, 6, 7 |
| $t_{PHL}$ | $D_n$ to $Q_n$ | 0.80 | 2.20 | 0.90 | 2.35 | 0.90 | 2.55 | ns | |
| $t_{PLH}$ | Propagation delay | 1.45 | 3.20 | 1.45 | 3.20 | 1.45 | 3.60 | ns | |
| $t_{PHL}$ | $S_0$, $S_1$ to $Q_n$ | 1.45 | 3.20 | 1.45 | 3.20 | 1.45 | 3.60 | ns | |
| $t_{PLH}$ | Propagation delay | 1.10 | 2.50 | 1.10 | 2.50 | 1.10 | 2.80 | ns | |
| $t_{PHL}$ | $S_2$, $S_3$ to $Q_n$ | 1.10 | 2.50 | 1.10 | 2.50 | 1.10 | 2.80 | ns | |
| $t_{TLH}$ | Transition time | 0.45 | 1.60 | 0.45 | 1.60 | 0.45 | 1.60 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.60 | 0.45 | 1.60 | 0.45 | 1.60 | ns | |

**Flat Pack** $V_{CC1} = V_{CC2} =$ GND, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 0.80 | 2.00 | 0.90 | 2.15 | 0.90 | 2.35 | ns | Figs. 5, 6, 7 |
| $t_{PHL}$ | $D_n$ to $Q_n$ | 0.80 | 2.00 | 0.90 | 2.15 | 0.90 | 2.35 | ns | |
| $t_{PLH}$ | Propagation delay | 1.45 | 3.00 | 1.45 | 3.00 | 1.45 | 3.40 | ns | |
| $t_{PHL}$ | $S_0$, $S_1$ to $Q_n$ | 1.45 | 3.00 | 1.45 | 3.00 | 1.45 | 3.40 | ns | |
| $t_{PLH}$ | Propagation delay | 1.10 | 2.30 | 1.10 | 2.30 | 1.10 | 2.60 | ns | |
| $t_{PHL}$ | $S_2$, $S_3$ to $Q_n$ | 1.10 | 2.30 | 1.10 | 2.30 | 1.10 | 2.60 | ns | |
| $t_{TLH}$ | Transition time | 0.45 | 1.60 | 0.45 | 1.60 | 0.45 | 1.60 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.60 | 0.45 | 1.60 | 0.45 | 1.60 | ns | |

## AC ELECTRICAL CHARACTERISTICS

**Flat Pack** $V_{CC1} = V_{CC2} = \text{GND}$, $V_{EE} = -5.2\text{V} \pm 5\%$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 0.80 | 2.00 | 0.90 | 2.15 | 0.90 | 2.35 | ns | Figs. 5, 6, 7 |
| $t_{PHL}$ | $D_n$ to $Q_n$ | 0.80 | 2.00 | 0.90 | 2.15 | 0.90 | 2.35 | ns | |
| $t_{PLH}$ | Propagation delay | 1.45 | 3.00 | 1.45 | 3.00 | 1.45 | 3.40 | ns | |
| $t_{PHL}$ | $S_0$, $S_1$ to $Q_n$ | 1.45 | 3.00 | 1.45 | 3.00 | 1.45 | 3.40 | ns | |
| $t_{PLH}$ | Propagation delay | 1.10 | 2.30 | 1.10 | 2.30 | 1.10 | 2.60 | ns | |
| $t_{PHL}$ | $S_2$, $S_3$ to $Q_n$ | 1.10 | 2.30 | 1.10 | 2.30 | 1.10 | 2.60 | ns | |
| $t_{TLH}$ | Transition time | 0.45 | 1.60 | 0.45 | 1.60 | 0.45 | 1.60 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.60 | 0.45 | 1.60 | 0.45 | 1.60 | ns | |

## AC WAVEFORMS

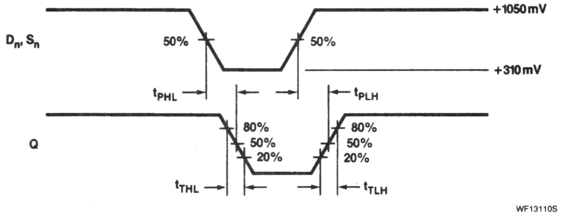
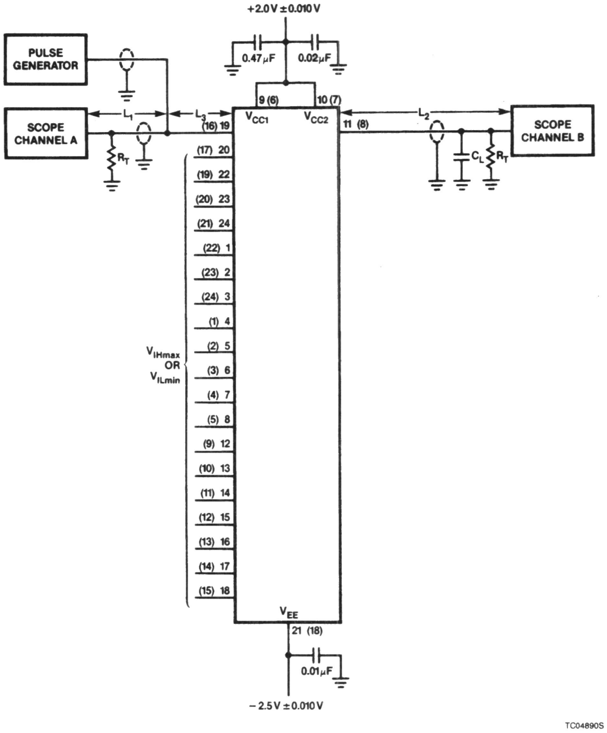


Figure 5. Propagation Delay and Transition Times

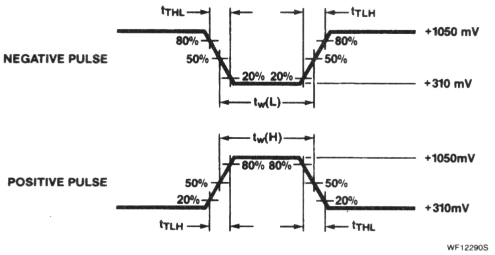
## TEST CIRCUITS AND WAVEFORMS


+2.0V ±0.010V
0.47μF
0.02μF
PULSE GENERATOR
SCOPE CHANNEL A
L1
L3
R_T
9 (6)
10 (7)
V_CC1
V_CC2
11 (8)
L2
SCOPE CHANNEL B
C_L
R_T
(16) 19
(17) 20
(19) 22
(20) 23
(21) 24
(22) 1
(23) 2
(24) 3
(1) 4
(2) 5
(3) 6
(4) 7
(5) 8
(9) 12
(10) 13
(11) 14
(12) 15
(13) 16
(14) 17
(15) 18
V_IHmax OR V_ILmin
V_EE
21 (18)
0.01μF
−2.5V ±0.010V
TC04890S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1μF and 25μF from GND to $V_{CC}$, 0.01μF and 25μF from GND to $V_{EE}$. (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance ≤3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ±1% or better.
11. Pin connections are for Flat Pack and in parentheses for Ceramic DIP.

Figure 6. Test Circuit


t_THL
t_TLH
NEGATIVE PULSE
80%
50%
20% 20%
80%
50%
t_w(L)
+1050 mV
+310 mV
t_w(H)
POSITIVE PULSE
80% 80%
50%
20%
50%
20%
t_TLH
t_THL
+1050mV
+310mV
WF12290S

| INPUT PULSE REQUIREMENTS<br>$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -2.5V \pm 0.010V$, $V_T$ = GND (0V) | | | | | |
|---|---|---|---|---|---|
| **Family** | **Amplitude** | **Rep Rate** | **Pulse Width** | **$t_{TLH}$** | **$t_{THL}$** |
| 100K ECL | 740mVp-p | 1MHz | 500ns | 0.7 ±0.1ns | 0.7 ±0.1ns |

Figure 7. Input Pulse Definition

Signetics

# 100165
# Encoder

**Universal Priority Encoder**
***Product Specification***

**ECL Products**

## DESCRIPTION

The 100165 operates as a Dual 4-Input Decoder, or as a Single 8-Input Decoder; the operating mode is fixed by the mode control input. The circuit contains eight latch inputs with a common enable ($\overline{E}$) and generates the binary address (Q) of the highest priority input, having a HIGH signal and a relevant group signal output (GS). A HIGH level on the output enable input ($\overline{OE}$) forces all $Q_n$ outputs LOW and all $GS_n$ outputs HIGH. The GS output of a higher priority group and the $\overline{OE}$ input of the next lower priority group can be tied together to accomodate more inputs.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 100165 | 2.50ns | 125mA |

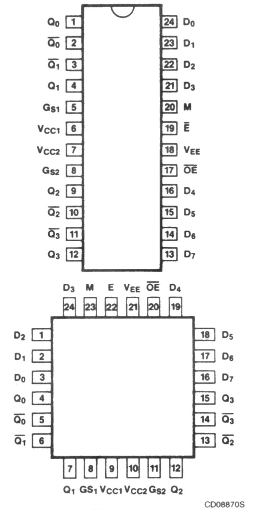
## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} = GND$; $V_{EE} = -4.2V$ to $-4.8V$<br>$T_A = 0°C$ to $+85°C$ |
|---|---|
| Ceramic DIP | 100165F |
| Ceramic Flat Pack | 100165Y |

## PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_0 - D_7$ | Data Inputs |
| M | Mode Control Input |
| $\overline{E}$ | Enable Input (Active LOW) |
| $\overline{OE}$ | Output Enable Input (Active LOW) |
| $GS_1$, $GS_2$ | Group Signal Outputs |
| $Q_0 - Q_3$ | Data Outputs |
| $\overline{Q}_0 - \overline{Q}_3$ | Data Outputs |

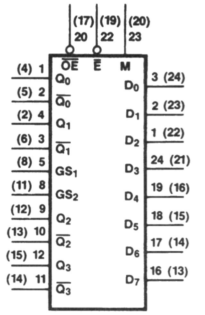
## PIN CONFIGURATION



Q0 1
Q̄0 2
Q̄1 3
Q1 4
GS1 5
VCC1 6
VCC2 7
GS2 8
Q2 9
Q̄2 10
Q̄3 11
Q3 12
24 D0
23 D1
22 D2
21 D3
20 M
19 Ē
18 VEE
17 OE
16 D4
15 D5
14 D6
13 D7
D3 M E VEE OE D4
24 23 22 21 20 19
D2 1
D1 2
D0 3
Q0 4
Q̄0 5
Q̄1 6
18 D5
17 D6
16 D7
15 Q3
14 Q̄3
13 Q̄2
7 8 9 10 11 12
Q1 GS1 VCC1 VCC2 GS2 Q2
CD08870S

Figure 1

## LOGIC SYMBOL



(17) 20
(19) 22
(20) 23
OE
E
M
(4) 1 Q0
(5) 2 Q̄0
(2) 4 Q1
(6) 3 Q̄1
(8) 5 GS1
(11) 8 GS2
(12) 9 Q2
(13) 10 Q̄2
(15) 12 Q3
(14) 11 Q̄3
D0 3 (24)
D1 2 (23)
D2 1 (22)
D3 24 (21)
D4 19 (16)
D5 18 (15)
D6 17 (14)
D7 16 (13)

$V_{CC1}$ = 9 (11)
$V_{CC2}$ = 10 (7)
$V_{EE}$ = 21 (18)

LS10620S

Figure 2

## ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | 100K ECL | UNIT |
|---|---|---|---|
| $V_{EE}$ | Supply voltage ($V_{CC1} = V_{CC2}$ = GND) | −7.0 to 0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | $V_{EE}$ to +0.5 | V |
| $I_O$ | Output source current | −55 | mA |
| $T_S$ | Storage temperature | −65 to +150 | °C |
| $T_J$ | Maximum junction temperature | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | | 100K ECL | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | −4.2 | −4.5 | −4.8 | V |
| $V_{EE}$ | Supply voltage (negative) when operating with 10K ECL family | | | | | −5.7 | V |
| $V_{IH}$ | HIGH level input voltage | $V_{CC1} = V_{CC2}$ = GND<br>$T_A$ = 0°C to +85°C | $V_{EE} = -4.2V$ | −1150 | | −880 | mV |
| | | | $V_{EE} = -4.5V$ | −1165 | | | |
| | | | $V_{EE} = -4.8V$ | | | | |
| $V_{IHT}$ | HIGH level input threshold voltage | | $V_{EE} = -4.2V$ | −1150 | | | mV |
| | | | $V_{EE} = -4.5V$ | −1165 | | | mV |
| | | | $V_{EE} = -4.8V$ | | | | |
| $V_{ILT}$ | LOW level input threshold voltage | | $V_{EE} = -4.2V$ | | | −1475 | mV |
| | | | $V_{EE} = -4.5V$ | | | | |
| | | | $V_{EE} = -4.8V$ | | | −1490 | mV |
| $V_{IL}$ | LOW level input voltage | | $V_{EE} = -4.2V$ | −1810 | | −1475 | mV |
| | | | $V_{EE} = -4.5V$ | | | | |
| | | | $V_{EE} = -4.8V$ | | | −1490 | |
| $T_A$ | Operating ambient temperature | | | 0 | +25 | +85 | °C |

**NOTE:**
When operating at other than specified voltages (−4.2V, −4.5V, −4.8V) DC & AC Characteristics will vary slightly from specified values.

## Encoder

## 100165

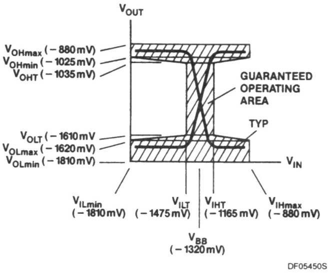
**DC ELECTRICAL CHARACTERISTICS** $V_{CC1} = V_{CC2} = \text{GND}$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$, $T_A = 0°C$ to $+85°C$ unless otherwise specified[1,3]

| PARAMETER | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] | |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | $V_{EE} = -4.2V$ | -1025 | | -870 | mV | $V_{IN} = V_{IHmax}$<br>or<br>$V_{IN} = V_{ILmin}$ | Loading with 50Ω to -2.0V ±0.010V |
| | | $V_{EE} = -4.5V$ | -1025 | -955 | -880 | mV | | |
| | | $V_{EE} = -4.8V$ | -1035 | | -880 | mV | | |
| $V_{OHT}$ | HIGH level output threshold voltage | $V_{EE} = -4.2V$ | -1035 | | | mV | $V_{IN} = V_{IHmin}$<br>or<br>$V_{IN} = V_{ILmax}$ | |
| | | $V_{EE} = -4.5V$ | -1035 | | | mV | | |
| | | $V_{EE} = -4.8V$ | -1045 | | | mV | | |
| $V_{OLT}$ | LOW level output threshold voltage | $V_{EE} = -4.2V$ | | | -1590 | mV | $V_{IN} = V_{IHmin}$<br>or<br>$V_{IN} = V_{ILmax}$ | |
| | | $V_{EE} = -4.5V$ | | | -1610 | mV | | |
| | | $V_{EE} = -4.8V$ | | | -1610 | mV | | |
| $V_{OL}$ | LOW level output voltage | $V_{EE} = -4.2V$ | -1810 | | -1600 | mV | $V_{IN} = V_{IHmax}$<br>or<br>$V_{IN} = V_{ILmin}$ | |
| | | $V_{EE} = -4.5V$ | -1810 | -1705 | -1620 | mV | | |
| | | $V_{EE} = -4.8V$ | -1830 | | -1620 | mV | | |
| $I_{IH}$ | HIGH level input current | | | | 230 | µA | $V_{IN} = V_{IHmax}$ | |
| $I_{IL}$ | LOW level input current | | 0.5 | | | µA | $V_{IN} = V_{ILmin}$ | |
| $-I_{EE}$ | $V_{EE}$ supply current | | 77 | 125 | 200 | mA | Inputs open | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | $V_{EE} = -4.2V$<br>$T_A = +25°C$ | | | 0.025 | V/V | | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | | 0.050 | V/V | | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 3.

# Encoder 100165



**NOTES:**

$V_{IHmax}$ – Maximum HIGH level input voltage (the most positive $V_{IH}$).
$V_{IHT}$ – HIGH level input threshold voltage.
$V_{ILT}$ – LOW level input threshold voltage.
$V_{ILmin}$ – Minimum LOW level input voltage (the most negative $V_{IL}$).
$V_{OHmax}$ – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition.
$V_{OHmin}$ – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition.
$V_{OHT}$ – HIGH level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLT}$ – LOW level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLmax}$ – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions.
$V_{OLmin}$ – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions.
$V_{BB}$ – Reference bias voltage. The internally generated reference voltage which is used to set the input and output threshold level.

**Figure 3. Transfer Characteristics**

## AC ELECTRICAL CHARACTERISTICS

**Ceramic DIP** $V_{CC1} = V_{CC2} = \text{GND}$, $V_{EE} = -4.2\text{V} \pm 0.010\text{V}$ to $-4.8\text{V} \pm 0.010\text{V}$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 1.10 | 4.10 | 1.10 | 4.10 | 1.10 | 4.60 | ns | Fig. 5, 7, 8 |
| $t_{PHL}$ | $D_n$ to $Q_n$, $\overline{Q}_n$ | 1.10 | 4.10 | 1.10 | 4.10 | 1.10 | 4.60 | ns | |
| $t_{PLH}$ | Propagation delay | 1.10 | 4.10 | 1.10 | 4.10 | 1.10 | 4.60 | ns | |
| $t_{PHL}$ | $D_n$ to GS | 1.10 | 4.10 | 1.10 | 4.10 | 1.10 | 4.60 | ns | |
| $t_{PLH}$ | Propagation delay | 1.00 | 3.30 | 1.00 | 3.30 | 1.00 | 3.40 | ns | Figs. 4, 7, 8 |
| $t_{PHL}$ | $\overline{OE}$ to $Q_n$, $\overline{Q}_n$ | 1.00 | 3.30 | 1.00 | 3.30 | 1.00 | 3.40 | ns | |
| $t_{PLH}$ | Propagation delay | 1.00 | 3.30 | 1.00 | 3.30 | 1.00 | 3.40 | ns | |
| $t_{PHL}$ | $\overline{OE}$ to GS | 1.00 | 3.30 | 1.00 | 3.30 | 1.00 | 3.40 | ns | |
| $t_{PLH}$ | Propagation delay | 0.90 | 3.60 | 1.00 | 3.60 | 1.00 | 3.80 | ns | |
| $t_{PHL}$ | M to $Q_n$, $\overline{Q}_n$, GS | 0.90 | 3.60 | 1.00 | 3.60 | 1.00 | 3.80 | ns | |
| $t_{PLH}$ | Propagation delay | 1.40 | 4.70 | 1.40 | 4.60 | 1.40 | 5.00 | ns | Figs. 6, 7, 8 |
| $t_{PHL}$ | $\overline{E}$ to $Q_n$, $\overline{Q}_n$, GS | 1.40 | 4.70 | 1.40 | 4.60 | 1.40 | 5.00 | ns | |
| $t_{TLH}$ | Transition time | 0.45 | 1.40 | 0.45 | 1.40 | 0.45 | 1.40 | ns | Figs. 5, 6, 7, 8 |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.40 | 0.45 | 1.40 | 0.45 | 1.40 | ns | |
| $t_s$ | Setup time $D_n$ to $\overline{E}$ | 1.10 | | 1.00 | | 1.10 | | ns | Figs. 6, 8 |
| $t_h$ | Hold time $D_n$ to $\overline{E}$ | 1.30 | | 1.30 | | 1.30 | | ns | |

## AC ELECTRICAL CHARACTERISTICS

**Ceramic DIP** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V \pm 5\%$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 1.10 | 4.10 | 1.10 | 4.10 | 1.10 | 4.60 | ns | Fig. 5, 7, 8 |
| $t_{PHL}$ | $D_n$ to $Q_n$, $\overline{Q}_n$ | 1.10 | 4.10 | 1.10 | 4.10 | 1.10 | 4.60 | ns | |
| $t_{PLH}$ | Propagation delay | 1.10 | 4.10 | 1.10 | 4.10 | 1.10 | 4.60 | ns | |
| $t_{PHL}$ | $D_n$ to GS | 1.10 | 4.10 | 1.10 | 4.10 | 1.10 | 4.60 | ns | |
| $t_{PLH}$ | Propagation delay | 1.00 | 3.30 | 1.00 | 3.30 | 1.00 | 3.40 | ns | Figs. 4, 7, 8 |
| $t_{PHL}$ | $\overline{OE}$ to $Q_n$, $\overline{Q}_n$ | 1.00 | 3.30 | 1.00 | 3.30 | 1.00 | 3.40 | ns | |
| $t_{PLH}$ | Propagation delay | 1.00 | 3.30 | 1.00 | 3.30 | 1.00 | 3.40 | ns | |
| $t_{PHL}$ | $\overline{OE}$ to GS | 1.00 | 3.30 | 1.00 | 3.30 | 1.00 | 3.40 | ns | |
| $t_{PLH}$ | Propagation delay | 0.90 | 3.60 | 1.00 | 3.60 | 1.00 | 3.80 | ns | |
| $t_{PHL}$ | M to $Q_n$, $\overline{Q}_n$, GS | 0.90 | 3.60 | 1.00 | 3.60 | 1.00 | 3.80 | ns | |
| $t_{PLH}$ | Propagation delay | 1.40 | 4.70 | 1.40 | 4.60 | 1.40 | 5.00 | ns | Figs. 6, 7, 8 |
| $t_{PHL}$ | $\overline{E}$ to $Q_n$, $\overline{Q}_n$, GS | 1.40 | 4.70 | 1.40 | 4.60 | 1.40 | 5.00 | ns | |
| $t_{TLH}$ | Transition time | 0.45 | 1.40 | 0.45 | 1.40 | 0.45 | 1.40 | ns | Figs. 5, 6, 7, 8 |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.40 | 0.45 | 1.40 | 0.45 | 1.40 | ns | |
| $t_s$ | Setup time $D_n$ to $\overline{E}$ | 1.10 | | 1.00 | | 1.10 | | ns | Figs. 6, 8 |
| $t_h$ | Hold time $D_n$ to $\overline{E}$ | 1.30 | | 1.30 | | 1.30 | | ns | |

**Flat Pack** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 1.10 | 3.90 | 1.10 | 3.90 | 1.10 | 4.40 | ns | Figs. 5, 7, 8 |
| $t_{PHL}$ | $D_n$ to $Q_n$, $\overline{Q}_n$ | 1.10 | 3.90 | 1.10 | 3.90 | 1.10 | 4.40 | ns | |
| $t_{PLH}$ | Propagation delay | 1.10 | 3.90 | 1.10 | 3.90 | 1.10 | 4.40 | ns | |
| $t_{PHL}$ | $D_n$ to GS | 1.10 | 3.90 | 1.10 | 3.90 | 1.10 | 4.40 | ns | |
| $t_{PLH}$ | Propagation delay | 1.00 | 3.10 | 1.00 | 3.10 | 1.00 | 3.20 | ns | Figs. 4, 7, 8 |
| $t_{PHL}$ | $\overline{OE}$ to $Q_n$, $\overline{Q}_n$ | 1.00 | 3.10 | 1.00 | 3.10 | 1.00 | 3.20 | ns | |
| $t_{PLH}$ | Propagation delay | 1.00 | 3.10 | 1.00 | 3.10 | 1.00 | 3.20 | ns | |
| $t_{PHL}$ | $\overline{OE}$ to GS | 1.00 | 3.10 | 1.00 | 3.10 | 1.00 | 3.20 | ns | |
| $t_{PLH}$ | Propagation delay | 0.90 | 3.40 | 1.00 | 3.40 | 1.00 | 3.60 | ns | |
| $t_{PHL}$ | M to $Q_n$, $\overline{Q}_n$, GS | 0.90 | 3.40 | 1.00 | 3.40 | 1.00 | 3.60 | ns | |
| $t_{PLH}$ | Propagation delay | 1.40 | 4.50 | 1.40 | 4.40 | 1.40 | 4.80 | ns | Figs. 6, 7, 8 |
| $t_{PHL}$ | $\overline{E}$ to $Q_n$, $\overline{Q}_n$, GS | 1.40 | 4.50 | 1.40 | 4.40 | 1.40 | 4.80 | ns | |
| $t_{TLH}$ | Transition time | 0.45 | 1.40 | 0.45 | 1.40 | 0.45 | 1.40 | ns | Figs. 5, 6, 7, 8 |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.40 | 0.45 | 1.40 | 0.45 | 1.40 | ns | |
| $t_s$ | Setup time $D_n$ to $\overline{E}$ | 0.90 | | 0.80 | | 0.90 | | ns | Figs. 6, 8 |
| $t_h$ | Hold time $D_n$ to $\overline{E}$ | 1.10 | | 1.10 | | 1.10 | | ns | |

# Encoder

# 100165

## AC ELECTRICAL CHARACTERISTICS

**Flat Pack** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V \pm 5\%$

| | PARAMETER | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 1.10 | 3.90 | 1.10 | 3.90 | 1.10 | 4.40 | ns | Figs. 5, 7, 8 |
| $t_{PHL}$ | $D_n$ to $Q_n$, $\overline{Q}_n$ | 1.10 | 3.90 | 1.10 | 3.90 | 1.10 | 4.40 | ns | |
| $t_{PLH}$ | Propagation delay | 1.10 | 3.90 | 1.10 | 3.90 | 1.10 | 4.40 | ns | |
| $t_{PHL}$ | $D_n$ to GS | 1.10 | 3.90 | 1.10 | 3.90 | 1.10 | 4.40 | ns | |
| $t_{PLH}$ | Propagation delay | 1.00 | 3.10 | 1.00 | 3.10 | 1.00 | 3.20 | ns | Figs. 4, 7, 8 |
| $t_{PHL}$ | $\overline{OE}$ to $Q_n$, $\overline{Q}_n$ | 1.00 | 3.10 | 1.00 | 3.10 | 1.00 | 3.20 | ns | |
| $t_{PLH}$ | Propagation delay | 1.00 | 3.10 | 1.00 | 3.10 | 1.00 | 3.20 | ns | |
| $t_{PHL}$ | $\overline{OE}$ to GS | 1.00 | 3.10 | 1.00 | 3.10 | 1.00 | 3.20 | ns | |
| $t_{PLH}$ | Propagation delay | 0.90 | 3.40 | 1.00 | 3.40 | 1.00 | 3.60 | ns | |
| $t_{PHL}$ | M to $Q_n$, $\overline{Q}_n$, GS | 0.90 | 3.40 | 1.00 | 3.40 | 1.00 | 3.60 | ns | |
| $t_{PLH}$ | Propagation delay | 1.40 | 4.50 | 1.40 | 4.40 | 1.40 | 4.80 | ns | Figs. 6, 7, 8 |
| $t_{PHL}$ | $\overline{E}$ to $Q_n$, $\overline{Q}_n$, GS | 1.40 | 4.50 | 1.40 | 4.40 | 1.40 | 4.80 | ns | |
| $t_{TLH}$ | Transition time | 0.45 | 1.40 | 0.45 | 1.40 | 0.45 | 1.40 | ns | Figs. 5, 6, 7, 8 |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.40 | 0.45 | 1.40 | 0.45 | 1.40 | ns | |
| $t_s$ | Setup time $D_n$ to $\overline{E}$ | 0.90 | | 0.80 | | 0.90 | | ns | Figs. 6, 8 |
| $t_h$ | Hold time $D_n$ to $\overline{E}$ | 1.10 | | 1.10 | | 1.10 | | ns | |

## AC WAVEFORMS

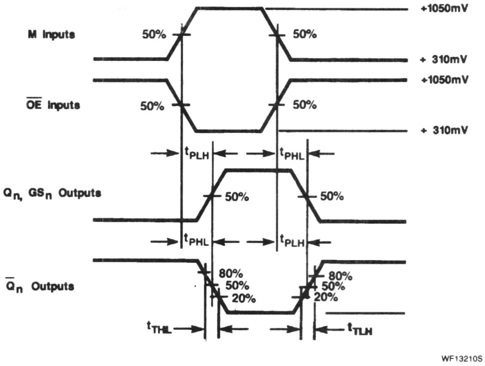

+1050mV
M Inputs
50%
50%
+ 310mV
+1050mV
$\overline{OE}$ Inputs
50%
50%
+ 310mV
$t_{PLH}$
$t_{PHL}$
$Q_n$, $GS_n$ Outputs
50%
50%
$t_{PHL}$
$t_{PLH}$
$\overline{Q}_n$ Outputs
80%
50%
20%
80%
50%
20%
$t_{THL}$
$t_{TLH}$
WF13210S

**Figure 4. Propagation Delay and Transition Times**

## Encoder

## 100165

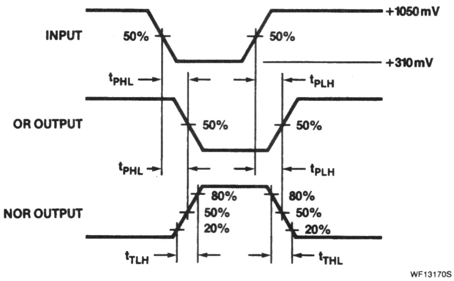

INPUT
50%
50%
+1050mV
+310mV
$t_{PHL}$
$t_{PLH}$
OR OUTPUT
50%
50%
$t_{PHL}$
$t_{PLH}$
NOR OUTPUT
80%
50%
20%
80%
50%
20%
$t_{TLH}$
$t_{THL}$
WF13170S

Figure 5. Enable Timing

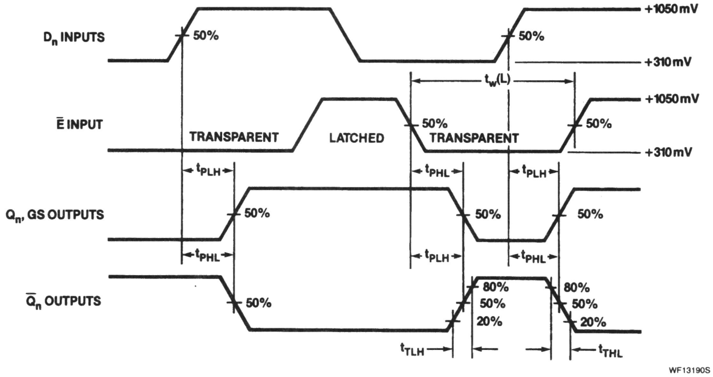
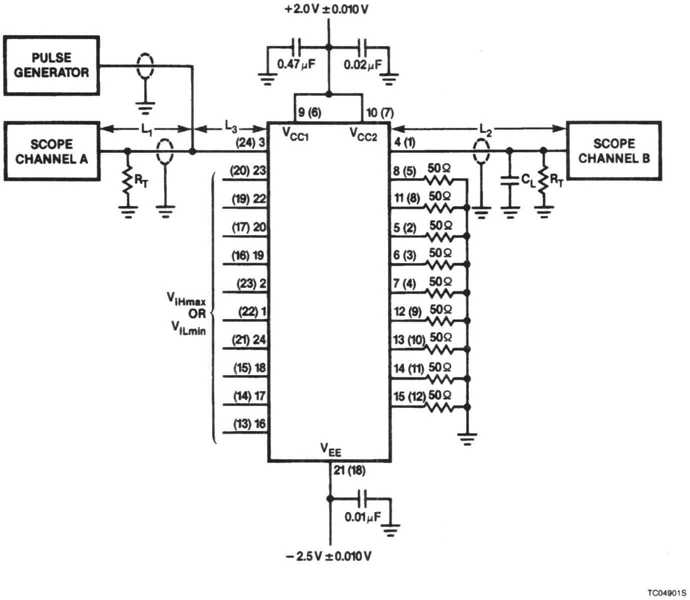

$D_n$ INPUTS
50%
50%
+1050mV
+310mV
$t_w(L)$
$\bar{E}$ INPUT
TRANSPARENT
LATCHED
50%
TRANSPARENT
50%
+1050mV
+310mV
$t_{PLH}$
$t_{PHL}$
$t_{PLH}$
$Q_n$, GS OUTPUTS
50%
50%
50%
$t_{PHL}$
$t_{PLH}$
$t_{PHL}$
$\bar{Q}_n$ OUTPUTS
50%
80%
50%
20%
80%
50%
20%
$t_{TLH}$
$t_{THL}$
WF13190S

Figure 6. Setup and Hold Times

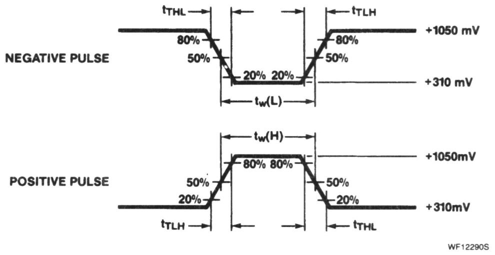
## TEST CIRCUITS AND WAVEFORMS


+2.0V ±0.010V
0.47µF
0.02µF
PULSE GENERATOR
SCOPE CHANNEL A
$L_1$
$L_3$
$R_T$
9 (6)
10 (7)
$V_{CC1}$
$V_{CC2}$
(24) 3
(20) 23
(19) 22
(17) 20
(16) 19
(23) 2
(22) 1
(21) 24
(15) 18
(14) 17
(13) 16
$V_{IHmax}$ OR $V_{ILmin}$
4 (1)
8 (5) 50Ω
11 (8) 50Ω
5 (2) 50Ω
6 (3) 50Ω
7 (4) 50Ω
12 (9) 50Ω
13 (10) 50Ω
14 (11) 50Ω
15 (12) 50Ω
$L_2$
$C_L$
$R_T$
SCOPE CHANNEL B
$V_{EE}$
21 (18)
0.01µF
−2.5V ±0.010V
TC04901S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1µF and 25µF from GND to $V_{CC}$, 0.01µF and 25µF from GND to $V_{EE}$. (0.01 and 0.1µF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T = 50\Omega$ terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance $\leqslant$ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ±1% or better.
11. Pin connections are for Flat Pack and in parentheses for Ceramic DIP.

Figure 7. Test Circuit


NEGATIVE PULSE
$t_{THL}$
$t_{TLH}$
80%
50%
20%
20%
80%
50%
$t_w(L)$
+1050 mV
+310 mV
POSITIVE PULSE
$t_w(H)$
80%
80%
50%
20%
50%
20%
$t_{TLH}$
$t_{THL}$
+1050mV
+310mV
WF12290S

| INPUT PULSE REQUIREMENTS<br>$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -2.5V \pm 0.010V$, $V_T$ = GND (0V) | | | | | |
|---|---|---|---|---|---|
| Family | Amplitude | Rep Rate | Pulse Width | $t_{TLH}$ | $t_{THL}$ |
| 100K ECL | 740mVp-p | 1MHz | 500ns | 0.7 ±0.1ns | 0.7 ±0.1ns |

Figure 8. Input Pulse Definition

**Signetics**

# 100166
# Comparator

**9-Bit Comparator**
***Product Specification***

**ECL Products**

## DESCRIPTION

The 100166 is a 9-bit Comparator which compares the arithmetic values of two 9-bit words and indicates whether one word is greater or equal to the other one.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 100166 | 2.3ns | 140mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC1} = V_{CC2} = \text{GND}$; $V_{EE} = -4.2V$ to $-4.8V$ $T_A = 0°C$ to $+85°C$ |
|---|---|
| Ceramic DIP | 100166F |
| Ceramic Flat Pack | 100166Y |

## PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $A_0 - A_8$ | A Data Inputs |
| $B_0 - B_8$ | B Data Inputs |
| $A > B$ | A Greater Than B Outputs |
| $A < B$ | B Greater Than A Outputs |
| $\overline{A} = \overline{B}$ | Complement A Equal To B Output (Active LOW) |

## PIN CONFIGURATION

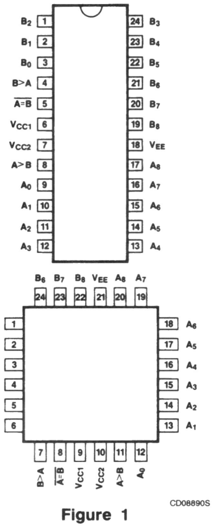

B2 1
B1 2
B0 3
B>A 4
A=B 5
VCC1 6
VCC2 7
A>B 8
A0 9
A1 10
A2 11
A3 12
24 B3
23 B4
22 B5
21 B6
20 B7
19 B8
18 VEE
17 A8
16 A7
15 A6
14 A5
13 A4
B6 24
B7 23
B8 22
VEE 21
A8 20
A7 19
B5 1
B4 2
B3 3
B2 4
B1 5
B0 6
18 A6
17 A5
16 A4
15 A3
14 A2
13 A1
7 B>A
8 A=B
9 VCC1
10 VCC2
11 A>B
12 A0
CD08890S

**Figure 1**

## LOGIC SYMBOL

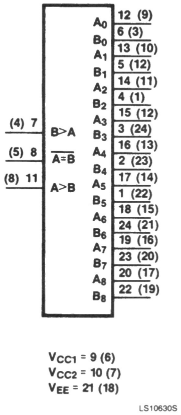

A0 12 (9)
B0 6 (3)
A1 13 (10)
B1 5 (12)
A2 14 (11)
B2 4 (1)
A3 15 (12)
B3 3 (24)
A4 16 (13)
B4 2 (23)
A5 17 (14)
B5 1 (22)
A6 18 (15)
B6 24 (21)
A7 19 (16)
B7 23 (20)
A8 20 (17)
B8 22 (19)
(4) 7 B>A
(5) 8 A=B
(8) 11 A>B
VCC1 = 9 (6)
VCC2 = 10 (7)
VEE = 21 (18)
LS10630S

**Figure 2**

# Comparator 100166

## LOGIC DIAGRAM

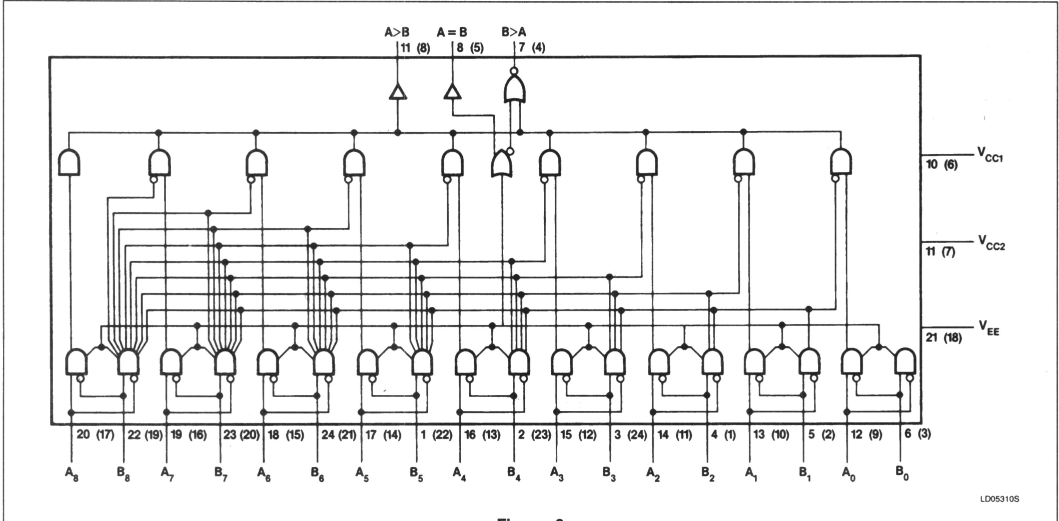

A>B
11 (8)
A = B
8 (5)
B>A
7 (4)
10 (6)
$V_{CC1}$
11 (7)
$V_{CC2}$
21 (18)
$V_{EE}$
20 (17)
22 (19)
19 (16)
23 (20)
18 (15)
24 (21)
17 (14)
1 (22)
16 (13)
2 (23)
15 (12)
3 (24)
14 (11)
4 (1)
13 (10)
5 (2)
12 (9)
6 (3)
$A_8$
$B_8$
$A_7$
$B_7$
$A_6$
$B_6$
$A_5$
$B_5$
$A_4$
$B_4$
$A_3$
$B_3$
$A_2$
$B_2$
$A_1$
$B_1$
$A_0$
$B_0$
LD05310S

Figure 3

## FUNCTION TABLE

| INPUTS | | | | | | | | | OUTPUTS | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $A_0B_0$ | $A_1B_1$ | $A_2B_2$ | $A_3B_3$ | $A_4B_4$ | $A_5B_5$ | $A_6B_6$ | $A_7B_7$ | $A_8B_8$ | A < B | B > A | A = B |
| | | | | | | | | H L | H | L | H |
| | | | | | | | | L H | L | H | H |
| | | | | | | | H L | $A_8 = A_8$ | H | L | H |
| | | | | | | | L H | $A_8 = A_8$ | L | H | H |
| | | | | | | H L | $A_7 = A_7$ | $A_8 = A_8$ | H | L | H |
| | | | | | | L H | $A_7 = A_7$ | $A_8 = A_8$ | L | H | H |
| | | | | | H L | $A_6 = A_6$ | $A_7 = A_7$ | $A_8 = A_8$ | H | L | H |
| | | | | | L H | $A_6 = A_6$ | $A_7 = A_7$ | $A_8 = A_8$ | L | H | H |
| | | | | H L | $A_5 = A_5$ | $A_6 = A_6$ | $A_7 = A_7$ | $A_8 = A_8$ | H | L | H |
| | | | | L H | $A_5 = A_5$ | $A_6 = A_6$ | $A_7 = A_7$ | $A_8 = A_8$ | L | H | H |
| | | | H L | $A_4 = A_4$ | $A_5 = A_5$ | $A_6 = A_6$ | $A_7 = A_7$ | $A_8 = A_8$ | H | L | H |
| | | | L H | $A_4 = A_4$ | $A_5 = A_5$ | $A_6 = A_6$ | $A_7 = A_7$ | $A_8 = A_8$ | L | H | H |
| | | H L | $A_3 = A_3$ | $A_4 = A_4$ | $A_5 = A_5$ | $A_6 = A_6$ | $A_7 = A_7$ | $A_8 = A_8$ | H | L | H |
| | | L H | $A_3 = A_3$ | $A_4 = A_4$ | $A_5 = A_5$ | $A_6 = A_6$ | $A_7 = A_7$ | $A_8 = A_8$ | L | H | H |
| | H L | $A_2 = A_2$ | $A_3 = A_3$ | $A_4 = A_4$ | $A_5 = A_5$ | $A_6 = A_6$ | $A_7 = A_7$ | $A_8 = A_8$ | H | L | H |
| | L H | $A_2 = A_2$ | $A_3 = A_3$ | $A_4 = A_4$ | $A_5 = A_5$ | $A_6 = A_6$ | $A_7 = A_7$ | $A_8 = A_8$ | L | H | H |
| H L | $A_1 = A_1$ | $A_2 = A_2$ | $A_3 = A_3$ | $A_4 = A_4$ | $A_5 = A_5$ | $A_6 = A_6$ | $A_7 = A_7$ | $A_8 = A_8$ | H | L | H |
| L H | $A_1 = A_1$ | $A_2 = A_2$ | $A_3 = A_3$ | $A_4 = A_4$ | $A_5 = A_5$ | $A_6 = A_6$ | $A_7 = A_7$ | $A_8 = A_8$ | L | H | H |
| $A_0 = A_0$ | $A_1 = A_1$ | $A_2 = A_2$ | $A_3 = A_3$ | $A_4 = A_4$ | $A_5 = A_5$ | $A_6 = A_6$ | $A_7 = A_7$ | $A_8 = A_8$ | L | L | L |

Positive Logic:
H = HIGH state (the more positive voltage) = 1
L = LOW state (the less positive voltage) = 0
Blank = Don't Care

# Comparator

# 100166

## ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | 100K ECL | UNIT |
|---|---|---|---|
| $V_{EE}$ | Supply voltage ($V_{CC1} = V_{CC2} =$ GND) | −7.0 to 0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | $V_{EE}$ to +0.5 | V |
| $I_O$ | Output source current | −55 | mA |
| $T_S$ | Storage temperature | −65 to +150 | °C |
| $T_J$ | Maximum junction temperature | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | | 100K ECL | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | −4.2 | −4.5 | −4.8 | V |
| $V_{EE}$ | Supply voltage (negative) when operating with 10K ECL family | | | | | −5.7 | V |
| $V_{IH}$ | HIGH level input voltage | $V_{CC1} = V_{CC2} =$ GND<br>$T_A$ = 0°C to +85°C | $V_{EE} = -4.2V$ | −1150 | | −880 | mV |
| | | | $V_{EE} = -4.5V$ | −1165 | | | |
| | | | $V_{EE} = -4.8V$ | | | | |
| $V_{IHT}$ | HIGH level input threshold voltage | | $V_{EE} = -4.2V$ | −1150 | | | mV |
| | | | $V_{EE} = -4.5V$ | −1165 | | | mV |
| | | | $V_{EE} = -4.8V$ | | | | |
| $V_{ILT}$ | LOW level input threshold voltage | | $V_{EE} = -4.2V$ | | | −1475 | mV |
| | | | $V_{EE} = -4.5V$ | | | | |
| | | | $V_{EE} = -4.8V$ | | | −1490 | mV |
| $V_{IL}$ | LOW level input voltage | | $V_{EE} = -4.2V$ | −1810 | | −1475 | mV |
| | | | $V_{EE} = -4.5V$ | | | | |
| | | | $V_{EE} = -4.8V$ | | | −1490 | |
| $T_A$ | Operating ambient temperature | | | 0 | | +85 | °C |

**NOTE:**
When operating at other than specified voltages (−4.2V, −4.5V, −4.8V) DC & AC Characteristics will vary slightly from specified values.

## Comparator

## 100166

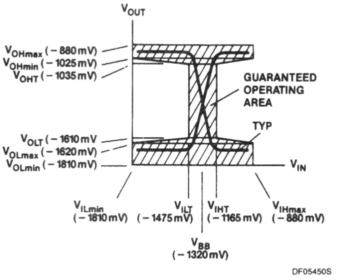
**DC ELECTRICAL CHARACTERISTICS** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$, $T_A = 0°C$ to $+85°C$ unless otherwise specified[1, 3]

| PARAMETER | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] | |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | $V_{EE} = -4.2V$ | -1025 | | -870 | mV | $V_{IN} = V_{IHmax}$ or $V_{IN} = V_{ILmin}$ | Loading with 50Ω to -2.0V ±0.010V |
| | | $V_{EE} = -4.5V$ | -1025 | -955 | -880 | mV | | |
| | | $V_{EE} = -4.8V$ | -1035 | | -880 | mV | | |
| $V_{OHT}$ | HIGH level output threshold voltage | $V_{EE} = -4.2V$ | -1035 | | | mV | $V_{IN} = V_{IHmin}$ or $V_{IN} = V_{ILmax}$ | |
| | | $V_{EE} = -4.5V$ | -1035 | | | mV | | |
| | | $V_{EE} = -4.8V$ | -1045 | | | mV | | |
| $V_{OLT}$ | LOW level output threshold voltage | $V_{EE} = -4.2V$ | | | -1590 | mV | $V_{IN} = V_{IHmin}$ or $V_{IN} = V_{ILmax}$ | |
| | | $V_{EE} = -4.5V$ | | | -1610 | mV | | |
| | | $V_{EE} = -4.8V$ | | | -1610 | mV | | |
| $V_{OL}$ | LOW level output voltage | $V_{EE} = -4.2V$ | -1810 | | -1600 | mV | $V_{IN} = V_{IHmax}$ or $V_{IN} = V_{ILmin}$ | |
| | | $V_{EE} = -4.5V$ | -1810 | -1705 | -1620 | mV | | |
| | | $V_{EE} = -4.8V$ | -1830 | | -1620 | mV | | |
| $I_{IH}$ | HIGH level input current | | | | 250 | µA | $V_{IN} = V_{IHmax}$ | |
| $I_{IL}$ | LOW level input current | | 0.5 | | | µA | $V_{IN} = V_{ILmin}$ | |
| $-I_{EE}$ | $V_{EE}$ supply current | | 119 | 140 | 238 | mA | Inputs open | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | $V_{EE} = -4.2V$<br>$T_A = +25°C$ | | | 0.035 | V/V | | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | | 0.070 | V/V | | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 4.

# Comparator 100166



**NOTES:**

$V_{IHmax}$ – Maximum HIGH level input voltage (the most positive $V_{IH}$).
$V_{IHT}$ – HIGH level input threshold voltage.
$V_{ILT}$ – LOW level input threshold voltage.
$V_{ILmin}$ – Minimum LOW level input voltage (the most negative $V_{IL}$).
$V_{OHmax}$ – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition.
$V_{OHmin}$ – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition.
$V_{OHT}$ – HIGH level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLT}$ – LOW level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLmax}$ – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions.
$V_{OLmin}$ – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions.
$V_{BB}$ – Reference bias voltage. The internally generated reference voltage which is used to set the input and output threshold level.

Figure 4. Transfer Characteristics

## AC ELECTRICAL CHARACTERISTICS

### Ceramic DIP $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 1.40 | 3.50 | 1.40 | 3.50 | 1.40 | 3.90 | ns | Figs. 5, 6, 7 |
| $t_{PHL}$ | $D_n$ to $Q_n$ | 1.40 | 3.50 | 1.40 | 3.50 | 1.40 | 3.90 | ns | |
| $t_{TLH}$ | Transition time | 0.45 | 1.60 | 0.45 | 1.60 | 0.45 | 1.60 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.60 | 0.45 | 1.60 | 0.45 | 1.60 | ns | |

### Ceramic DIP $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V \pm 5\%$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 1.40 | 3.50 | 1.40 | 3.50 | 1.40 | 3.90 | ns | Figs. 5, 6, 7 |
| $t_{PHL}$ | $D_n$ to $Q_n$ | 1.40 | 3.50 | 1.40 | 3.50 | 1.40 | 3.90 | ns | |
| $t_{TLH}$ | Transition time | 0.45 | 1.60 | 0.45 | 1.60 | 0.45 | 1.60 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.60 | 0.45 | 1.60 | 0.45 | 1.60 | ns | |

### Flat Pack $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 1.40 | 3.30 | 1.40 | 3.30 | 1.40 | 3.70 | ns | Figs. 5, 6, 7 |
| $t_{PHL}$ | $D_n$ to $Q_n$ | 1.40 | 3.30 | 1.40 | 3.30 | 1.40 | 3.70 | ns | |
| $t_{TLH}$ | Transition time | 0.45 | 1.60 | 0.45 | 1.60 | 0.45 | 1.60 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.60 | 0.45 | 1.60 | 0.45 | 1.60 | ns | |

### Flat Pack $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V \pm 5\%$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 1.40 | 3.30 | 1.40 | 3.30 | 1.40 | 3.70 | ns | Figs. 5, 6, 7 |
| $t_{PHL}$ | $D_n$ to $Q_n$ | 1.40 | 3.30 | 1.40 | 3.30 | 1.40 | 3.70 | ns | |
| $t_{TLH}$ | Transition time | 0.45 | 1.60 | 0.45 | 1.60 | 0.45 | 1.60 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.60 | 0.45 | 1.60 | 0.45 | 1.60 | ns | |

# Comparator 100166

## AC WAVEFORMS

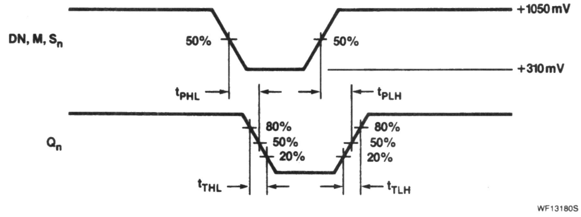
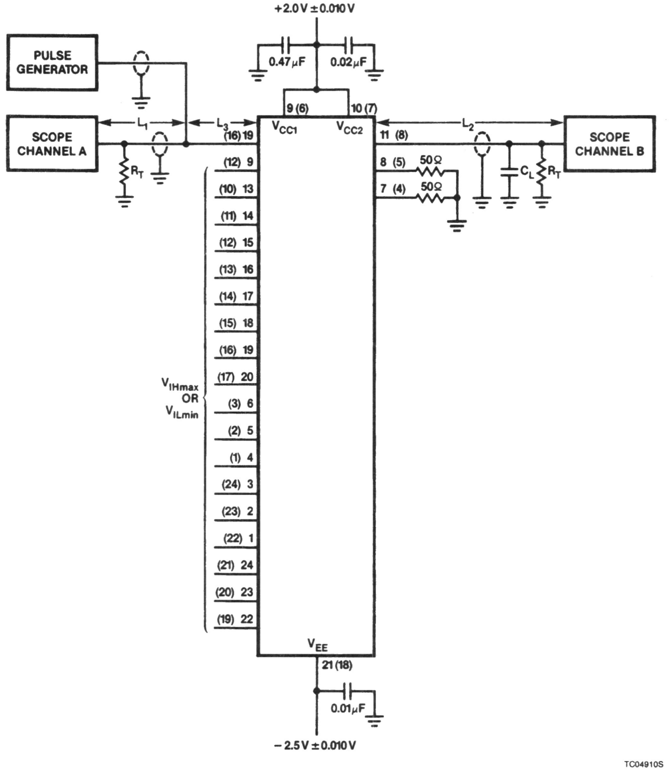

DN, M, S$_n$
+1050mV
+310mV
50%
50%
t$_{PHL}$
t$_{PLH}$
Q$_n$
80%
50%
20%
80%
50%
20%
t$_{THL}$
t$_{TLH}$
WF13180S

Figure 5. Propagation Delay and Transition Times

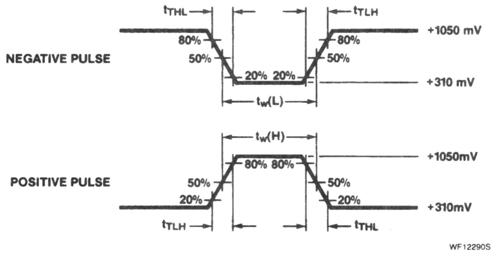
## TEST CIRCUITS AND WAVEFORMS


+2.0V ±0.010V
0.47μF
0.02μF
PULSE GENERATOR
SCOPE CHANNEL A
L$_1$
L$_3$
R$_T$
9 (6)
10 (7)
V$_{CC1}$
V$_{CC2}$
(16) 19
(12) 9
(10) 13
(11) 14
(12) 15
(13) 16
(14) 17
(15) 18
(16) 19
(17) 20
(3) 6
(2) 5
(1) 4
(24) 3
(23) 2
(22) 1
(21) 24
(20) 23
(19) 22
V$_{IHmax}$ OR V$_{ILmin}$
11 (8)
8 (5)
7 (4)
50Ω
50Ω
L$_2$
C$_L$
R$_T$
SCOPE CHANNEL B
V$_{EE}$
21 (18)
0.01μF
−2.5V ±0.010V
TC04910S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1μF and 25μF from GND to $V_{CC}$, 0.01μF and 25μF from GND to $V_{EE}$. (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance $\leqslant$ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.
11. Pin connections are for Flat Pack and in parentheses for Ceramic DIP.

Figure 6. Test Circuit


$t_{THL}$
$t_{TLH}$
+1050 mV
80%
50%
NEGATIVE PULSE
20% 20%
+310 mV
$t_w(L)$
$t_w(H)$
+1050mV
80% 80%
POSITIVE PULSE
50%
20%
+310mV
$t_{TLH}$
$t_{THL}$
WF12290S

| INPUT PULSE REQUIREMENTS<br>$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -2.5V \pm 0.010V$, $V_T = GND$ (0V) | | | | | |
|---|---|---|---|---|---|
| **Family** | **Amplitude** | **Rep Rate** | **Pulse Width** | $t_{TLH}$ | $t_{THL}$ |
| 100K ECL | 740mVp-p | 1MHz | 500ns | 0.7 ±0.1ns | 0.7 ±0.1ns |

Figure 7. Input Pulse Definition

**Signetics**

**ECL Products**

# 100170

# Demultiplexer/Decoder

**Universal Demultiplexer/Decoder**
***Product Specification***

## DESCRIPTION

The 100170 operates as a Dual 1-of-4 Decoder, or as a Single 1-of-8 Decoder; the operating mode is fixed by the mode control input (M). The inputs $H_a$, $H_b$, $H_c$, determine whether the outputs are active LOW or HIGH. In the 1-of-8 mode, the two pairs of active LOW Enables can be tied together (pin 19 to 20 and 22 to 23), to provide two active LOW Enables.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 100170 | 1.8ns | 110mA |

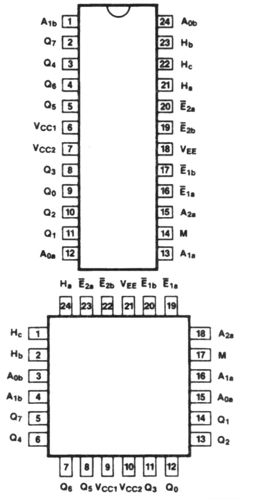
## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} = GND$; $V_{EE} = -4.2V$ to $-4.8V$<br>$T_A = 0°C$ to $+85°C$ |
|---|---|
| Ceramic DIP | 100170F |
| Ceramic Flat Pack | 100170Y |

## PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $A_{na}$, $A_{nb}$ | Address Inputs |
| $\overline{E}_{na}$, $\overline{E}_{nb}$ | Enable Inputs |
| M | Mode Control Input |
| $H_a$ | $Q_0 - Q_3$ Polarity Select Input |
| $H_b$ | $Q_4 - Q_7$ Polarity Select Input |
| $H_c$ | Common Polarity Select Input |
| $Q_0 - Q_7$ | Data Outputs |

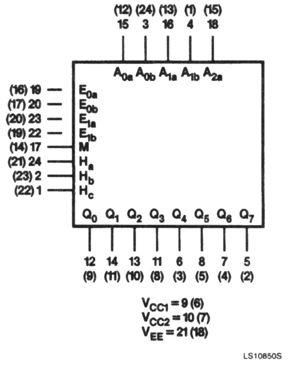
## PIN CONFIGURATION



A1b 1
Q7 2
Q4 3
Q6 4
Q5 5
VCC1 6
VCC2 7
Q3 8
Q0 9
Q2 10
Q1 11
A0a 12
24 A0b
23 Hb
22 Hc
21 Ha
20 Ē2a
19 Ē2b
18 VEE
17 Ē1b
16 Ē1a
15 A2a
14 M
13 A1a
Ha 24
Ē2a 23
Ē2b 22
VEE 21
Ē1b 20
Ē1a 19
Hc 1
Hb 2
A0b 3
A1b 4
Q7 5
Q4 6
18 A2a
17 M
16 A1a
15 A0a
14 Q1
13 Q2
7 Q6
8 Q5
9 VCC1
10 VCC2
11 Q3
12 Q0
CD08910S

Figure 1

## LOGIC SYMBOL



(12) 15 A0a
(24) 3 A0b
(13) 16 A1a
(1) 4 A1b
(15) 18 A2a
(16) 19 E0a
(17) 20 E0b
(20) 23 E1a
(19) 22 E1b
(14) 17 M
(21) 24 Ha
(23) 2 Hb
(22) 1 Hc
Q0 12 (9)
Q1 14 (11)
Q2 13 (10)
Q3 11 (8)
Q4 6 (3)
Q5 8 (5)
Q6 7 (4)
Q7 5 (2)
VCC1 = 9 (6)
VCC2 = 10 (7)
VEE = 21 (18)
LS10850S

Figure 2

# Demultiplexer/Decoder 100170

## LOGIC DIAGRAM

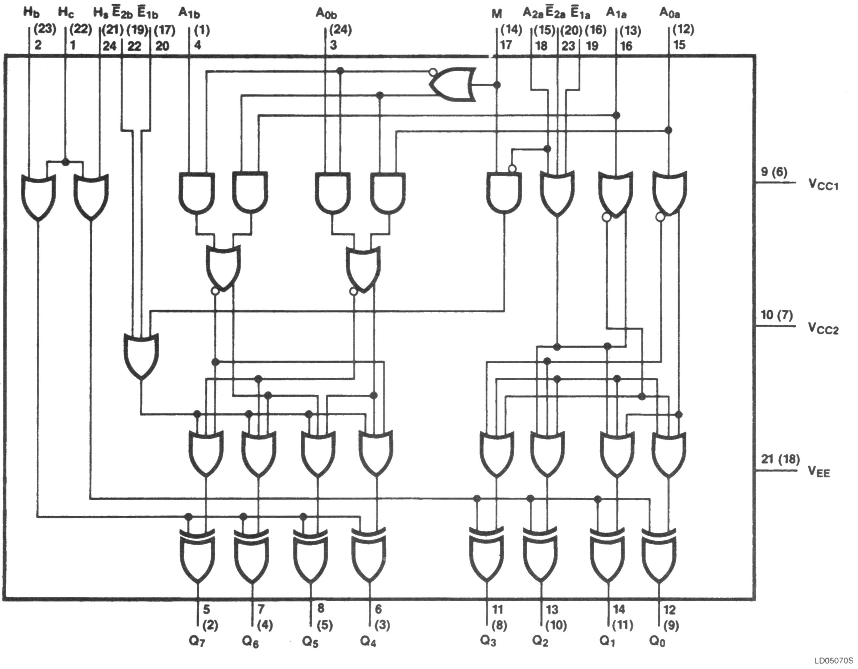

$H_b$ (23) 2
$H_c$ (22) 1
$H_a$ (21) 24
$\overline{E}_{2b}$ (19) 22
$\overline{E}_{1b}$ (17) 20
$A_{1b}$ (1) 4
$A_{0b}$ (24) 3
M (14) 17
$A_{2a}$ (15) 18
$\overline{E}_{2a}$ (20) 23
$\overline{E}_{1a}$ (16) 19
$A_{1a}$ (13) 16
$A_{0a}$ (12) 15
9 (6) $V_{CC1}$
10 (7) $V_{CC2}$
21 (18) $V_{EE}$
5 (2) $Q_7$
7 (4) $Q_6$
8 (5) $Q_5$
6 (3) $Q_4$
11 (8) $Q_3$
13 (10) $Q_2$
14 (11) $Q_1$
12 (9) $Q_0$
LD05070S

Figure 3. Universal Demux/Decoder

## FUNCTION TABLE (Dual 1-of-4 Mode)

| INPUTS | | | | OUTPUTS | | | | | | | | OPERATING MODE |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $H_a = H_b$ = HIGH | | | | $H_a = H_b$ = LOW | | | | |
| $\overline{E}_{0b}$ | $\overline{E}_{1b}$ | $A_{0b}$ | $A_{1b}$ | $Q_0$ | $Q_1$ | $Q_2$ | $Q_3$ | $Q_0$ | $Q_1$ | $Q_2$ | $Q_3$ | |
| H | X | X | X | L | L | L | L | H | H | H | H | Dual 1-of-4 Mode<br>M = $A_{2a}$ = $H_c$ = LOW |
| X | H | X | X | L | L | L | L | H | H | H | H | |
| L | L | L | H | H | L | L | L | L | H | H | H | |
| L | L | H | L | L | L | H | L | H | L | H | H | |
| L | L | H | H | L | L | L | H | H | H | H | L | |

## FUNCTION TABLE (Single 1-of-8 Mode)

| INPUTS | | | | | OUTPUTS | | | | | | | | | | | | | | | | OPERATING MODE |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | $H_c$ = HIGH | | | | | | | | $H_c$ = LOW | | | | | | | | |
| $\overline{E}_0$ | $\overline{E}_1$ | $A_{0a}$ | $A_{1a}$ | $A_{2a}$ | $Q_0$ | $Q_1$ | $Q_2$ | $Q_3$ | $Q_4$ | $Q_5$ | $Q_6$ | $Q_7$ | $Q_0$ | $Q_1$ | $Q_2$ | $Q_3$ | $Q_4$ | $Q_5$ | $Q_6$ | $Q_7$ | |
| H | X | X | X | X | L | L | L | L | L | L | L | L | H | H | H | H | H | H | H | H | Single 1-of-8 Mode<br>M = HIGH<br>$A_{0b} = A_{1b} = H_a = H_b$<br>= LOW |
| X | H | X | X | X | L | L | L | L | L | L | L | L | H | H | H | H | H | H | H | H | |
| L | L | L | L | L | H | L | L | L | L | L | L | L | L | H | H | H | H | H | H | H | |
| L | L | H | L | L | L | H | L | L | L | L | L | L | H | L | H | H | H | H | H | H | |
| L | L | L | H | L | L | L | H | L | L | L | L | L | H | H | L | H | H | H | H | H | |
| L | L | H | H | L | L | L | L | H | L | L | L | L | H | H | H | L | H | H | H | H | |
| L | L | L | L | H | L | L | L | L | H | L | L | L | H | H | H | H | L | H | H | H | |
| L | L | H | L | H | L | L | L | L | L | H | L | L | H | H | H | H | H | L | H | H | |
| L | L | L | H | H | L | L | L | L | L | L | H | L | H | H | H | H | H | H | L | H | |
| L | L | H | H | H | L | L | L | L | L | L | L | H | H | H | H | H | H | H | H | L | |

Positive Logic:
H = HIGH state (the more positive voltage) = 1
L = LOW state (the less positive voltage) = 0
X = Don't Care
$\overline{E}_0 = \overline{E}_{0a}$ and $\overline{E}_{0b}$ wired; $\overline{E}_1 = \overline{E}_{1a}$ and $\overline{E}_{1b}$ wired

# Demultiplexer/Decoder 100170

## ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | 100K ECL | UNIT |
|---|---|---|---|
| $V_{EE}$ | Supply voltage ($V_{CC1} = V_{CC2} =$ GND) | −7.0 to 0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | $V_{EE}$ to +0.5 | V |
| $I_O$ | Output source current | −55 | mA |
| $T_S$ | Storage temperature | −65 to +150 | °C |
| $T_J$ | Maximum junction temperature | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | | 100K ECL | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | −4.2 | −4.5 | −4.8 | V |
| $V_{EE}$ | Supply voltage (negative) when operating with 10K ECL family | | | | | −5.7 | V |
| $V_{IH}$ | HIGH level input voltage | $V_{CC1} = V_{CC2} =$ GND<br>$T_A = 0$°C to +85°C | $V_{EE} = -4.2$V | −1150 | | −880 | mV |
| | | | $V_{EE} = -4.5$V | −1165 | | | |
| | | | $V_{EE} = -4.8$V | | | | |
| $V_{IHT}$ | HIGH level input threshold voltage | | $V_{EE} = -4.2$V | −1150 | | | mV |
| | | | $V_{EE} = -4.5$V | −1165 | | | mV |
| | | | $V_{EE} = -4.8$V | | | | |
| $V_{ILT}$ | LOW level input threshold voltage | | $V_{EE} = -4.2$V | | | −1475 | mV |
| | | | $V_{EE} = -4.5$V | | | | |
| | | | $V_{EE} = -4.8$V | | | −1490 | mV |
| $V_{IL}$ | LOW level input voltage | | $V_{EE} = -4.2$V | −1810 | | −1475 | mV |
| | | | $V_{EE} = -4.5$V | | | | |
| | | | $V_{EE} = -4.8$V | | | −1490 | |
| $T_A$ | Operating ambient temperature | | | 0 | +25 | +85 | °C |

**NOTE:**
When operating at other than specified voltages (−4.2V, −4.5V, −4.8V) DC & AC Characteristics will vary slightly from specified values.

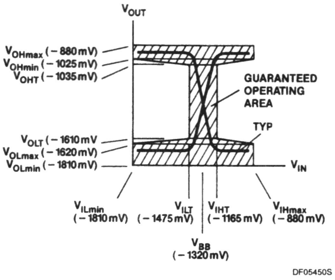
**DC ELECTRICAL CHARACTERISTICS** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$, $T_A = 0°C$ to $+85°C$ unless otherwise specified[1, 3]

| PARAMETER | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] | |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | $V_{EE} = -4.2V$ | −1025 | | −870 | mV | $V_{IN} = V_{IHmax}$ or $V_{IN} = V_{ILmin}$ | Loading with 50Ω to −2.0V ±0.010V |
| | | $V_{EE} = -4.5V$ | −1025 | −955 | −880 | mV | | |
| | | $V_{EE} = -4.8V$ | −1035 | | −880 | mV | | |
| $V_{OHT}$ | HIGH level output threshold voltage | $V_{EE} = -4.2V$ | −1035 | | | mV | $V_{IN} = V_{IHmin}$ or $V_{IN} = V_{ILmax}$ | |
| | | $V_{EE} = -4.5V$ | −1035 | | | mV | | |
| | | $V_{EE} = -4.8V$ | −1045 | | | mV | | |
| $V_{OLT}$ | LOW level output threshold voltage | $V_{EE} = -4.2V$ | | | −1590 | mV | $V_{IN} = V_{IHmin}$ or $V_{IN} = V_{ILmax}$ | |
| | | $V_{EE} = -4.5V$ | | | −1610 | mV | | |
| | | $V_{EE} = -4.8V$ | | | −1610 | mV | | |
| $V_{OL}$ | LOW level output voltage | $V_{EE} = -4.2V$ | −1810 | | −1600 | mV | $V_{IN} = V_{IHmax}$ or $V_{IN} = V_{ILmin}$ | |
| | | $V_{EE} = -4.5V$ | −1810 | −1705 | −1620 | mV | | |
| | | $V_{EE} = -4.8V$ | −1830 | | −1620 | mV | | |
| $I_{IH}$ | HIGH level input current | $H_C$, $A_{0a}$, $A_{1a}$, $A_{2a}$ | | | 310 | μA | $V_{IN} = V_{IHmax}$ | |
| | | All others | | | 250 | | | |
| $I_{IL}$ | LOW level input current | | 0.5 | | | μA | $V_{IN} = V_{ILmin}$ | |
| $-I_{EE}$ | $V_{EE}$ supply current | | 76 | 110 | 153 | mA | Inputs open | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | $V_{EE} = -4.2V$<br>$T_A = +25°C$ | | | 0.035 | V/V | | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | | 0.070 | V/V | | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 4.

## Demultiplexer/Decoder 100170



**NOTES:**

$V_{IHmax}$ – Maximum HIGH level input voltage (the most positive $V_{IH}$).
$V_{IHT}$ – HIGH level input threshold voltage.
$V_{ILT}$ – LOW level input threshold voltage.
$V_{ILmin}$ – Minimum LOW level input voltage (the most negative $V_{IL}$).
$V_{OHmax}$ – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition.
$V_{OHmin}$ – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition.
$V_{OHT}$ – HIGH level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLT}$ – LOW level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLmax}$ – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions.
$V_{OLmin}$ – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions.
$V_{BB}$ – Reference bias voltage (the internally generated reference voltage which is used to set the input and output threshold level).

**Figure 4. Transfer Characteristics**

## AC ELECTRICAL CHARACTERISTICS

**Ceramic DIP** $V_{CC1} = V_{CC2} = \text{GND}$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 0.80 | 2.30 | 0.80 | 2.20 | 0.80 | 2.30 | ns | Figs. 5, 6, 7 |
| $t_{PHL}$ | $\overline{E}_{na}$, $\overline{E}_{nb}$ to $Q_n$ | 0.80 | 2.30 | 0.80 | 2.20 | 0.80 | 2.30 | ns | |
| $t_{PLH}$ | Propagation delay | 0.95 | 2.80 | 0.95 | 2.70 | 1.00 | 2.90 | ns | |
| $t_{PHL}$ | $A_{na}$, $A_{nb}$ to $Q_n$ | 0.95 | 2.80 | 1.00 | 2.70 | 1.00 | 2.90 | ns | |
| $t_{PLH}$ | Propagation delay | 1.00 | 3.00 | 1.00 | 2.90 | 1.00 | 3.00 | ns | |
| $t_{PHL}$ | $H_a$, $H_b$, $H_c$ to $Q_n$ | 1.00 | 3.00 | 1.00 | 2.90 | 1.00 | 3.00 | ns | |
| $t_{PLH}$ | Propagation delay | 1.50 | 3.90 | 1.60 | 3.80 | 1.60 | 3.90 | ns | |
| $t_{PHL}$ | M to $Q_n$ | 1.50 | 3.90 | 1.60 | 3.80 | 1.60 | 3.90 | ns | |
| $t_{TLH}$ | Transition time | 0.45 | 1.60 | 0.45 | 1.60 | 0.45 | 1.60 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.60 | 0.45 | 1.60 | 0.45 | 1.60 | ns | |

**Ceramic DIP** $V_{CC1} = V_{CC2} = \text{GND}$, $V_{EE} = -5.2V \pm 5\%$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 0.80 | 2.30 | 0.80 | 2.20 | 0.80 | 2.30 | ns | Figs. 5, 6, 7 |
| $t_{PHL}$ | $\overline{E}_{na}$, $\overline{E}_{nb}$ to $Q_n$ | 0.80 | 2.30 | 0.80 | 2.20 | 0.80 | 2.30 | ns | |
| $t_{PLH}$ | Propagation delay | 0.95 | 2.80 | 0.95 | 2.70 | 1.00 | 2.90 | ns | |
| $t_{PHL}$ | $A_{na}$, $A_{nb}$ to $Q_n$ | 1.00 | 2.80 | 1.00 | 2.70 | 1.00 | 2.90 | ns | |
| $t_{PLH}$ | Propagation delay | 1.00 | 3.00 | 1.00 | 2.90 | 1.00 | 3.00 | ns | |
| $t_{PHL}$ | $H_a$, $H_b$, $H_c$ to $Q_n$ | 1.00 | 3.00 | 1.00 | 2.90 | 1.00 | 3.00 | ns | |
| $t_{PLH}$ | Propagation delay | 1.50 | 3.90 | 1.60 | 3.80 | 1.60 | 3.90 | ns | |
| $t_{PHL}$ | M to $Q_n$ | 1.50 | 3.90 | 1.60 | 3.80 | 1.60 | 3.90 | ns | |
| $t_{TLH}$ | Transition time | 0.45 | 1.60 | 0.45 | 1.60 | 0.45 | 1.60 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.60 | 0.45 | 1.60 | 0.45 | 1.60 | ns | |

## AC ELECTRICAL CHARACTERISTICS

**Flat Pack** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$\overline{E}_{na}$, $\overline{E}_{nb}$ to $Q_n$ | 0.80<br>0.80 | 2.10<br>2.10 | 0.80<br>0.80 | 2.00<br>2.00 | 0.80<br>0.80 | 2.10<br>2.10 | ns<br>ns | Figs. 5, 6, 7 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$A_{na}$, $A_{nb}$ to $Q_n$ | 0.95<br>0.95 | 2.60<br>2.60 | 0.95<br>1.00 | 2.50<br>2.50 | 1.00<br>1.00 | 2.70<br>2.70 | ns<br>ns | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$H_a$, $H_b$, $H_c$ to $Q_n$ | 1.00<br>1.00 | 2.80<br>2.80 | 1.00<br>1.00 | 2.70<br>2.70 | 1.00<br>1.00 | 2.80<br>2.80 | ns<br>ns | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>M to $Q_n$ | 1.50<br>1.50 | 3.70<br>3.70 | 1.60<br>1.60 | 3.60<br>3.60 | 1.60<br>1.60 | 3.70<br>3.70 | ns<br>ns | |
| $t_{TLH}$<br>$t_{THL}$ | Transition time<br>20% to 80%, 80% to 20% | 0.45<br>0.45 | 1.60<br>1.60 | 0.45<br>0.45 | 1.60<br>1.60 | 0.45<br>0.45 | 1.60<br>1.60 | ns<br>ns | |

**Flat Pack** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V \pm 5\%$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$\overline{E}_{na}$, $\overline{E}_{nb}$ to $Q_n$ | 0.80<br>0.80 | 2.10<br>2.10 | 0.80<br>0.80 | 2.00<br>2.00 | 0.80<br>0.80 | 2.10<br>2.10 | ns<br>ns | Figs. 5, 6, 7 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$A_{na}$, $A_{nb}$ to $Q_n$ | 0.95<br>0.95 | 2.60<br>2.60 | 0.95<br>1.00 | 2.50<br>2.50 | 1.00<br>1.00 | 2.70<br>2.70 | ns<br>ns | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$H_a$, $H_b$, $H_c$ to $Q_n$ | 1.00<br>1.00 | 2.80<br>2.80 | 1.00<br>1.00 | 2.70<br>2.70 | 1.00<br>1.00 | 2.80<br>2.80 | ns<br>ns | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>M to $Q_n$ | 1.50<br>1.50 | 3.70<br>3.70 | 1.60<br>1.60 | 3.60<br>3.60 | 1.60<br>1.60 | 3.70<br>3.70 | ns<br>ns | |
| $t_{TLH}$<br>$t_{THL}$ | Transition time<br>20% to 80%, 80% to 20% | 0.45<br>0.45 | 1.60<br>1.60 | 0.45<br>0.45 | 1.60<br>1.60 | 0.45<br>0.45 | 1.60<br>1.60 | ns<br>ns | |

## AC WAVEFORMS

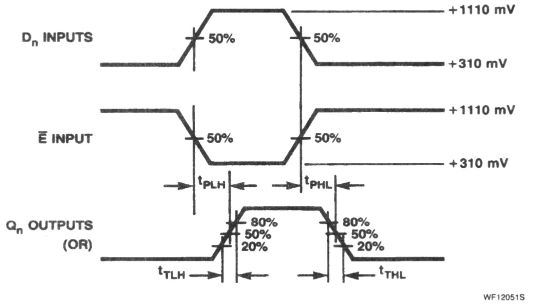
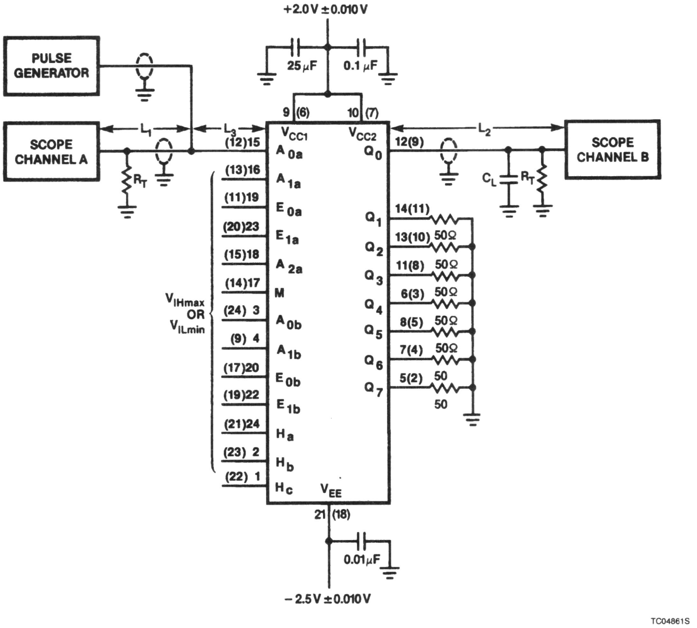


Figure 5. Propagation Delay and Transition Times

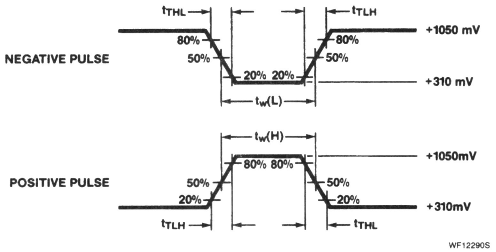
## TEST CIRCUITS AND WAVEFORMS


+2.0V ±0.010V
PULSE GENERATOR
25μF
0.1μF
9 (6)
10 (7)
SCOPE CHANNEL A
L1
L3
L2
SCOPE CHANNEL B
RT
CL
VCC1
VCC2
(12)15 A0a
(13)16 A1a
(11)19 E0a
(20)23 E1a
(15)18 A2a
(14)17 M
(24) 3 A0b
(9) 4 A1b
(17)20 E0b
(19)22 E1b
(21)24 Ha
(23) 2 Hb
(22) 1 Hc
VIHmax OR VILmin
12(9) Q0
14(11) Q1
13(10) Q2
11(8) Q3
6(3) Q4
8(5) Q5
7(4) Q6
5(2) Q7
50Ω
50
VEE
21 (18)
0.01μF
−2.5V ±0.010V
TC04861S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1μF and 25μF from GND to $V_{CC}$, 0.01μF and 25μF from GND to $V_{EE}$. (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance ≤ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ±1% or better.
11. Pin connections are for Flat Pack and in parentheses for Ceramic DIP.

Figure 6. Test Circuit


NEGATIVE PULSE
tTHL
tTLH
80%
50%
20%
tw(L)
+1050 mV
+310 mV
POSITIVE PULSE
tw(H)
+1050mV
+310mV
WF12290S

| INPUT PULSE REQUIREMENTS<br>$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -2.5V \pm 0.010V$, $V_T$ = GND (0V) | | | | | |
|---|---|---|---|---|---|
| Family | Amplitude | Rep Rate | Pulse Width | $t_{TLH}$ | $t_{THL}$ |
| 100K ECL | 740mVp-p | 1MHz | 500ns | 0.7 ±0.1ns | 0.7 ±0.1ns |

Figure 7. Input Pulse Definition

**Signetics**

# 100171
# Multiplexer

**Triple 4-Input Multiplexer**
***Product Specification***

**ECL Products**

## DESCRIPTION

The 100171 is a Triple 4-input Multiplexer fed by 2 common address inputs, with true and complementary data outputs. A HIGH state on the Enable Input ($\overline{E}$) forces all true outputs low.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 100171 | 1.10ns | 83mA |

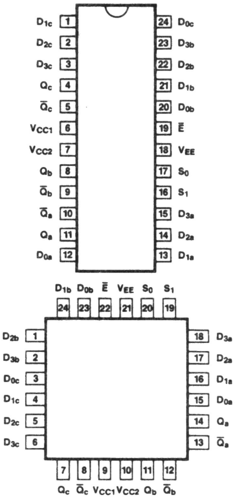
## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} = GND$; $V_{EE} = -4.2V$ to $-4.8V$<br>$T_A = 0°C$ to $+85°C$ |
|---|---|
| Ceramic DIP | 100171F |
| Ceramic Flat Pack | 100171Y |

## PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_{na}$, $D_{nb}$, $D_{nc}$ | Data Inputs |
| $S_0$, $S_1$ | Select Inputs |
| $\overline{E}$ | Enable Input |
| $Q_a$, $Q_b$, $Q_c$:$\overline{Q}_a$, $\overline{Q}_b$, $\overline{Q}_c$ | Data Outputs |

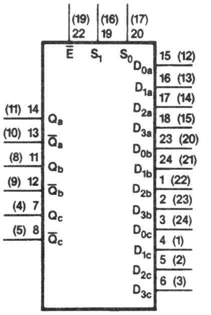
## PIN CONFIGURATION


D1c 1
D2c 2
D3c 3
Qc 4
Q̄c 5
VCC1 6
VCC2 7
Qb 8
Q̄b 9
Q̄a 10
Qa 11
D0a 12
24 D0c
23 D3b
22 D2b
21 D1b
20 D0b
19 Ē
18 VEE
17 S0
16 S1
15 D3a
14 D2a
13 D1a
D1b 24
D0b 23
Ē 22
VEE 21
S0 20
S1 19
D2b 1
D3b 2
D0c 3
D1c 4
D2c 5
D3c 6
18 D3a
17 D2a
16 D1a
15 D0a
14 Qa
13 Q̄a
7 Qc
8 Q̄c
9 VCC1
10 VCC2
11 Qb
12 Q̄b

CD08930S

Figure 1

## LOGIC SYMBOL


(19) 22
(16) 19
(17) 20
Ē
S1
S0
(11) 14 Qa
(10) 13 Q̄a
(8) 11 Qb
(9) 12 Q̄b
(4) 7 Qc
(5) 8 Q̄c
D0a 15 (12)
D1a 16 (13)
D2a 17 (14)
D3a 18 (15)
D0b 23 (20)
D1b 24 (21)
D2b 1 (22)
D3b 2 (23)
D0c 3 (24)
D1c 4 (1)
D2c 5 (2)
D3c 6 (3)

$V_{CC1} = 9$ (6)
$V_{CC2} = 10$ (7)
$V_{EE} = 21$ (18)

**Pin connections for Flat Pack and in ( ) for Slim Dip package**

LS10780S

Figure 2

# Multiplexer 100171

## LOGIC DIAGRAM

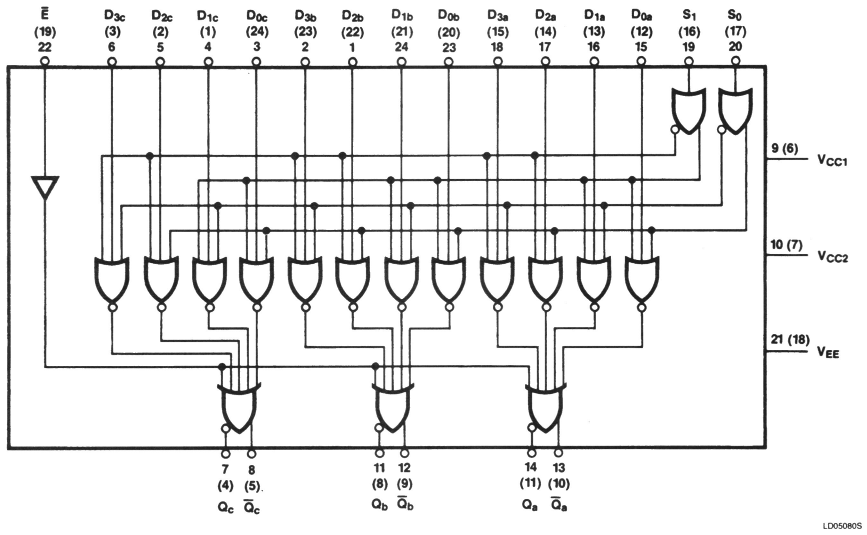

Ē (19) 22
D3c (3) 6
D2c (2) 5
D1c (1) 4
D0c (24) 3
D3b (23) 2
D2b (22) 1
D1b (21) 24
D0b (20) 23
D3a (15) 18
D2a (14) 17
D1a (13) 16
D0a (12) 15
S1 (16) 19
S0 (17) 20
9 (6) VCC1
10 (7) VCC2
21 (18) VEE
7 (4) Qc
8 (5) Q̄c
11 (8) Qb
12 (9) Q̄b
14 (11) Qa
13 (10) Q̄a
LD05080S

Figure 3

## FUNCTION TABLE

| INPUTS | | | | | | | OUTPUTS | |
|---|---|---|---|---|---|---|---|---|
| $\overline{E}$ | $S_0$ | $S_1$ | $D_0$ | $D_1$ | $D_2$ | $D_3$ | $\overline{Q}$ | Q |
| H | X | X | X | X | X | X | H | L |
| L | L | L | L | X | X | X | H | L |
| L | L | L | H | X | X | X | L | H |
| L | L | H | X | L | X | X | H | L |
| L | L | H | X | H | X | X | L | H |
| L | H | L | X | X | L | X | H | L |
| L | H | L | X | X | H | X | L | H |
| L | H | H | X | X | X | L | H | L |
| L | H | H | X | X | X | H | L | H |

Positive Logic:
H = HIGH state (more positive voltage) = 1
L = LOW state (less positive voltage) = 0
X = Don't care

# Multiplexer　　100171

**ABSOLUTE MAXIMUM RATINGS** (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | 100K ECL | UNIT |
|---|---|---|---|
| $V_{EE}$ | Supply voltage ($V_{CC1} = V_{CC2}$ = GND) | −7.0 to 0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | $V_{EE}$ to +0.5 | V |
| $I_O$ | Output source current | −55 | mA |
| $T_S$ | Storage temperature | −65 to +150 | °C |
| $T_J$ | Maximum junction temperature | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | | 100K ECL | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | −4.2 | −4.5 | −4.8 | V |
| $V_{EE}$ | Supply voltage (negative) when operating with 10K ECL family | | | | | −5.7 | V |
| $V_{IH}$ | HIGH level input voltage | $V_{CC1} = V_{CC2}$ = GND<br>$T_A$ = 0°C to +85°C | $V_{EE}$ = −4.2V | −1150 | | −880 | mV |
| | | | $V_{EE}$ = −4.5V | −1165 | | | |
| | | | $V_{EE}$ = −4.8V | | | | |
| $V_{IHT}$ | HIGH level input threshold voltage | | $V_{EE}$ = −4.2V | −1150 | | | mV |
| | | | $V_{EE}$ = −4.5V | −1165 | | | mV |
| | | | $V_{EE}$ = −4.8V | | | | |
| $V_{ILT}$ | LOW level input threshold voltage | | $V_{EE}$ = −4.2V | | | −1475 | mV |
| | | | $V_{EE}$ = −4.5V | | | | |
| | | | $V_{EE}$ = −4.8V | | | −1490 | mV |
| $V_{IL}$ | LOW level input voltage | | $V_{EE}$ = −4.2V | −1810 | | −1475 | mV |
| | | | $V_{EE}$ = −4.5V | | | | |
| | | | $V_{EE}$ = −4.8V | | | −1490 | |
| $T_A$ | Operating ambient temperature | | | 0 | +25 | +85 | °C |

**NOTE:**
When operating at other than specified voltages (−4.2V, −4.5V, −4.8V) DC & AC Characteristics will vary slightly from specified values.

# Multiplexer 100171

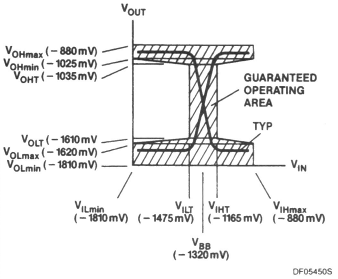
## DC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$, $T_A = 0°C$ to $+85°C$ unless otherwise specified[1, 3]

| PARAMETER | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] | |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | $V_{EE} = -4.2V$ | -1025 | | -870 | mV | $V_{IN} = V_{IHmax}$ or $V_{IN} = V_{ILmin}$ | Loading with 50Ω to -2.0V ±0.010V |
| | | $V_{EE} = -4.5V$ | -1025 | -955 | -880 | mV | | |
| | | $V_{EE} = -4.8V$ | -1035 | | -880 | mV | | |
| $V_{OHT}$ | HIGH level output threshold voltage | $V_{EE} = -4.2V$ | -1035 | | | mV | $V_{IN} = V_{IHmin}$ or $V_{IN} = V_{ILmax}$ | |
| | | $V_{EE} = -4.5V$ | -1035 | | | mV | | |
| | | $V_{EE} = -4.8V$ | -1045 | | | mV | | |
| $V_{OLT}$ | LOW level output threshold voltage | $V_{EE} = -4.2V$ | | | -1590 | mV | $V_{IN} = V_{IHmin}$ or $V_{IN} = V_{ILmax}$ | |
| | | $V_{EE} = -4.5V$ | | | -1610 | mV | | |
| | | $V_{EE} = -4.8V$ | | | -1610 | mV | | |
| $V_{OL}$ | LOW level output voltage | $V_{EE} = -4.2V$ | -1810 | | -1600 | mV | $V_{IN} = V_{IHmax}$ or $V_{IN} = V_{ILmin}$ | |
| | | $V_{EE} = -4.5V$ | -1810 | -1705 | -1620 | mV | | |
| | | $V_{EE} = -4.8V$ | -1830 | | -1620 | mV | | |
| $I_{IH}$ | High level input current | $D_{na}$, $D_{nb}$, $D_{nc}$ | | | 340 | µA | $V_{IN} = V_{IHmax}$ | |
| | | $S_0$, $S_1$, $\overline{E}$ | | | 300 | | | |
| $I_{IL}$ | LOW level input current | | 0.5 | | | µA | $V_{IN} = V_{ILmin}$ | |
| $-I_{EE}$ | $V_{EE}$ supply current | | 56 | 83 | 114 | mA | Inputs open | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | $V_{EE} = -4.2V$<br>$T_A = +25°C$ | | | 0.035 | V/V | | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | | 0.070 | V/V | | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 4.

# Multiplexer 100171



**NOTES:**

| | |
|---|---|
| $V_{IHmax}$ | – Maximum HIGH level input voltage (the most positive $V_{IH}$). |
| $V_{IHT}$ | – HIGH level input threshold voltage. |
| $V_{ILT}$ | – LOW level input threshold voltage. |
| $V_{ILmin}$ | – Minimum LOW level input voltage (the most negative $V_{IL}$). |
| $V_{OHmax}$ | – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition. |
| $V_{OHmin}$ | – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition. |
| $V_{OHT}$ | – HIGH level output threshold voltage with the inputs set to their respective threshold levels. |
| $V_{OLT}$ | – LOW level output threshold voltage with the inputs set to their respective threshold levels. |
| $V_{OLmax}$ | – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions. |
| $V_{OLmin}$ | – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions. |
| $V_{BB}$ | – Reference bias voltage. The internally generated reference voltage which is used to set the input and output threshold level. |

**Figure 4. Transfer Characteristics**

## AC ELECTRICAL CHARACTERISTICS

### Ceramic DIP $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 0.45 | 1.70 | 0.45 | 1.60 | 0.50 | 1.70 | ns | Figs. 5, 6, 7 |
| $t_{PHL}$ | $D_{na}$, $D_{nb}$, $D_{nc}$ to output | 0.45 | 1.70 | 0.45 | 1.60 | 0.50 | 1.70 | ns | |
| $t_{PLH}$ | Propagation delay | 0.90 | 2.40 | 0.90 | 2.60 | 1.00 | 3.00 | ns | |
| $t_{PHL}$ | $S_0$, $S_1$ to output | 0.90 | 2.40 | 0.90 | 2.60 | 1.00 | 3.00 | ns | |
| $t_{PLH}$ | Propagation delay | 0.65 | 2.40 | 0.65 | 2.30 | 0.75 | 2.40 | ns | |
| $t_{PHL}$ | $\overline{E}$ to output | 0.65 | 2.40 | 0.65 | 2.30 | 0.75 | 2.40 | ns | |
| $t_{TLH}$ | Transition time | 0.45 | 1.70 | 0.45 | 1.50 | 0.45 | 1.50 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.70 | 0.45 | 1.50 | 0.45 | 1.50 | ns | |

### Ceramic DIP $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V \pm 5\%$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 0.45 | 1.70 | 0.45 | 1.60 | 0.50 | 1.70 | ns | Figs. 5, 6, 7 |
| $t_{PHL}$ | $D_{na}$, $D_{nb}$, $D_{nc}$ to output | 0.45 | 1.70 | 0.45 | 1.60 | 0.50 | 1.70 | ns | |
| $t_{PLH}$ | Propagation delay | 0.90 | 2.40 | 0.90 | 2.60 | 1.00 | 3.00 | ns | |
| $t_{PHL}$ | $S_0$, $S_1$ to output | 0.90 | 2.40 | 0.90 | 2.60 | 1.00 | 3.00 | ns | |
| $t_{PLH}$ | Propagation delay | 0.65 | 2.40 | 0.65 | 2.30 | 0.75 | 2.40 | ns | |
| $t_{PHL}$ | $\overline{E}$ to output | 0.65 | 2.40 | 0.65 | 2.30 | 0.75 | 2.40 | ns | |
| $t_{TLH}$ | Transition time | 0.45 | 1.70 | 0.45 | 1.50 | 0.45 | 1.50 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.70 | 0.45 | 1.50 | 0.45 | 1.50 | ns | |

### Flat Pack $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 0.45 | 1.50 | 0.45 | 1.40 | 0.50 | 1.50 | ns | Figs. 5, 6, 7 |
| $t_{PHL}$ | $D_{na}$, $D_{nb}$, $D_{nc}$ to output | 0.45 | 1.50 | 0.45 | 1.40 | 0.50 | 1.50 | ns | |
| $t_{PLH}$ | Propagation delay | 0.90 | 2.20 | 0.90 | 2.40 | 1.00 | 2.80 | ns | |
| $t_{PHL}$ | $S_0$, $S_1$ to output | 0.90 | 2.20 | 0.90 | 2.40 | 1.00 | 2.80 | ns | |
| $t_{PLH}$ | Propagation delay | 0.65 | 2.20 | 0.65 | 2.10 | 0.75 | 2.20 | ns | |
| $t_{PHL}$ | $\overline{E}$ to output | 0.65 | 2.20 | 0.65 | 2.10 | 0.75 | 2.20 | ns | |
| $t_{TLH}$ | Transition time | 0.45 | 1.70 | 0.45 | 1.50 | 0.45 | 1.50 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.70 | 0.45 | 1.50 | 0.45 | 1.50 | ns | |

## AC ELECTRICAL CHARACTERISTICS

**Flat Pack** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V \pm 5\%$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 0.45 | 1.50 | 0.45 | 1.40 | 0.50 | 1.50 | ns | Figs. 5, 6, 7 |
| $t_{PHL}$ | $D_{na}$, $D_{nb}$, $D_{nc}$ to output | 0.45 | 1.50 | 0.45 | 1.40 | 0.50 | 1.50 | ns | |
| $t_{PLH}$ | Propagation delay | 0.90 | 2.20 | 0.90 | 2.40 | 1.00 | 2.80 | ns | |
| $t_{PHL}$ | $S_0$, $S_1$ to output | 0.90 | 2.20 | 0.90 | 2.40 | 1.00 | 2.80 | ns | |
| $t_{PLH}$ | Propagation delay | 0.65 | 2.20 | 0.65 | 2.10 | 0.75 | 2.20 | ns | |
| $t_{PHL}$ | $\overline{E}$ to output | 0.65 | 2.20 | 0.65 | 2.10 | 0.75 | 2.20 | ns | |
| $t_{TLH}$ | Transition time | 0.45 | 1.70 | 0.45 | 1.50 | 0.45 | 1.50 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.70 | 0.45 | 1.50 | 0.45 | 1.50 | ns | |

## AC WAVEFORMS

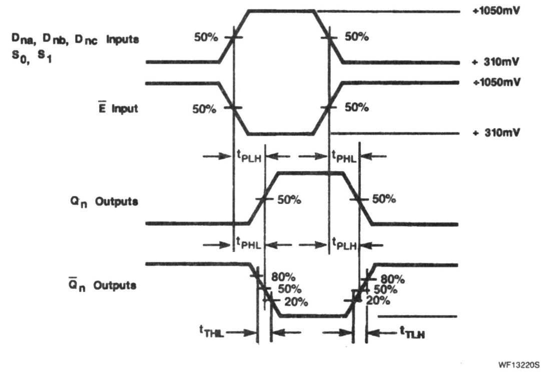
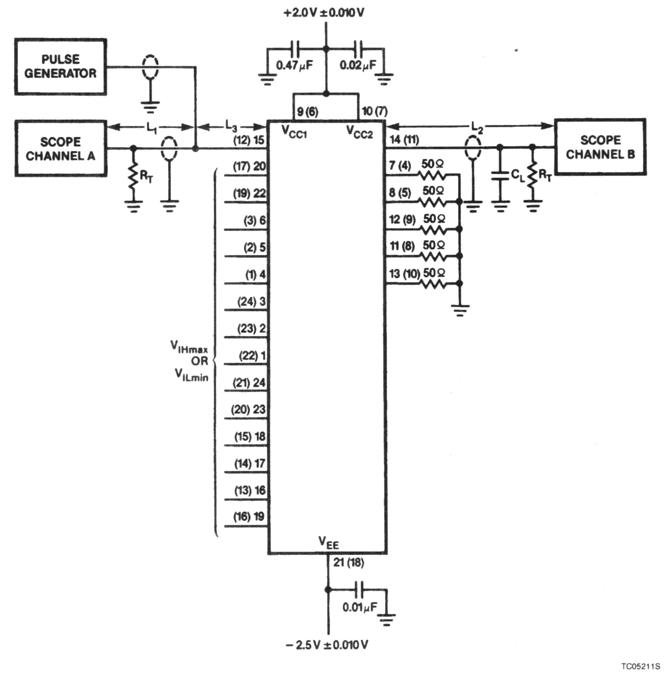

$D_{na}$, $D_{nb}$, $D_{nc}$ Inputs
$S_0$, $S_1$
50%
50%
+1050mV
+ 310mV
+1050mV
$\overline{E}$ Input
50%
50%
+ 310mV
$t_{PLH}$
$t_{PHL}$
$Q_n$ Outputs
50%
50%
$t_{PHL}$
$t_{PLH}$
$\overline{Q}_n$ Outputs
80%
50%
20%
80%
50%
20%
$t_{THL}$
$t_{TLH}$
WF13220S

Figure 5. Propagation Delay and Transition Times

# Multiplexer 100171

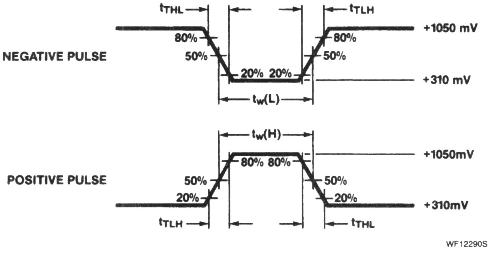
## TEST CIRCUITS AND WAVEFORMS


+2.0V ±0.010V
0.47µF
0.02µF
PULSE GENERATOR
SCOPE CHANNEL A
SCOPE CHANNEL B
L1
L2
L3
RT
CL
9 (6)
10 (7)
VCC1
VCC2
(12) 15
(17) 20
(19) 22
(3) 6
(2) 5
(1) 4
(24) 3
(23) 2
(22) 1
(21) 24
(20) 23
(15) 18
(14) 17
(13) 16
(16) 19
VIHmax OR VILmin
14 (11)
7 (4) 50Ω
8 (5) 50Ω
12 (9) 50Ω
11 (8) 50Ω
13 (10) 50Ω
VEE
21 (18)
0.01µF
−2.5V ±0.010V
TC05211S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1µF and 25µF from GND to $V_{CC}$, 0.01µF and 25µF from GND to $V_{EE}$. (0.01 and 0.1µF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance ≤ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ±1% or better.
11. Pin connections are for Flat Pack and in parentheses for Ceramic DIP.

Figure 6. Test Circuit


NEGATIVE PULSE
POSITIVE PULSE
tTHL
tTLH
80%
50%
20%
tw(L)
tw(H)
+1050 mV
+310 mV
WF12290S

| INPUT PULSE REQUIREMENTS<br>$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -2.5V \pm 0.010V$, $V_T$ = GND (0V) | | | | | |
|---|---|---|---|---|---|
| Family | Amplitude | Rep Rate | Pulse Width | $t_{TLH}$ | $t_{THL}$ |
| 100K ECL | 740mVp-p | 1MHz | 500ns | 0.7 ±0.1ns | 0.7 ±0.1ns |

Figure 7. Input Pulse Definition

**Signetics**

# 100175
## Translator

**100K-to-10K Translator**
***Product Specification***

**ECL Products**

## DESCRIPTION

The 100175 is composed of five latches with one data input and one data output. All latches have a Master Reset (MR) input and two Enable ($E_0$, $E_1$) inputs. A Q output follows its $D_n$ inputs when both $\overline{E}_0$ and $\overline{E}_1$ are LOW. When either $\overline{E}_0$ or $\overline{E}_1$ (or both) are HIGH, the latches store the last valid data present on their $D_n$ inputs. The MR input makes the Q outputs LOW if either $\overline{E}_0$ or $\overline{E}_1$ (or both) are HIGH. The inputs are 100K compatible and the outputs are 10K compatible.

| TYPE | TYPICAL PROPAGATION DELAY | | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|---|
| 100175 | $D_n$ to $Q_n$ | 2.2ns | 78mA |
| | $\overline{E}_n$ to $Q_n$ | 2.7ns | |

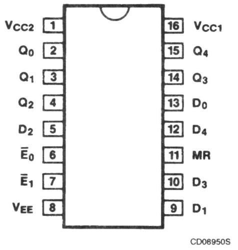
## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} = GND$; $V_{EE} = -5.2V$<br>$T_A = 0°C$ to $+75°C$ |
|---|---|
| Ceramic DIP | 100175F |

## PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_0 - D_4$ | Data Inputs |
| MR | Master Reset Input |
| $\overline{E}_0$, $\overline{E}_1$ | Enable Inputs |
| $Q_0 - Q_4$ | Data Outputs |

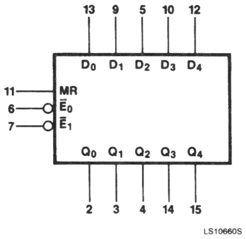
## PIN CONFIGURATION



VCC2 1
Q0 2
Q1 3
Q2 4
D2 5
Ē0 6
Ē1 7
VEE 8
16 VCC1
15 Q4
14 Q3
13 D0
12 D4
11 MR
10 D3
9 D1
CD08950S

Figure 1

## LOGIC SYMBOL



13
9
5
10
12
D0
D1
D2
D3
D4
11
MR
6
Ē0
7
Ē1
Q0
Q1
Q2
Q3
Q4
2
3
4
14
15
LS10660S

Figure 2

## LOGIC DIAGRAM

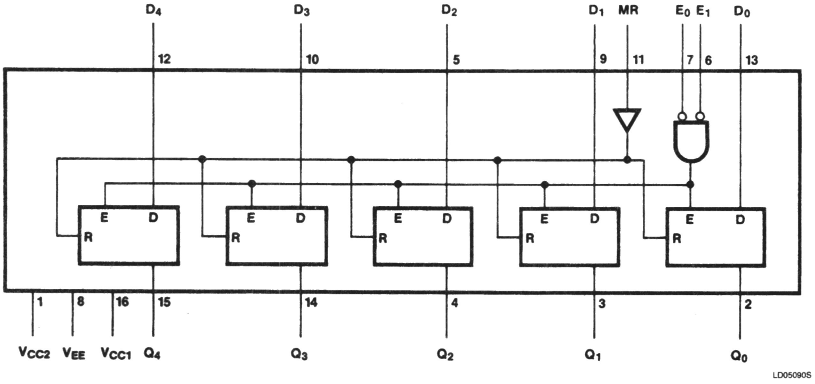

D4
D3
D2
D1
MR
E0
E1
D0
12
10
5
9
11
7
6
13
E
D
R
1
8
16
15
14
4
3
2
VCC2
VEE
VCC1
Q4
Q3
Q2
Q1
Q0
LD05090S

Figure 3

## FUNCTION TABLE

| $D_n$ | $\overline{E}_0$ | $\overline{E}_1$ | MR | $Q_n$ |
|---|---|---|---|---|
| H | L | L | X | H |
| L | L | L | X | L |
| X | H | X | L | $Q_n - 1$ |
| X | X | H | L | $Q_n - 1$ |
| X | H | X | H | L |
| X | X | H | H | L |

Positive Logic:
H = HIGH state (more positive voltage) = 1
L = LOW state (less positive voltage) = 0
X = Don't Care
$Q_n - 1$ = Previous state (state does not change)

# Translator

# 100175

**ABSOLUTE MAXIMUM RATINGS** (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| | PARAMETER | 100K ECL | UNIT |
|---|---|---|---|
| $V_{EE}$ | Supply voltage ($V_{CC1}$ = $V_{CC2}$ = GND) | -7.0 to 0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | $V_{EE}$to +0.5 | V |
| $I_O$ | Output source current | -55 | mA |
| $T_S$ | Storage temperature | -65 to +150 | °C |
| $T_J$ | Maximum junction temperature | +150 | °C |

## DC OPERATING CONDITIONS

| | PARAMETER | | 100K ECL | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | -5.2 | | V |
| $V_{EE}$ | Supply voltage (negative) when operating with 10K ECL family | | | | -5.7 | V |
| $V_{IH}$ | HIGH level input voltage | $V_{CC1}$ = $V_{CC2}$ = GND<br>$V_{EE}$ = -5.2V<br>$T_A$ = 0°C to +75°C | -1165 | | -880 | mV |
| $V_{IHT}$ | HIGH level input threshold voltage | | -1165 | | | mV |
| $V_{ILT}$ | LOW level input threshold voltage | | | | -1475 | mV |
| $V_{IL}$ | LOW level input voltage | | -1810 | | -1475 | mV |
| $T_A$ | Operating ambient temperature | | 0 | +25 | +75 | °C |

**NOTE:**
When operating at other than specified voltages (-5.2V) DC & AC Characteristics will vary slightly from specified values.

# Translator

# 100175

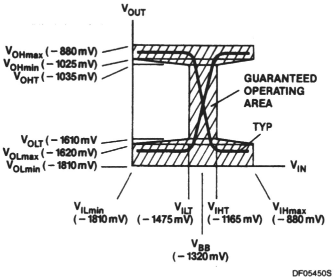
## DC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = \text{GND}$, $V_{EE} = -5.2\text{V} \pm 5\%$, $T_A = 0°\text{C}$ to $+75°\text{C}$ unless otherwise specified[1, 3]

| PARAMETER | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] | |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | $T_A = 0°\text{C}$ | −1000 | | −840 | mV | $V_{IN} = V_{IHmax}$ or $V_{IN} = V_{ILmin}$ | Loading with 50Ω to −2.0V ±0.010V |
| | | $T_A = +25°\text{C}$ | −960 | | −810 | mV | | |
| | | $T_A = +75°\text{C}$ | −900 | | −720 | mV | | |
| $V_{OHT}$ | HIGH level output threshold voltage | $T_A = 0°\text{CV}$ | −1020 | | | mV | $V_{IN} = V_{IHmin}$ or $V_{IN} = V_{ILmax}$ | |
| | | $T_A = +25°\text{CV}$ | −980 | | | mV | | |
| | | $T_A = +75°\text{CV}$ | −920 | | | mV | | |
| $V_{OLT}$ | LOW level output threshold voltage | $T_A = 0°\text{CV}$ | | | −1645 | mV | $V_{IN} = V_{IHmin}$ or $V_{IN} = V_{ILmax}$ | |
| | | $T_A = +25°\text{CV}$ | | | −1630 | mV | | |
| | | $T_A = +75°\text{CV}$ | | | −1605 | mV | | |
| $V_{OL}$ | LOW level output voltage | $T_A = 0°\text{CV}$ | −1870 | | −1665 | mV | $V_{IN} = V_{IHmax}$ or $V_{IN} = V_{ILmin}$ | |
| | | $T_A = +25°\text{CV}$ | −1850 | | −1650 | mV | | |
| | | $T_A = +75°\text{CV}$ | −1830 | | −1625 | mV | | |
| $I_{IH}$ | HIGH level input current | C input | | | 650 | µA | $V_{IN} = V_{IHmax}$ | |
| | | All others | | | 290 | | | |
| $I_{IL}$ | LOW level input current | | 0.5 | | | µA | $V_{IN} = V_{ILmin}$ | |
| $-I_{EE}$ | $V_{EE}$ supply current | | 50 | 67 | 102 | mA | Inputs open | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | $V_{EE} = -4.2\text{V}$<br>$T_A = +25°\text{C}$ | | | 0.035 | V/V | | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | | 0.070 | V/V | | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 4.

## Translator 100175


$V_{OUT}$
$V_{OHmax}$ (−880mV)
$V_{OHmin}$ (−1025mV)
$V_{OHT}$ (−1035mV)
GUARANTEED OPERATING AREA
TYP
$V_{OLT}$ (−1610mV
$V_{OLmax}$ (−1620mV)
$V_{OLmin}$ (−1810mV)
$V_{IN}$
$V_{ILmin}$ (−1810mV)
$V_{ILT}$ (−1475mV)
$V_{IHT}$ (−1165mV)
$V_{IHmax}$ (−880mV)
$V_{BB}$ (−1320mV)
DF05450S

**NOTES:**

| | |
|---|---|
| $V_{IHmax}$ | – Maximum HIGH level input voltage (the most positive $V_{IH}$). |
| $V_{IHT}$ | – HIGH level input threshold voltage. |
| $V_{ILT}$ | – LOW level input threshold voltage. |
| $V_{ILmin}$ | – Minimum LOW level input voltage (the most negative $V_{IL}$). |
| $V_{OHmax}$ | – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition. |
| $V_{OHmin}$ | – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition. |
| $V_{OHT}$ | – HIGH level output threshold voltage with the inputs set to their respective threshold levels. |
| $V_{OLT}$ | – LOW level output threshold voltage with the inputs set to their respective threshold levels. |
| $V_{OLmax}$ | – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions. |
| $V_{OLmin}$ | – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions. |
| $V_{BB}$ | – Reference bias voltage. The internally generated reference voltage which is used to set the input and output threshold level. |

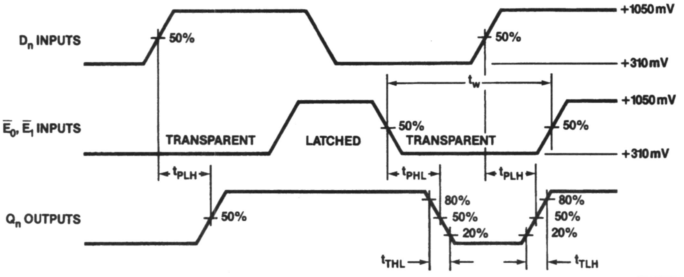
**Figure 4. Transfer Characteristics**

## AC ELECTRICAL CHARACTERISTICS

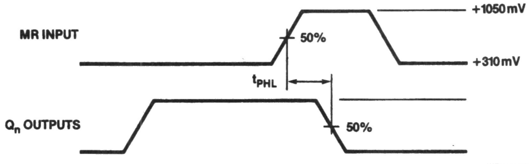
**Ceramic DIP** $V_{CC1} = V_{CC2} = \text{GND}$, $V_{EE} = -5.2\text{V} \pm 5\%$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +75°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$D_n$ to output | 1.00<br>1.00 | 3.40<br>3.40 | 1.00<br>1.00 | 3.40<br>3.40 | 1.00<br>1.00 | 3.40<br>3.40 | ns<br>ns | Figs. 5, 6, 7 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$\overline{E}_1$, $\overline{E}_2$ to output | 1.00<br>1.00 | 4.30<br>4.30 | 1.00<br>1.00 | 4.30<br>4.30 | 1.00<br>1.00 | 4.30<br>4.30 | ns<br>ns | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>C to output | 1.00<br>1.00 | 3.90<br>3.90 | 1.00<br>1.00 | 3.90<br>3.90 | 1.00<br>1.00 | 3.90<br>3.90 | ns<br>ns | |
| $t_{TLH}$<br>$t_{THL}$ | Transition time<br>20% to 80%, 80% to 20% | 0.90<br>0.90 | 3.50<br>3.50 | 1.00<br>1.00 | 3.50<br>3.50 | 0.90<br>0.90 | 3.50<br>3.50 | ns<br>ns | |
| $t_s$ | Setup time, $D_n$ to $\overline{E}_n$ | 2.5 | | 2.5 | | 2.5 | | ns | |
| $t_h$ | Hold time, $D_n$ to $\overline{E}_n$ | 0.5 | | 0.5 | | 0.5 | | ns | |

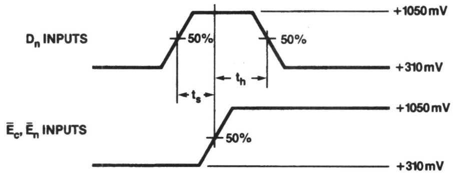
## AC WAVEFORMS


D$_n$ INPUTS
50%
50%
+1050mV
+310mV
$t_w$
$\overline{E}_0$, $\overline{E}_1$ INPUTS
TRANSPARENT
LATCHED
50%
TRANSPARENT
50%
+1050mV
+310mV
$t_{PLH}$
$t_{PHL}$
$t_{PLH}$
Q$_n$ OUTPUTS
50%
80%
50%
20%
80%
50%
20%
$t_{THL}$
$t_{TLH}$
WF13120S

a. Enable Timing


MR INPUT
50%
+1050mV
+310mV
$t_{PHL}$
Q$_n$ OUTPUTS
50%
WF13130S

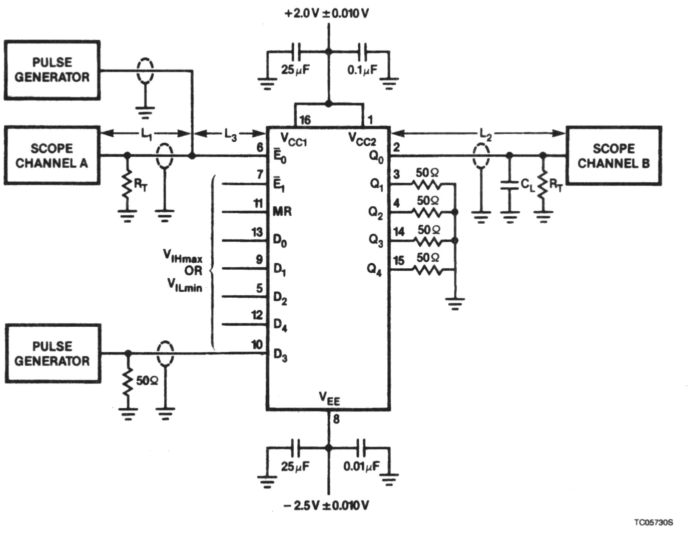
b. Clear Timing


D$_n$ INPUTS
50%
50%
+1050mV
+310mV
$t_h$
$t_s$
$\overline{E}_c$, $\overline{E}_n$ INPUTS
50%
+1050mV
+310mV
WF13140S

c. Data Setup and Hold Times

Figure 5

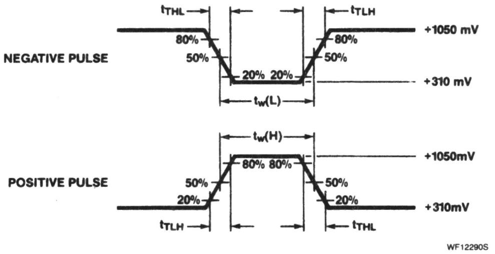
## TEST CIRCUITS AND WAVEFORMS


+2.0V ±0.010V
25μF
0.1μF
PULSE GENERATOR
SCOPE CHANNEL A
L1
L3
RT
16
1
VCC1
VCC2
6
Ē0
Q0
2
7
Ē1
Q1
3
11
MR
Q2
4
13
D0
Q3
14
9
D1
Q4
15
5
D2
12
D4
10
D3
50Ω
VIHmax OR VILmin
PULSE GENERATOR
50Ω
VEE
8
L2
SCOPE CHANNEL B
CL
RT
25μF
0.01μF
−2.5V ±0.010V
TC05730S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1μF and 25μF from GND to $V_{CC}$, 0.01μF and 25μF from GND to $V_{EE}$. (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance $\leqslant$ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ±1% or better.
11. Pin connections are for Flat Pack and in parentheses for Ceramic DIP.

Figure 6. Test Circuit


NEGATIVE PULSE
tTHL
tTLH
80%
50%
20%
20%
80%
50%
+1050 mV
+310 mV
tw(L)
tw(H)
POSITIVE PULSE
80%
80%
50%
20%
50%
20%
+1050mV
+310mV
tTLH
tTHL
WF12290S

| INPUT PULSE REQUIREMENTS<br>$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -2.5V \pm 0.010V$, $V_T$ = GND (0V) | | | | | |
|---|---|---|---|---|---|
| **Family** | **Amplitude** | **Rep Rate** | **Pulse Width** | **$t_{TLH}$** | **$t_{THL}$** |
| 100K ECL | 740mVp-p | 1MHz | 500ns | 0.7 ±0.1ns | 0.7 ±0.1ns |

Figure 7. Input Pulse Definition

**Signetics**

# 100179
# Carry Look-Ahead Generator

***Preliminary Specification***

**ECL Products**

## DESCRIPTION

The 100179 is a high-speed Carry Look-Ahead Generator intended for use with the F100180 6-Bit Fast Adder and the F100181 4-Bit ALU.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 100179 | 1.9ns | 150mA |

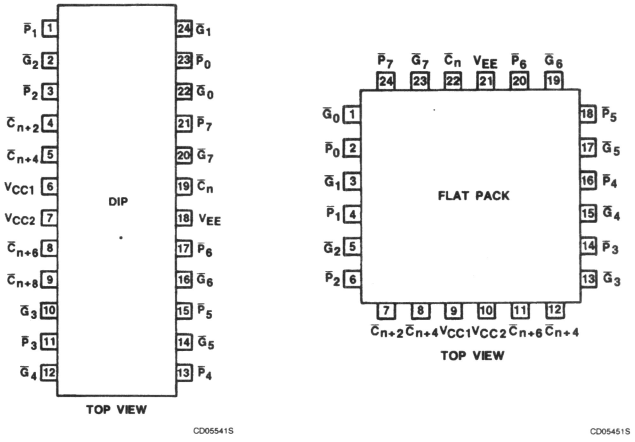
## ORDERING CODE

| PACKAGES | $V_{CC1} = V_{CC2}$ = GND, $V_{EE}$ = −4.2V to −4.8V<br>$T_A$ = 0°C to + 85°C |
|---|---|
| Ceramic DIP | 100179F |
| Ceramic Flat Pack | 100179Y |

## PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $C_n$ | Carry Input (active LOW) |
| $\overline{P}_0 - \overline{P}_7$ | Carry Look-Ahead Propagate Input (Active LOW) |
| $\overline{G}_0 - \overline{G}_7$ | Carry Look-Ahead Generate Input (Active LOW) |
| $C_{n+2}$, $C_{n+4}$ | Carry Outputs |
| $C_{n+6}$, $C_{n+8}$ | Carry Outputs |

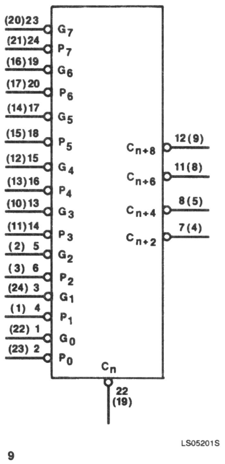
## PIN CONFIGURATIONS



P̄1 1
Ḡ2 2
P̄2 3
C̄n+2 4
C̄n+4 5
VCC1 6
VCC2 7
C̄n+6 8
C̄n+8 9
Ḡ3 10
P̄3 11
Ḡ4 12
24 Ḡ1
23 P̄0
22 Ḡ0
21 P̄7
20 Ḡ7
19 C̄n
18 VEE
17 P̄6
16 Ḡ6
15 P̄5
14 Ḡ5
13 P̄4
DIP
TOP VIEW
CD05541S
P̄7 Ḡ7 C̄n VEE P̄6 Ḡ6
24 23 22 21 20 19
Ḡ0 1
P̄0 2
Ḡ1 3
P̄1 4
Ḡ2 5
P̄2 6
18 P̄5
17 Ḡ5
16 P̄4
15 Ḡ4
14 P̄3
13 Ḡ3
FLAT PACK
7 8 9 10 11 12
C̄n+2 C̄n+4 VCC1 VCC2 C̄n+6 C̄n+4
TOP VIEW
CD05451S

Figure 1

## LOGIC SYMBOL

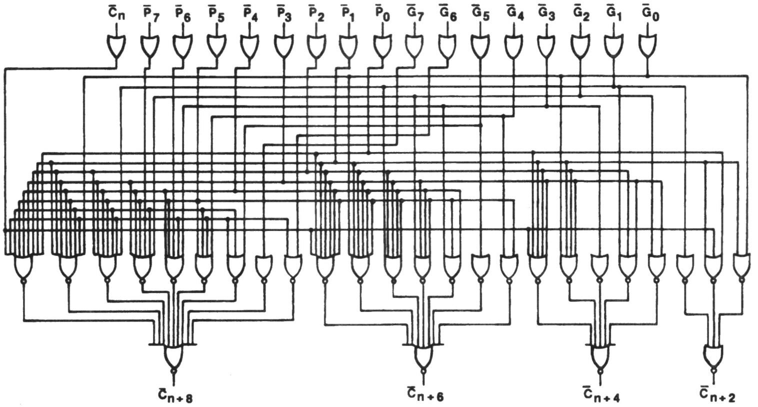


(20)23 G7
(21)24 P7
(16)19 G6
(17)20 P6
(14)17 G5
(15)18 P5
(12)15 G4
(13)16 P4
(10)13 G3
(11)14 P3
(2) 5 G2
(3) 6 P2
(24) 3 G1
(1) 4 P1
(22) 1 G0
(23) 2 P0
Cn+8 12(9)
Cn+6 11(8)
Cn+4 8(5)
Cn+2 7(4)
Cn 22 (19)
LS05201S

$V_{CC1}$ = 9
$V_{CC2}$ = 10
$V_{EE}$ = 21
Pin connections are for Flat Pack and in parentheses for Ceramic DIP package.

Figure 2

## Carry Look-Ahead Generator 100179


$\bar{C}_n$
$\bar{P}_7$
$\bar{P}_6$
$\bar{P}_5$
$\bar{P}_4$
$\bar{P}_3$
$\bar{P}_2$
$\bar{P}_1$
$\bar{P}_0$
$\bar{G}_7$
$\bar{G}_6$
$\bar{G}_5$
$\bar{G}_4$
$\bar{G}_3$
$\bar{G}_2$
$\bar{G}_1$
$\bar{G}_0$
$\bar{C}_{n+8}$
$\bar{C}_{n+6}$
$\bar{C}_{n+4}$
$\bar{C}_{n+2}$

LD02730S

**Figure 3. Logic Diagram**

7

## FUNCTION TABLES

### $\overline{C}_{n+2}$ OUTPUT

| INPUTS | | | | | OUTPUT |
|---|---|---|---|---|---|
| $\overline{C}_n$ | $\overline{G}_0$ | $\overline{P}_0$ | $\overline{G}_1$ | $\overline{P}_1$ | $\overline{C}_{n+2}$ |
| X | X | X | L | X | L |
| X | L | X | X | L | L |
| L | X | L | X | L | L |
| All other combinations | | | | | H |

$\overline{C}_{n+2} = \overline{G}_1 \bullet (\overline{P}_1 + \overline{G}_0) \bullet (\overline{P}_1 + \overline{P}_0 + \overline{C}_n)$

H = HIGH Voltage Level

L = LOW Voltage Level

X = Don't Care

### $\overline{C}_{n+4}$ OUTPUT

| INPUTS | | | | | | | | | OUTPUT |
|---|---|---|---|---|---|---|---|---|---|
| $\overline{C}_n$ | $\overline{G}_0$ | $\overline{P}_0$ | $\overline{G}_1$ | $\overline{P}_1$ | $\overline{G}_2$ | $\overline{P}_2$ | $\overline{G}_3$ | $\overline{P}_3$ | $\overline{C}_{n+4}$ |
| X | X | X | X | X | X | X | L | X | L |
| X | X | X | X | X | L | X | X | L | L |
| X | X | X | L | X | X | L | X | L | L |
| X | L | X | X | L | X | L | X | L | L |
| L | X | L | X | L | X | L | X | L | L |
| All other combinations | | | | | | | | | H |

$\overline{C}_{n+4} = \overline{G}_3 \bullet (\overline{P}_3 + \overline{G}_2) \bullet (\overline{P}_3 + \overline{P}_2 + \overline{G}_1) \bullet (\overline{P}_3 + \overline{P}_2 + \overline{P}_1 + \overline{G}_0) \bullet (\overline{P}_3 + \overline{P}_2 + \overline{P}_1 + \overline{P}_0 + \overline{C}_n)$

### $\overline{C}_{n+6}$ OUTPUT

| INPUTS | | | | | | | | | | | | | OUTPUT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $\overline{C}_n$ | $\overline{G}_0$ | $\overline{P}_0$ | $\overline{G}_1$ | $\overline{P}_1$ | $\overline{G}_2$ | $\overline{P}_2$ | $\overline{G}_3$ | $\overline{P}_3$ | $\overline{G}_4$ | $\overline{P}_4$ | $\overline{G}_5$ | $\overline{P}_5$ | $\overline{C}_{n+6}$ |
| X | X | X | X | X | X | X | X | X | X | X | L | X | L |
| X | X | X | X | X | X | X | X | X | L | X | X | L | L |
| X | X | X | X | X | X | X | L | X | X | L | X | L | L |
| X | X | X | X | X | L | X | X | L | X | L | X | L | L |
| X | X | X | L | X | X | L | X | L | X | L | X | L | L |
| X | L | X | X | L | X | L | X | L | X | L | X | L | L |
| L | X | L | X | L | X | L | X | L | X | L | X | L | L |
| All other combinations | | | | | | | | | | | | | H |

$\overline{C}_{n+6} = \overline{G}_5 \bullet (\overline{P}_5 + \overline{G}_4) \bullet (\overline{P}_5 + \overline{P}_4 + \overline{G}_3) \bullet (\overline{P}_5 + \overline{P}_4 + \overline{P}_3 + \overline{G}_2) \bullet (\overline{P}_5 + \overline{P}_4 + \overline{P}_3 + \overline{P}_2 + \overline{G}_1) \bullet (\overline{P}_5 + \overline{P}_4 + \overline{P}_3 + \overline{P}_2 + \overline{P}_1 + \overline{G}_0) \bullet (\overline{P}_5 + \overline{P}_4 + \overline{P}_3 + \overline{P}_2 + \overline{P}_1 + \overline{P}_0 + \overline{C}_n)$

### $\overline{C}_{n+8}$ OUTPUT

| INPUTS | | | | | | | | | | | | | | | | | OUTPUT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $\overline{C}_n$ | $\overline{G}_0$ | $\overline{P}_0$ | $\overline{G}_1$ | $\overline{P}_1$ | $\overline{G}_2$ | $\overline{P}_2$ | $\overline{G}_3$ | $\overline{P}_3$ | $\overline{G}_4$ | $\overline{P}_4$ | $\overline{G}_5$ | $\overline{P}_5$ | $\overline{G}_6$ | $\overline{P}_6$ | $\overline{G}_7$ | $\overline{P}_7$ | $\overline{C}_{n+8}$ |
| X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | L | X | L |
| X | X | X | X | X | X | X | X | X | X | X | X | X | L | X | X | L | L |
| X | X | X | X | X | X | X | X | X | X | X | L | X | X | L | X | L | L |
| X | X | X | X | X | X | X | X | X | L | X | X | L | X | L | X | L | L |
| X | X | X | X | X | X | X | L | X | X | L | X | L | X | L | X | L | L |
| X | X | X | X | X | L | X | X | L | X | L | X | L | X | L | X | L | L |
| X | X | X | L | X | X | L | X | L | X | L | X | L | X | L | X | L | L |
| X | L | X | X | L | X | L | X | L | X | L | X | L | X | L | X | L | L |
| L | X | L | X | L | X | L | X | L | X | L | X | L | X | L | X | L | L |
| All other combinations | | | | | | | | | | | | | | | | | H |

$\overline{C}_{n+8} = \overline{G}_7 \bullet (\overline{P}_7 + \overline{G}_6) \bullet (\overline{P}_7 + \overline{P}_6 + \overline{G}_5) \bullet (\overline{P}_7 + \overline{P}_6 + \overline{P}_5 + \overline{G}_4) \bullet (\overline{P}_7 + \overline{P}_6 + \overline{P}_5 + \overline{P}_4 + \overline{G}_3) \bullet (\overline{P}_7 + \overline{P}_6 + \overline{P}_5 + \overline{P}_4 + \overline{P}_3 + \overline{G}_2) \bullet (\overline{P}_7 + \overline{P}_6 + \overline{P}_5 + \overline{P}_4 + \overline{P}_3 + \overline{P}_2 + \overline{G}_1) \bullet (\overline{P}_7 + \overline{P}_6 + \overline{P}_5 + \overline{P}_4 + \overline{P}_3 + \overline{P}_2 + \overline{P}_1 + \overline{G}_0) \bullet (\overline{P}_7 + \overline{P}_6 + \overline{P}_5 + \overline{P}_4 + \overline{P}_3 + \overline{P}_2 + \overline{P}_1 + \overline{P}_0 + \overline{C}_n)$

H = HIGH Voltage Level

L = LOW Voltage Level

X = Don't Care

## Carry Look-Ahead Generator 100179

**ABSOLUTE MAXIMUM RATINGS** (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | 100K ECL | UNIT |
|---|---|---|---|
| $V_{EE}$ | Supply voltage ($V_{CC1} = V_{CC2}$ = GND) | −7.0 to 0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | $V_{EE}$ to +0.5 | V |
| $I_O$ | Output source current | −55 | mA |
| $T_S$ | Storage temperature | −65 to +150 | °C |
| $T_J$ | Maximum junction temperature | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | | 100K ECL | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | Min | Nom | Max | |
| $V_{CC1}$,<br>$V_{CC2}$ | Circuit ground | | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | −4.2 | −4.5 | −4.8 | V |
| $V_{EE}$ | Supply voltage (negative) When operating with 10K ECL Family | | | | | −5.7 | V |
| $V_{IH}$ | HIGH level input voltage | $V_{CC1} = V_{CC2}$ = GND<br>$T_A$ = 0°C to +85°C | $V_{EE}$ = −4.2V | −1150 | | −880 | mV |
| | | | $V_{EE}$ = −4.5V | −1165 | | | |
| | | | $V_{EE}$ = −4.8V | | | | |
| $V_{IHT}$ | HIGH level input threshold voltage | | $V_{EE}$ = −4.2V | −1150 | | | mV |
| | | | $V_{EE}$ = −4.5V | −1165 | | | mV |
| | | | $V_{EE}$ = −4.8V | | | | |
| $V_{ILT}$ | LOW level input threshold voltage | | $V_{EE}$ = −4.2V | | | −1475 | mV |
| | | | $V_{EE}$ = −4.5V | | | | |
| | | | $V_{EE}$ = −4.8V | | | −1490 | mV |
| $V_{IL}$ | LOW level input voltage | | $V_{EE}$ = −4.2V | −1810 | | −1475 | mV |
| | | | $V_{EE}$ = −4.5V | | | | |
| | | | $V_{EE}$ = −4.8V | | | −1490 | |
| $T_A$ | Operating ambient temperature | | | 0 | +25 | +85 | °C |

**NOTE:**
When operating at other than specified voltages (−4.2V, −4.5V, −4.8V) DC & AC Characteristics will vary slightly from specified values.

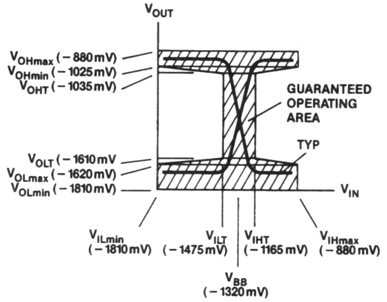
# Carry Look-Ahead Generator 100179

## DC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = \text{GND}$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$, $T_A = 0°C$ to $+85°C$ unless otherwise specified[1,4]

| PARAMETER | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] | |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | $V_{EE} = -4.2V$ | -1025 | | -870 | mV | $V_{IN} = V_{IHmax}$ or $V_{IN} = V_{ILmax}$ | Loading with 50Ω to -2.0V ±0.010V |
| | | $V_{EE} = -4.5V$ | -1025 | -955 | -880 | mV | | |
| | | $V_{EE} = -4.8V$ | -1035 | | -880 | mV | | |
| $V_{OHT}$ | HIGH level output threshold voltage | $V_{EE} = -4.2V$ | -1035 | | | mV | $V_{IN} = V_{IHT}$[3] or $V_{IN} = V_{ILT}$[3] | |
| | | $V_{EE} = -4.5V$ | -1035 | | | mV | | |
| | | $V_{EE} = -4.8V$ | -1045 | | | mV | | |
| $V_{OLT}$ | LOW level output threshold voltage | $V_{EE} = -4.2V$ | | | -1590 | mV | $V_{IN} = V_{IHT}$[3] or $V_{IN} = V_{ILT}$[3] | |
| | | $V_{EE} = -4.5V$ | | | -1610 | mV | | |
| | | $V_{EE} = -4.8V$ | | | -1610 | mV | | |
| $V_{OL}$ | LOW level output voltage | $V_{EE} = -4.2V$ | -1810 | | -1600 | mV | $V_{IN} = V_{IHmax}$ or $V_{IN} = V_{ILmin}$ | |
| | | $V_{EE} = -4.5V$ | -1810 | -1705 | -1620 | mV | | |
| | | $V_{EE} = -4.8V$ | -1830 | | -1620 | mV | | |
| $I_{IH}$ | HIGH level input current | $\overline{C}_n$, $\overline{G}_0 - \overline{G}_7$ | | | 250 | μA | $V_{IN} = V_{IHmax}$ | |
| | | $P_0 - P_7$ | | | 340 | μA | | |
| $I_{IL}$ | LOW level input current | | 0.5 | | | μA | $V_{IN} = V_{ILmin}$ | |
| $-I_{EE}$ | $V_{EE}$ supply current | | 100 | 150 | 220 | mA | Inputs open | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to Section 3 Testing, DC testing.
3. Only one input at a time should be at the threshold level; all other inputs should be at a $V_{IHmax}$ or $V_{ILmin}$.
4. The specified limited shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are in the DC Operating Conditions and defined in Figure 4.



**NOTES:**

$V_{IHmax}$ – Maximum HIGH level input voltage (the most positive $V_{IH}$).
$V_{IHT}$ – HIGH level input threshold voltage.
$V_{ILT}$ – LOW level input threshold voltage.
$V_{ILmin}$ – Minimum LOW level input voltage (the most negative $V_{IL}$).
$V_{OHmax}$ – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition.
$V_{OHmin}$ – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition.
$V_{OHT}$ – HIGH level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLT}$ – LOW level output threshold voltage with the inputs set to their respective threshold levels.
$V_{OLmax}$ – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions.
$V_{OLmin}$ – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions.
$V_{BB}$ – Reference bias voltage. The internally generated reference voltage which is used to set the input and output threshold level.

Figure 4. Transfer Characteristics

## Carry Look-Ahead Generator 100179

### AC ELECTRICAL CHARACTERISTICS

**Ceramic DIP** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 1.10 | 2.90 | 1.10 | 2.90 | 1.10 | 3.00 | ns | Figs. 5, 6, 7 |
| $t_{PHL}$ | $\overline{C}_n$, $\overline{G}_0 - \overline{G}_7$, $\overline{P}_0 - \overline{P}_7$ to $\overline{C}_{n+4}$ | 1.10 | 2.90 | 1.10 | 2.90 | 1.10 | 3.00 | ns | |
| $t_{TLH}$ | Transition time | 0.45 | 1.80 | 0.45 | 1.80 | 0.45 | 1.80 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.80 | 0.45 | 1.80 | 0.45 | 1.80 | ns | |

**Ceramic DIP** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V \pm 5\%$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 1.10 | 2.90 | 1.10 | 2.90 | 1.10 | 3.00 | ns | Figs. 5, 6, 7 |
| $t_{PHL}$ | $C_n$, $G_0 - G_7$, $P_0 - P_7$ to $C_{n+4}$ | 1.10 | 2.90 | 1.10 | 2.90 | 1.10 | 3.00 | ns | |
| $t_{TLH}$ | Transition time | 0.45 | 1.80 | 0.45 | 1.80 | 0.45 | 1.80 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.80 | 0.45 | 1.80 | 0.45 | 1.80 | ns | |

**Flat Pack** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 1.10 | 2.70 | 1.10 | 2.70 | 1.10 | 2.80 | ns | Figs. 5, 6, 7 |
| $t_{PHL}$ | $C_n$, $G_0 - G_7$, $P_0 - P_7$ to $C_{n+4}$ | 1.10 | 2.70 | 1.10 | 2.70 | 1.10 | 2.80 | ns | |
| $t_{TLH}$ | Transition time | 0.45 | 1.70 | 0.45 | 1.70 | 0.45 | 1.70 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.70 | 0.45 | 1.70 | 0.45 | 1.70 | ns | |

**Flat Pack** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V \pm 5\%$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 1.10 | 2.70 | 1.10 | 2.70 | 1.10 | 2.80 | ns | Figs. 5, 6, 7 |
| $t_{PHL}$ | $\overline{C}_n$, $\overline{G}_0 - \overline{G}_7$, $\overline{P}_0 - \overline{P}_7$ to $C_{n+4}$ | 1.10 | 2.70 | 1.10 | 2.70 | 1.10 | 2.80 | ns | |
| $t_{TLH}$ | Transition time | 0.45 | 1.70 | 0.45 | 1.70 | 0.45 | 1.70 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.70 | 0.45 | 1.70 | 0.45 | 1.70 | ns | |

### AC WAVEFORMS

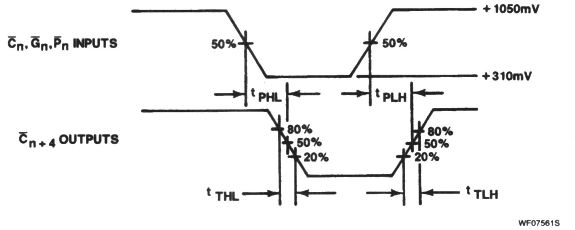
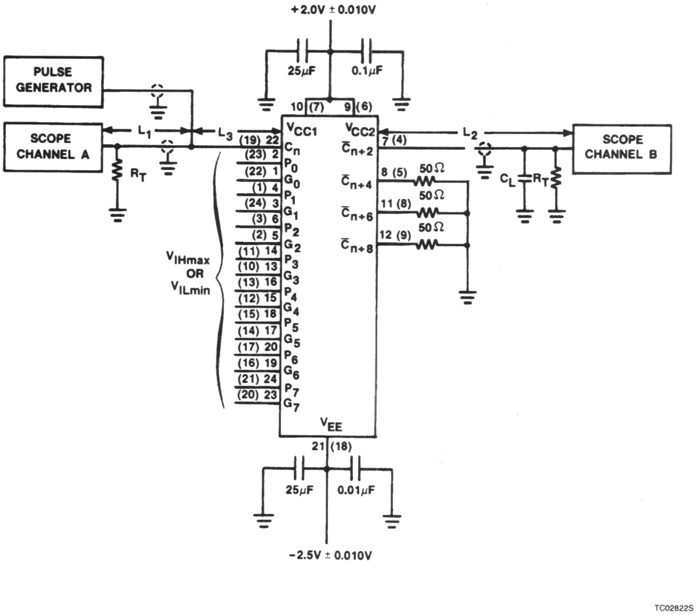

+1050mV
$\overline{C}_n, \overline{G}_n, \overline{P}_n$ INPUTS
50%
50%
+310mV
$t_{PHL}$
$t_{PLH}$
$\overline{C}_{n+4}$ OUTPUTS
80%
50%
20%
80%
50%
20%
$t_{THL}$
$t_{TLH}$
WF07561S

Figure 5. Propagation Delay And Transition Times For Data Inputs To Outputs

# Carry Look-Ahead Generator 100179

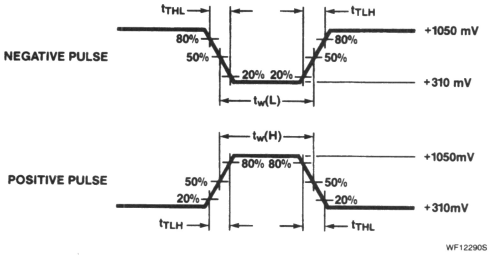
## TEST CIRCUITS AND WAVEFORMS


+2.0V ± 0.010V
25μF
0.1μF
PULSE GENERATOR
SCOPE CHANNEL A
L1
L3
RT
10 (7)
9 (6)
VCC1
VCC2
(19) 22 Cn
(23) 2 P0
(22) 1 G0
(1) 4 P1
(24) 3 G1
(3) 6 P2
(2) 5 G2
(11) 14 P3
(10) 13 G3
(13) 16 P4
(12) 15 G4
(15) 18 P5
(14) 17 G5
(17) 20 P6
(16) 19 G6
(21) 24 P7
(20) 23 G7
VIHmax OR VILmin
C̄n+2 7 (4)
C̄n+4 8 (5)
C̄n+6 11 (8)
C̄n+8 12 (9)
50Ω
50Ω
50Ω
L2
SCOPE CHANNEL B
CL
RT
VEE
21 (18)
25μF
0.01μF
-2.5V ± 0.010V
TC02822S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -2.5V \pm 0.010V$.
2. Decoupling 0.1μF and 25μF from GND to $V_{CC}$, 0.01μF and 25μF from GND to $V_{EE}$. (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance ⩽ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ±1% or better.
11. Pin connections for Flat Pack and in parentheses for Ceramic DIP package.

Figure 6. AC Test Circuit For 100179


NEGATIVE PULSE
tTHL
tTLH
80%
50%
20% 20%
80%
50%
+1050 mV
+310 mV
tw(L)
tw(H)
POSITIVE PULSE
80% 80%
50%
20%
50%
20%
+1050mV
+310mV
tTLH
tTHL
WF12290S

| INPUT PULSE REQUIREMENTS<br>$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -2.5V \pm 0.010V$, $V_T$ = GND (0V) | | | | | |
|---|---|---|---|---|---|
| Family | Amplitude | Rep Rate | Pulse Width | $t_{TLH}$ | $t_{THL}$ |
| 100K ECL | 740mVp-p | 1MHz | 500ns | 0.7 ±0.1ns | 0.7 ±0.1ns |

Figure 7. Input Pulse Definition

**Signetics**

# 100180
## Adder

**High-Speed 6-Bit Adder**
***Product Specification***

**ECL Products**

### DESCRIPTION

The 100180 is a High-Speed 6-bit Adder which performs a full 6-bit addition of 2 operands in 2ns. The inputs are: carrying (CN) (active LOW), operands A (An), operands B (Bn); the outputs are: function (Fn), carry generate (G) (active LOW), carry propagate (P) (active LOW).

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 100180 | 2.35ns | 205mA |

### ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} =$ GND; $V_{EE} = -4.2V$ to $-4.8V$<br>$T_A = 0°C$ to $+85°C$ |
|---|---|
| Ceramic DIP | 100180F |
| Ceramic Flat Pack | 100180Y |

### PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $A_0 - A_5$ | Operand A Inputs |
| $B_0 - B_5$ | Operand B Inputs |
| $\overline{C}_n$ | Carry Input (Active LOW) |
| $\overline{G}$ | Carry Generate Output (Active LOW) |
| $\overline{P}$ | Carry Propagate Output (Active LOW) |
| $F_0 - F_5$ | Function Outputs |

### PIN CONFIGURATION

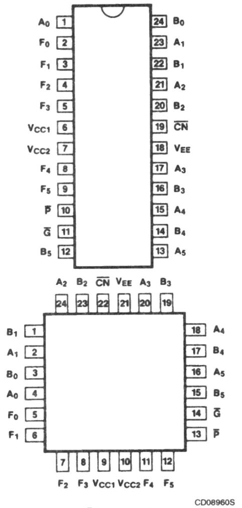

A0 1
F0 2
F1 3
F2 4
F3 5
VCC1 6
VCC2 7
F4 8
F5 9
P̄ 10
Ḡ 11
B5 12
24 B0
23 A1
22 B1
21 A2
20 B2
19 CN̄
18 VEE
17 A3
16 B3
15 A4
14 B4
13 A5
A2 B2 CN̄ VEE A3 B3
24 23 22 21 20 19
B1 1
A1 2
B0 3
A0 4
F0 5
F1 6
18 A4
17 B4
16 A5
15 B5
14 Ḡ
13 P̄
7 8 9 10 11 12
F2 F3 VCC1 VCC2 F4 F5
CD08960S

Figure 1

### LOGIC SYMBOL

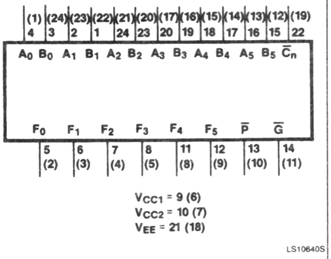
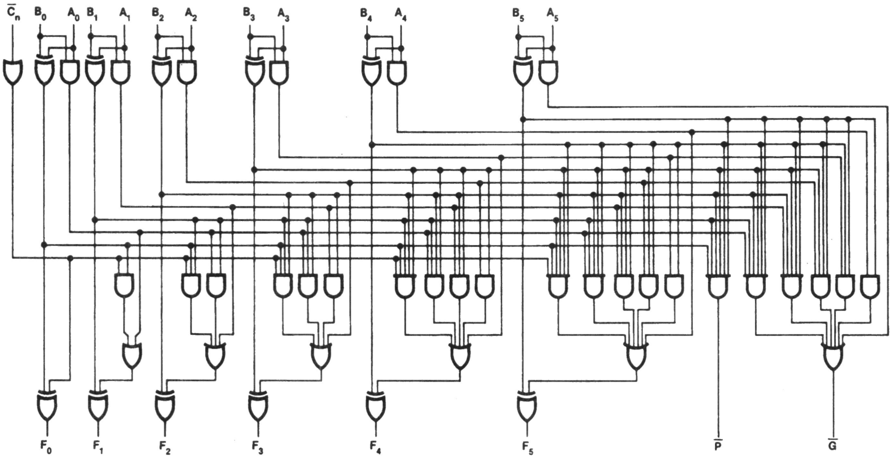

(1) (24) (23) (22) (21) (20) (17) (16) (15) (14) (13) (12) (19)
4 3 2 1 24 23 20 19 18 17 16 15 22
A0 B0 A1 B1 A2 B2 A3 B3 A4 B4 A5 B5 C̄n
F0 F1 F2 F3 F4 F5 P̄ Ḡ
5 6 7 8 11 12 13 14
(2) (3) (4) (5) (8) (9) (10) (11)
VCC1 = 9 (6)
VCC2 = 10 (7)
VEE = 21 (18)
LS10640S

Figure 2

# Adder

# 100180

## LOGIC DIAGRAM


$\overline{C}_n$
$B_0$
$A_0$
$B_1$
$A_1$
$B_2$
$A_2$
$B_3$
$A_3$
$B_4$
$A_4$
$B_5$
$A_5$
$F_0$
$F_1$
$F_2$
$F_3$
$F_4$
$F_5$
$\overline{P}$
$\overline{G}$

**LOGIC EQUATIONS**

$P_1 = A_1 \oplus B_1$

$G_1 = A_1B_1$

$I = 0, 1, 2, 3, 4, 5$

$F_0 = P_0 \oplus C_n$

$F_1 = P_1 \oplus (G_0 + P_0C_n)$

$F_2 = P_2 \oplus (G_1 + P_1G_0 + P_1P_0C_n)$

$F_3 = P_3 \oplus (G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n)$

$F_4 = P_4 \oplus (G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0 + P_3P_2P_1P_0C_n)$

$F_5 = P_5 \oplus (G_4 + P_4G_3 + P_4P_3G_2 + P_4P_3P_2G_1 + P_4P_3P_2P_1G_0 + P_4P_3P_2P_1P_0C_n$

$\overline{P} = \overline{P_0P_1P_2P_3P_4P_5}$

$\overline{G} = \overline{G_5 + P_5G_4 + P_5P_4G_3 + P_5P_4P_3G_2 + P_5P_4P_3P_2G_1 + P_5P_4P_3P_2P_1G_0}$

LD05320S

Figure 3

## ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| | PARAMETER | 100K ECL | UNIT |
|---|---|---|---|
| $V_{EE}$ | Supply voltage ($V_{CC1} = V_{CC2}$ = GND) | −7.0 to 0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | $V_{EE}$ to +0.5 | V |
| $I_O$ | Output source current | −55 | mA |
| $T_S$ | Storage temperature | −65 to +150 | °C |
| $T_J$ | Maximum junction temperature | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | | 100K ECL | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | −4.2 | −4.5 | −4.8 | V |
| $V_{EE}$ | Supply voltage (negative) when operating with 10K ECL family | | | | | −5.7 | V |
| $V_{IH}$ | HIGH level input voltage | $V_{CC1} = V_{CC2}$ = GND<br>$T_A$ = 0°C to +85°C | $V_{EE}$ = −4.2V | −1150 | | −880 | mV |
| | | | $V_{EE}$ = −4.5V | −1165 | | | |
| | | | $V_{EE}$ = −4.8V | | | | |
| $V_{IHT}$ | HIGH level input threshold voltage | | $V_{EE}$ = −4.2V | −1150 | | | mV |
| | | | $V_{EE}$ = −4.5V | −1165 | | | mV |
| | | | $V_{EE}$ = −4.8V | | | | |
| $V_{ILT}$ | LOW level input threshold voltage | | $V_{EE}$ = −4.2V | | | −1475 | mV |
| | | | $V_{EE}$ = −4.5V | | | | |
| | | | $V_{EE}$ = −4.8V | | | −1490 | mV |
| $V_{IL}$ | LOW level input voltage | | $V_{EE}$ = −4.2V | −1810 | | −1475 | mV |
| | | | $V_{EE}$ = −4.5V | | | | |
| | | | $V_{EE}$ = −4.8V | | | −1490 | |
| $T_A$ | Operating ambient temperature | | | 0 | +25 | +85 | °C |

**NOTE:**
When operating at other than specified voltages (−4.2V, −4.5V, −4.8V) DC & AC Characteristics will vary slightly from specified values.

## DC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$, $T_A = 0°C$ to $+85°C$ unless otherwise specified[1,3]

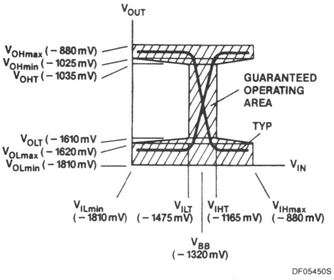
| PARAMETER | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] | |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | $V_{EE} = -4.2V$ | −1025 | | −870 | mV | $V_{IN} = V_{IHmax}$ or $V_{IN} = V_{ILmin}$ | Loading with 50Ω to −2.0V ±0.010V |
| | | $V_{EE} = -4.5V$ | −1025 | −955 | −880 | mV | | |
| | | $V_{EE} = -4.8V$ | −1035 | | −880 | mV | | |
| $V_{OHT}$ | HIGH level output threshold voltage | $V_{EE} = -4.2V$ | −1035 | | | mV | $V_{IN} = V_{IHmin}$ or $V_{IN} = V_{ILmax}$ | |
| | | $V_{EE} = -4.5V$ | −1035 | | | mV | | |
| | | $V_{EE} = -4.8V$ | −1045 | | | mV | | |
| $V_{OLT}$ | LOW level output threshold voltage | $V_{EE} = -4.2V$ | | | −1590 | mV | $V_{IN} = V_{IHmin}$ or $V_{IN} = V_{ILmax}$ | |
| | | $V_{EE} = -4.5V$ | | | −1610 | mV | | |
| | | $V_{EE} = -4.8V$ | | | −1610 | mV | | |
| $V_{OL}$ | LOW level output voltage | $V_{EE} = -4.2V$ | −1810 | | −1600 | mV | $V_{IN} = V_{IHmax}$ or $V_{IN} = V_{ILmin}$ | |
| | | $V_{EE} = -4.5V$ | −1810 | −1705 | −1620 | mV | | |
| | | $V_{EE} = -4.8V$ | −1830 | | −1620 | mV | | |
| $I_{IH}$ | Input high current | | | | 220 | µA | $V_{IN} = V_{IHmin}$ | |
| $I_{IL}$ | Input low current | | 0.5 | | | µA | $V_{IN} = V_{ILmin}$ | |
| $-I_{EE}$ | $V_{EE}$ supply current | | 135 | 205 | 290 | mA | Inputs open | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | $V_{EE} = -4.2V$<br>$T_A = +25°C$ | | | 0.035 | V/V | | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | | 0.070 | V/V | | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 4.

## Adder

## 100180



**NOTES:**

| | |
|---|---|
| $V_{IHmax}$ | – Maximum HIGH level input voltage (the most positive $V_{IH}$). |
| $V_{IHT}$ | – HIGH level input threshold voltage. |
| $V_{ILT}$ | – LOW level input threshold voltage. |
| $V_{ILmin}$ | – Minimum LOW level input voltage (the most negative $V_{IL}$). |
| $V_{OHmax}$ | – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition. |
| $V_{OHmin}$ | – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition. |
| $V_{OHT}$ | – HIGH level output threshold voltage with the inputs set to their respective threshold levels. |
| $V_{OLT}$ | – LOW level output threshold voltage with the inputs set to their respective threshold levels. |
| $V_{OLmax}$ | – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions. |
| $V_{OLmin}$ | – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions. |
| $V_{BB}$ | – Reference bias voltage. The internally generated reference voltage which is used to set the input and output threshold level. |

**Figure 4. Transfer Characteristics**

## AC ELECTRICAL CHARACTERISTICS

### Ceramic DIP $V_{CC1} = V_{CC2} =$ GND, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 1.10 | 4.70 | 1.10 | 4.60 | 1.10 | 4.70 | ns | Figs. 5, 6, 7 |
| $t_{PHL}$ | $A_n$, $B_n$, to $F_n$ | 1.10 | 4.70 | 1.10 | 4.60 | 1.10 | 4.70 | ns | |
| $t_{PLH}$ | Propagation delay | 1.00 | 3.00 | 1.00 | 3.00 | 1.00 | 3.30 | ns | |
| $t_{PHL}$ | $A_n$, $B_n$, to $\overline{P}$ | 1.00 | 3.00 | 1.00 | 3.00 | 1.00 | 3.30 | ns | |
| $t_{PLH}$ | Propagation delay | 1.10 | 3.90 | 1.20 | 3.80 | 1.20 | 3.90 | ns | |
| $t_{PHL}$ | $A_n$, $B_n$, to $\overline{G}$ | 1.10 | 3.90 | 1.20 | 3.80 | 1.20 | 3.90 | ns | |
| $t_{PLH}$ | Propagation delay | 0.90 | 4.00 | 0.90 | 3.90 | 0.90 | 4.00 | ns | |
| $t_{PHL}$ | $\overline{G}$ to $F_n$ | 0.90 | 4.00 | 0.90 | 3.90 | 0.90 | 4.00 | ns | |
| $t_{TLH}$ | Transition time | 0.45 | 2.30 | 0.45 | 2.20 | 0.45 | 2.30 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 2.30 | 0.45 | 2.20 | 0.45 | 2.30 | ns | |

### Ceramic DIP $V_{CC1} = V_{CC2} =$ GND, $V_{EE} = -5.2V \pm 5\%$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 1.10 | 4.70 | 1.10 | 4.60 | 1.10 | 4.70 | ns | Figs. 5, 6, 7 |
| $t_{PHL}$ | $A_n$, $B_n$, to $F_n$ | 1.10 | 4.70 | 1.10 | 4.60 | 1.10 | 4.70 | ns | |
| $t_{PLH}$ | Propagation delay | 1.00 | 3.00 | 1.00 | 3.00 | 1.00 | 3.30 | ns | |
| $t_{PHL}$ | $A_n$, $B_n$, to $\overline{P}$ | 1.00 | 3.00 | 1.00 | 3.00 | 1.00 | 3.30 | ns | |
| $t_{PLH}$ | Propagation delay | 1.10 | 3.90 | 1.20 | 3.80 | 1.20 | 3.90 | ns | |
| $t_{PHL}$ | $A_n$, $B_n$, to $\overline{G}$ | 1.10 | 3.90 | 1.20 | 3.80 | 1.20 | 3.90 | ns | |
| $t_{PLH}$ | Propagation delay | 0.90 | 4.00 | 0.90 | 3.90 | 0.90 | 4.00 | ns | |
| $t_{PHL}$ | $\overline{G}$ to $F_n$ | 0.90 | 4.00 | 0.90 | 3.90 | 0.90 | 4.00 | ns | |
| $t_{TLH}$ | Transition time | 0.45 | 2.30 | 0.45 | 2.20 | 0.45 | 2.30 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 2.30 | 0.45 | 2.20 | 0.45 | 2.30 | ns | |

# Adder 100180

## AC ELECTRICAL CHARACTERISTICS

**Flat Pack** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 1.10 | 4.50 | 1.10 | 4.40 | 1.10 | 4.50 | ns | Figs. 5, 6, 7 |
| $t_{PHL}$ | $A_n$, $B_n$, to $F_n$ | 1.10 | 4.50 | 1.10 | 4.40 | 1.10 | 4.50 | ns | |
| $t_{PLH}$ | Propagation delay | 1.00 | 2.80 | 1.00 | 2.80 | 1.00 | 3.10 | ns | |
| $t_{PHL}$ | $A_n$, $B_n$, to $\overline{P}$ | 1.00 | 2.80 | 1.00 | 2.80 | 1.00 | 3.10 | ns | |
| $t_{PLH}$ | Propagation delay | 1.10 | 3.70 | 1.20 | 3.60 | 1.20 | 3.70 | ns | |
| $t_{PHL}$ | $A_n$, $B_n$, to $\overline{G}$ | 1.10 | 3.70 | 1.20 | 3.60 | 1.20 | 3.70 | ns | |
| $t_{PLH}$ | Propagation delay | 0.90 | 3.80 | 0.90 | 3.70 | 0.90 | 3.80 | ns | |
| $t_{PHL}$ | $\overline{G}$ to $F_n$ | 0.90 | 3.80 | 0.90 | 3.70 | 0.90 | 3.80 | ns | |
| $t_{TLH}$ | Transition time | 0.45 | 2.30 | 0.45 | 2.20 | 0.45 | 2.30 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 2.30 | 0.45 | 2.20 | 0.45 | 2.30 | ns | |

**Flat Pack** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V \pm 5\%$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 1.10 | 4.50 | 1.10 | 4.40 | 1.10 | 4.50 | ns | Figs. 5, 6, 7 |
| $t_{PHL}$ | $A_n$, $B_n$, to $F_n$ | 1.10 | 4.50 | 1.10 | 4.40 | 1.10 | 4.50 | ns | |
| $t_{PLH}$ | Propagation delay | 1.00 | 2.80 | 1.00 | 2.80 | 1.00 | 3.10 | ns | |
| $t_{PHL}$ | $A_n$, $B_n$, to $\overline{P}$ | 1.00 | 2.80 | 1.00 | 2.80 | 1.00 | 3.10 | ns | |
| $t_{PLH}$ | Propagation delay | 1.10 | 3.70 | 1.20 | 3.60 | 1.20 | 3.70 | ns | |
| $t_{PHL}$ | $A_n$, $B_n$, to $\overline{G}$ | 1.10 | 3.70 | 1.20 | 3.60 | 1.20 | 3.70 | ns | |
| $t_{PLH}$ | Propagation delay | 0.90 | 3.80 | 0.90 | 3.70 | 0.90 | 3.80 | ns | |
| $t_{PHL}$ | $\overline{G}$ to $F_n$ | 0.90 | 3.80 | 0.90 | 3.70 | 0.90 | 3.80 | ns | |
| $t_{TLH}$ | Transition time | 0.45 | 2.30 | 0.45 | 2.20 | 0.45 | 2.30 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 2.30 | 0.45 | 2.20 | 0.45 | 2.30 | ns | |

## AC WAVEFORMS

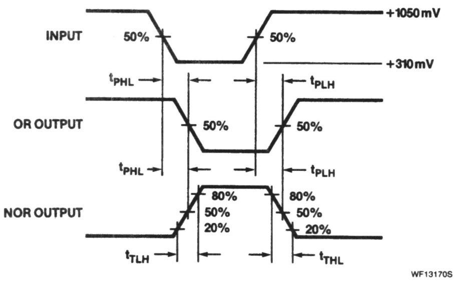
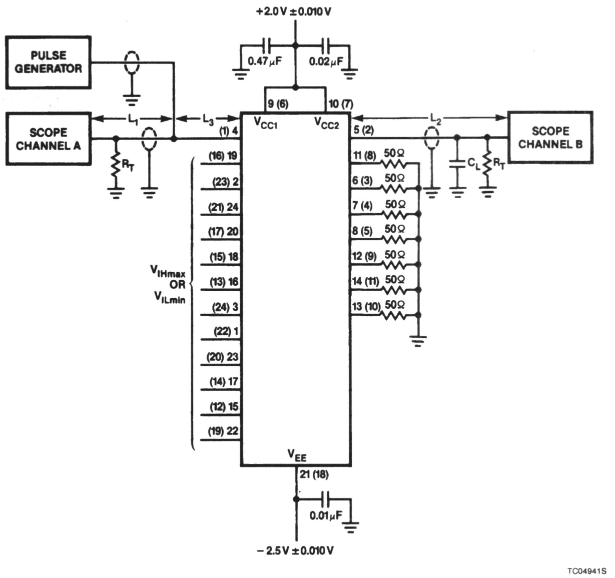


Figure 5. Propagation Delay and Transition Times

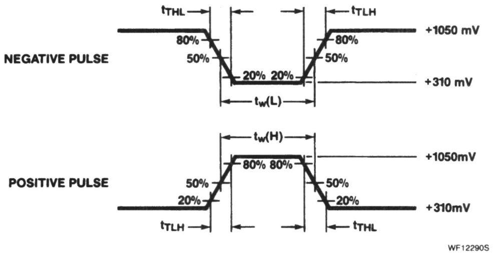
## TEST CIRCUITS AND WAVEFORMS


+2.0V ±0.010V
0.47μF
0.02μF
PULSE GENERATOR
SCOPE CHANNEL A
L1
L3
$R_T$
9 (6)
10 (7)
$V_{CC1}$
$V_{CC2}$
(1) 4
(16) 19
(23) 2
(21) 24
(17) 20
(15) 18
(13) 16
(24) 3
(22) 1
(20) 23
(14) 17
(12) 15
(19) 22
$V_{IHmax}$ OR $V_{ILmin}$
5 (2)
11 (8)
6 (3)
7 (4)
8 (5)
12 (9)
14 (11)
13 (10)
50Ω
L2
$C_L$
$R_T$
SCOPE CHANNEL B
$V_{EE}$
21 (18)
0.01μF
−2.5V ±0.010V
TC04941S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1μF and 25μF from GND to $V_{CC}$, 0.01μF and 25μF from GND to $V_{EE}$. (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T = 50\Omega$ terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance $\leqslant 3pF$.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.
11. Pin connections are for Flat Pack and in parentheses for Ceramic DIP.

**Figure 6. Test Circuit**


NEGATIVE PULSE
$t_{THL}$
$t_{TLH}$
80%
50%
20% 20%
80%
50%
+1050 mV
+310 mV
$t_w(L)$
POSITIVE PULSE
$t_w(H)$
80% 80%
50%
20%
50%
20%
+1050mV
+310mV
$t_{TLH}$
$t_{THL}$
WF12290S

**INPUT PULSE REQUIREMENTS**
**$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -2.5V \pm 0.010V$, $V_T$ = GND (0V)**

| Family | Amplitude | Rep Rate | Pulse Width | $t_{TLH}$ | $t_{THL}$ |
|---|---|---|---|---|---|
| 100K ECL | 740mVp-p | 1MHz | 500ns | 0.7 ±0.1ns | 0.7 ±0.1ns |

**Figure 7. Input Pulse Definition**

Signetics

# 100181
## ALU

**4-Bit Binary/BCD ALU**
***Preliminary Specification***

**ECL Products**

### DESCRIPTION

The 100181 is a 4-bit Binary/BCD Arithmetic Logic Unit which performs eight logic operations and eight arithmetic operations on two 4-bit words. Arithmetic and logic operations are selected by a 4-bit select input ($S_0$, $S_3$). The circuit performs BCD addition and subtraction, in supplement of binary arithmetic.

It contains four output latches, in order to increase operating speed. The latches are transparent, when the enable input ($\overline{E}$) is open. The internal look-ahead carry minimizes delay to the F outputs and to the ripple carry output ($\overline{C_{n+4}}$). Group carry look-ahead propagate (P) and generate ($\overline{G}$) outputs are also provided with independance from carry in ($\overline{C}_n$). P output goes low when a plus operation produces fifteen (or nine in BCD), or when a minus operation produces zero. $\overline{G}$ output goes low when the sum of word A and word B is greater than fifteen (or nine in BCD), or when their difference is greater than zero in a minus mode.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 100181 | 2.10ns | 205mA |

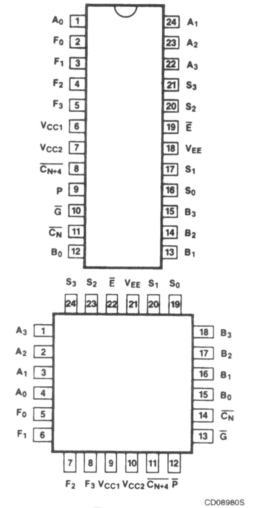
### ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} =$ GND; $V_{EE} = -4.2V$ to $-4.8V$<br>$T_A = 0°C$ to $+85°C$ |
|---|---|
| Ceramic DIP | 100181F |
| Ceramic Flat Pack | 100181Y |

### PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $A_0 - A_3$ | Word A Operand Inputs |
| $B_0 - B_3$ | Word B Operand Inputs |
| $\overline{C}_n$ | Carry Input (Active LOW) |
| $S_0 - S_3$ | Function Select Inputs |
| $\overline{E}$ | Enable Input (Active LOW) |
| $\overline{P}$ | Carry Lookahead Propagate Output (Active LOW) |
| $\overline{G}$ | Carry Lookahead Propagate Output (Active LOW) |
| $\overline{C_{n+4}}$ | Carry Output |
| $F_0 - F_3$ | Function Outputs |

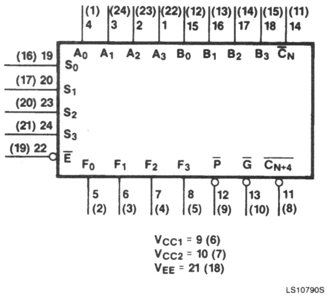
### PIN CONFIGURATION



A0 1
F0 2
F1 3
F2 4
F3 5
VCC1 6
VCC2 7
CN+4 8
P 9
G 10
CN 11
B0 12
24 A1
23 A2
22 A3
21 S3
20 S2
19 E
18 VEE
17 S1
16 S0
15 B3
14 B2
13 B1
S3 S2 E VEE S1 S0
24 23 22 21 20 19
A3 1
A2 2
A1 3
A0 4
F0 5
F1 6
18 B3
17 B2
16 B1
15 B0
14 CN
13 G
7 8 9 10 11 12
F2 F3 VCC1 VCC2 CN+4 P
CD08980S

Figure 1

### LOGIC SYMBOL



(1) 4
(24) 3
(23) 2
(22) 1
(12) 15
(13) 16
(14) 17
(15) 18
(11) 14
A0 A1 A2 A3 B0 B1 B2 B3 CN
(16) 19 S0
(17) 20 S1
(20) 23 S2
(21) 24 S3
(19) 22 E
F0 F1 F2 F3 P G CN+4
5 (2)
6 (3)
7 (4)
8 (5)
12 (9)
13 (10)
11 (8)
VCC1 = 9 (6)
VCC2 = 10 (7)
VEE = 21 (18)
LS10790S

Figure 2

## LOGIC DIAGRAM

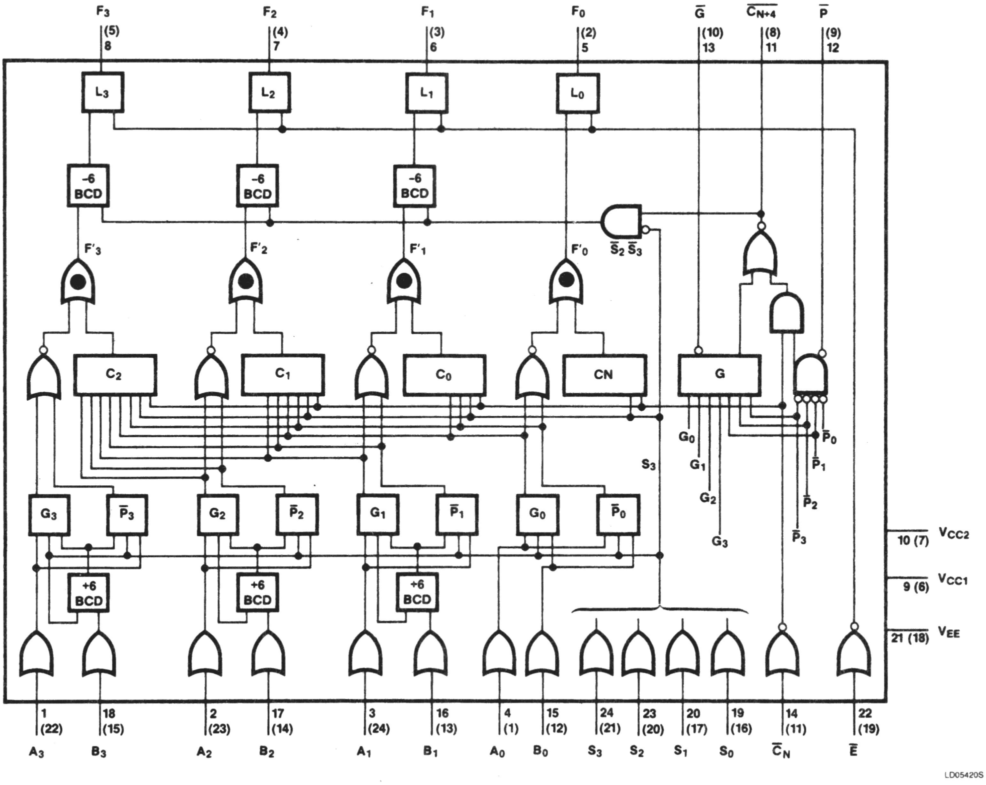

F3
(5)
8
F2
(4)
7
F1
(3)
6
F0
(2)
5
$\overline{G}$
(10)
13
$\overline{C_{N+4}}$
(8)
11
$\overline{P}$
(9)
12
L3
L2
L1
L0
-6 BCD
-6 BCD
-6 BCD
F'3
F'2
F'1
F'0
$\overline{S}_2 \overline{S}_3$
C2
C1
C0
CN
G
G0
G1
G2
G3
$\overline{P}_0$
$\overline{P}_1$
$\overline{P}_2$
$\overline{P}_3$
S3
G3
$\overline{P}_3$
G2
$\overline{P}_2$
G1
$\overline{P}_1$
G0
$\overline{P}_0$
+6 BCD
+6 BCD
+6 BCD
10 (7) VCC2
9 (6) VCC1
21 (18) VEE
1 (22) A3
18 (15) B3
2 (23) A2
17 (14) B2
3 (24) A1
16 (13) B1
4 (1) A0
15 (12) B0
24 (21) S3
23 (20) S2
20 (17) S1
19 (16) S0
14 (11) $\overline{C}_N$
22 (19) $\overline{E}$
LD05420S

Figure 3

## FUNCTION TABLE

| $S_3$ | $S_2$ | $S_1$ | $S_0$ | FUNCTIONS | |
|---|---|---|---|---|---|
| | | | | $\overline{C}_N$ = H | $\overline{C}_N$ = L |
| L | L | L | L | A plus B (BCD) | A plus B plus 1 (BCD) |
| L | L | L | H | A minus B (BCD) | A minus B plus 1 (BCD) |
| L | L | H | L | B minus A (BCD) | B minus A plus 1 (BCD) |
| L | L | H | H | O minus B (BCD) | O minus B plus 1 (BCD) |
| L | H | L | L | A plus B (Binary) | A plus B plus 1 (Binary) |
| L | H | L | H | A minus B (Binary) | A minus B plus 1 (Binary) |
| L | H | H | L | B minus A (Binary) | B minus A plus 1 (Binary) |
| L | H | H | H | O minus B (Binary) | O minus B plus 1 (Binary) |
| H | L | L | L | $F_n = A_nB_n + \overline{A}_n\overline{B}_n$ | ← SAME LOGIC |
| H | L | L | H | $F_n = A_n\overline{B_n} + \overline{A}_nB_n$ | |
| H | L | H | L | $F_n = A_n + B_n$ | |
| H | L | H | H | $F_n = A_n$ | |
| H | H | L | L | $F_n = \overline{B_n}$ | |
| H | H | L | H | $F_n = B_n$ | |
| H | H | H | L | $F_n = A_n \cdot B_n$ | |
| H | H | H | H | $F_n$ = LOW | |

Positive Logic:
L = LOW state (the less positive voltage level) = 0
H = HIGH state (the more positive voltage level) = 1

**NOTE:**
When $\overline{C}_N$ is low, BCD subtractions are performed in ten's complement, or binary subtractions are performed in one's complement.

## ALU 100181

**ABSOLUTE MAXIMUM RATINGS** (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | 100K ECL | UNIT |
|---|---|---|---|
| $V_{EE}$ | Supply voltage ($V_{CC1} = V_{CC2} = GND$) | −7.0 to 0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | $V_{EE}$ to +0.5 | V |
| $I_O$ | Output source current | −55 | mA |
| $T_S$ | Storage temperature | −65 to +150 | °C |
| $T_J$ | Maximum junction temperature | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | | 100K ECL | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | −4.2 | −4.5 | −4.8 | V |
| $V_{EE}$ | Supply voltage (negative) when operating with 10K ECL family | | | | | −5.7 | V |
| $V_{IH}$ | HIGH level input voltage | $V_{CC1} = V_{CC2} = GND$<br>$T_A = 0°C$ to $+85°C$ | $V_{EE} = -4.2V$ | −1150 | | −880 | mV |
| | | | $V_{EE} = -4.5V$ | −1165 | | | |
| | | | $V_{EE} = -4.8V$ | | | | |
| $V_{IHT}$ | HIGH level input threshold voltage | | $V_{EE} = -4.2V$ | −1150 | | | mV |
| | | | $V_{EE} = -4.5V$ | −1165 | | | mV |
| | | | $V_{EE} = -4.8V$ | | | | |
| $V_{ILT}$ | LOW level input threshold voltage | | $V_{EE} = -4.2V$ | | | −1475 | mV |
| | | | $V_{EE} = -4.5V$ | | | | |
| | | | $V_{EE} = -4.8V$ | | | −1490 | mV |
| $V_{IL}$ | LOW level input voltage | | $V_{EE} = -4.2V$ | −1810 | | −1475 | mV |
| | | | $V_{EE} = -4.5V$ | | | | |
| | | | $V_{EE} = -4.8V$ | | | −1490 | |
| $T_A$ | Operating ambient temperature | | | 0 | +25 | +85 | °C |

**NOTE:**
When operating at other than specified voltages (−4.2V, −4.5V, −4.8V) DC & AC Characteristics will vary slightly from specified values.

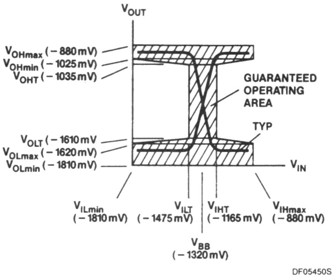
## DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = GND, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$, $T_A = 0°C$ to $+85°C$ unless otherwise specified[1,3]

| PARAMETER | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] | |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | $V_{EE} = -4.2V$ | -1025 | | -870 | mV | $V_{IN} = V_{IHmax}$ or $V_{IN} = V_{ILmin}$ | Loading with 50Ω to -2.0V ±0.010V |
| | | $V_{EE} = -4.5V$ | -1025 | -955 | -880 | mV | | |
| | | $V_{EE} = -4.8V$ | -1035 | | -880 | mV | | |
| $V_{OHT}$ | HIGH level output threshold voltage | $V_{EE} = -4.2V$ | -1035 | | | mV | $V_{IN} = V_{IHmin}$ or $V_{IN} = V_{ILmax}$ | |
| | | $V_{EE} = -4.5V$ | -1035 | | | mV | | |
| | | $V_{EE} = -4.8V$ | -1045 | | | mV | | |
| $V_{OLT}$ | LOW level output threshold voltage | $V_{EE} = -4.2V$ | | | -1590 | mV | $V_{IN} = V_{IHmin}$ or $V_{IN} = V_{ILmax}$ | |
| | | $V_{EE} = -4.5V$ | | | -1610 | mV | | |
| | | $V_{EE} = -4.8V$ | | | -1610 | mV | | |
| $V_{OL}$ | LOW level output voltage | $V_{EE} = -4.2V$ | -1810 | | -1600 | mV | $V_{IN} = V_{IHmax}$ or $V_{IN} = V_{ILmin}$ | |
| | | $V_{EE} = -4.5V$ | -1810 | -1705 | -1620 | mV | | |
| | | $V_{EE} = -4.8V$ | -1830 | | -1620 | mV | | |
| $I_{IH}$ | HIGH level input current | $S_n$, $\overline{E}$ | | | 220 | μA | $V_{IN} = V_{IHmax}$ | |
| | | Others | | | 350 | | | |
| $I_{IL}$ | LOW level input current | | 0.5 | | | μA | $V_{IN} = V_{ILmin}$ | |
| $-I_{EE}$ | $V_{EE}$ supply current | | 130 | 205 | 300 | mA | Inputs open | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | $V_{EE} = -4.2V$<br>$T_A = +25°C$ | | | 0.035 | V/V | | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | | 0.070 | V/V | | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 4.



**NOTES:**

| | |
|---|---|
| $V_{IHmax}$ | – Maximum HIGH level input voltage (the most positive $V_{IH}$). |
| $V_{IHT}$ | – HIGH level input threshold voltage. |
| $V_{ILT}$ | – LOW level input threshold voltage. |
| $V_{ILmin}$ | – Minimum LOW level input voltage (the most negative $V_{IL}$). |
| $V_{OHmax}$ | – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition. |
| $V_{OHmin}$ | – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition. |
| $V_{OHT}$ | – HIGH level output threshold voltage with the inputs set to their respective threshold levels. |
| $V_{OLT}$ | – LOW level output threshold voltage with the inputs set to their respective threshold levels. |
| $V_{OLmax}$ | – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions. |
| $V_{OLmin}$ | – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions. |
| $V_{BB}$ | – Reference bias voltage. The internally generated reference voltage which is used to set the input and output threshold level. |

**Figure 4. Transfer Characteristics**

## AC ELECTRICAL CHARACTERISTICS

**Ceramic DIP** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 2.00 | 6.90 | 2.10 | 6.80 | 2.10 | 7.40 | ns | Figs. 5, 6, 7 |
| $t_{PHL}$ | $A_n$, $B_n$, to $F_n$ | 2.00 | 6.90 | 2.10 | 6.80 | 2.10 | 7.40 | ns | |
| $t_{PLH}$ | Propagation delay | 1.40 | 4.70 | 1.40 | 4.40 | 1.40 | 4.70 | ns | |
| $t_{PHL}$ | $A_n$, $B_n$, to $\overline{P}$, $\overline{G}$ | 1.40 | 4.70 | 1.40 | 4.40 | 1.40 | 4.70 | ns | |
| $t_{PLH}$ | Propagation delay | 2.00 | 6.50 | 2.00 | 6.50 | 2.10 | 6.80 | ns | |
| $t_{PHL}$ | $A_n$, $B_n$, to $\overline{C}_{n+4}$ | 2.00 | 6.50 | 2.00 | 6.50 | 2.10 | 6.80 | ns | |
| $t_{PLH}$ | Propagation delay | 1.60 | 5.10 | 1.60 | 5.20 | 1.60 | 5.50 | ns | |
| $t_{PHL}$ | $\overline{C}_n$ to $F_n$ | 1.60 | 5.10 | 1.60 | 5.20 | 1.60 | 5.50 | ns | |
| $t_{PLH}$ | Propagation delay | 1.30 | 3.00 | 1.40 | 3.00 | 1.40 | 3.10 | ns | |
| $t_{PHL}$ | $\overline{C}_n$ to $\overline{C}_{n+4}$ | 1.30 | 3.00 | 1.40 | 3.00 | 1.40 | 3.10 | ns | |
| $t_{PLH}$ | Propagation delay | 1.40 | 8.80 | 1.50 | 8.60 | 1.50 | 9.00 | ns | |
| $t_{PHL}$ | $S_n$ to $F_n$ | 1.40 | 8.80 | 1.50 | 8.60 | 1.50 | 9.00 | ns | |
| $t_{PLH}$ | Propagation delay | 1.70 | 7.40 | 2.00 | 5.90 | 2.00 | 6.50 | ns | |
| $t_{PHL}$ | $S_n$ to $\overline{P}$, $\overline{G}$ | 1.70 | 7.40 | 2.00 | 5.90 | 2.00 | 6.50 | ns | |
| $t_{PLH}$ | Propagation delay | 2.70 | 10.1 | 2.80 | 8.50 | 2.90 | 8.70 | ns | |
| $t_{PHL}$ | $\overline{S}_n$ to $\overline{C}_{n+4}$ | 2.70 | 10.1 | 2.80 | 8.50 | 2.90 | 8.70 | ns | |
| $t_{PLH}$ | Propagation delay | 1.00 | 3.40 | 0.90 | 3.60 | 1.10 | 3.80 | ns | |
| $t_{PHL}$ | $\overline{E}$ to $F_n$ | 1.00 | 3.40 | 0.90 | 3.60 | 1.10 | 3.80 | ns | |
| $t_{TLH}$ | Transition time | 0.45 | 3.50 | 0.45 | 3.50 | 0.45 | 3.50 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 3.50 | 0.45 | 3.50 | 0.45 | 3.50 | ns | |
| $t_s$ | Setup time $A_n$, $B_n$ to $\overline{E}$ | 6.00 | | 6.00 | | 6.00 | | ns | Figs. 6, 8 |
| $t_h$ | Hold time $A_n$, $B_n$ to $\overline{E}$ | 0.10 | | 0.10 | | 0.10 | | ns | |
| $t_s$ | Setup time $S_n$ to $\overline{E}$ | 7.00 | | 7.00 | | 7.00 | | ns | |
| $t_h$ | Hold time $S_n$ to $\overline{E}$ | 0.60 | | 0.60 | | 0.60 | | ns | |
| $t_s$ | Setup time $\overline{C}_n$ to $\overline{E}$ | 4.00 | | 4.00 | | 4.00 | | ns | |
| $t_h$ | Hold time $\overline{C}_n$ to $\overline{E}$ | 0.60 | | 0.60 | | 0.60 | | ns | |
| $t_w(L)$ | Pulse width, LOW $\overline{E}$ | 2.50 | | 2.50 | | 2.50 | | ns | Figs. 5, 8 |

## AC ELECTRICAL CHARACTERISTICS

**Ceramic DIP** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V \pm 5\%$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 2.00 | 6.90 | 2.10 | 6.80 | 2.10 | 7.40 | ns | Figs. 5, 6, 7 |
| $t_{PHL}$ | $A_n$, $B_n$, to $F_n$ | 2.00 | 6.90 | 2.10 | 6.80 | 2.10 | 7.40 | ns | |
| $t_{PLH}$ | Propagation delay | 1.40 | 4.70 | 1.40 | 4.40 | 1.40 | 4.70 | ns | |
| $t_{PHL}$ | $A_n$, $B_n$, to $\overline{P}$, $\overline{G}$ | 1.40 | 4.70 | 1.40 | 4.40 | 1.40 | 4.70 | ns | |
| $t_{PLH}$ | Propagation delay | 2.00 | 6.50 | 2.00 | 6.50 | 2.10 | 6.80 | ns | |
| $t_{PHL}$ | $A_n$, $B_n$, to $\overline{C}_{n+4}$ | 2.00 | 6.50 | 2.00 | 6.50 | 2.10 | 6.80 | ns | |
| $t_{PLH}$ | Propagation delay | 1.60 | 5.10 | 1.60 | 5.20 | 1.60 | 5.50 | ns | |
| $t_{PHL}$ | $\overline{C}_n$ to $F_n$ | 1.60 | 5.10 | 1.60 | 5.20 | 1.60 | 5.50 | ns | |
| $t_{PLH}$ | Propagation delay | 1.30 | 3.00 | 1.40 | 3.00 | 1.40 | 3.10 | ns | |
| $t_{PHL}$ | $\overline{C}_n$ to $\overline{C}_{n+4}$ | 1.30 | 3.00 | 1.40 | 3.00 | 1.40 | 3.10 | ns | |
| $t_{PLH}$ | Propagation delay | 1.40 | 8.80 | 1.50 | 8.60 | 1.50 | 9.00 | ns | |
| $t_{PHL}$ | $S_n$ to $F_n$ | 1.40 | 8.80 | 1.50 | 8.60 | 1.50 | 9.00 | ns | |
| $t_{PLH}$ | Propagation delay | 1.70 | 7.40 | 2.00 | 5.90 | 2.00 | 6.50 | ns | |
| $t_{PHL}$ | $S_n$ to $\overline{P}$, $\overline{G}$ | 1.70 | 7.40 | 2.00 | 5.90 | 2.00 | 6.50 | ns | |
| $t_{PLH}$ | Propagation delay | 2.70 | 10.1 | 2.80 | 8.50 | 2.90 | 8.70 | ns | |
| $t_{PHL}$ | $\overline{S}_n$ to $\overline{C}_{n+4}$ | 2.70 | 10.1 | 2.80 | 8.50 | 2.90 | 8.70 | ns | |
| $t_{PLH}$ | Propagation delay | 1.00 | 3.40 | 0.90 | 3.60 | 1.10 | 3.80 | ns | |
| $t_{PHL}$ | $\overline{E}$ to $F_n$ | 1.00 | 3.40 | 0.90 | 3.60 | 1.10 | 3.80 | ns | |
| $t_{TLH}$ | Transition time | 0.45 | 3.50 | 0.45 | 3.50 | 0.45 | 3.50 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 3.50 | 0.45 | 3.50 | 0.45 | 3.50 | ns | |
| $t_s$ | Setup time $A_n$, $B_n$ to $\overline{E}$ | 6.00 | | 6.00 | | 6.00 | | ns | Figs. 6, 8 |
| $t_h$ | Hold time $A_n$, $B_n$ to $\overline{E}$ | 0.10 | | 0.10 | | 0.10 | | ns | |
| $t_s$ | Setup time $S_n$ to $\overline{E}$ | 7.00 | | 7.00 | | 7.00 | | ns | |
| $t_h$ | Hold time $S_n$ to $\overline{E}$ | 0.60 | | 0.60 | | 0.60 | | ns | |
| $t_s$ | Setup time $\overline{C}_n$ to $\overline{E}$ | 4.00 | | 4.00 | | 4.00 | | ns | |
| $t_h$ | Hold time $\overline{C}_n$ to $\overline{E}$ | 0.60 | | 0.60 | | 0.60 | | ns | |
| $t_w(L)$ | Pulse width, LOW $\overline{E}$ | 2.50 | | 2.50 | | 2.50 | | ns | Figs. 5, 8 |

## ALU

## 100181

### AC ELECTRICAL CHARACTERISTICS

**Flat Pack** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$

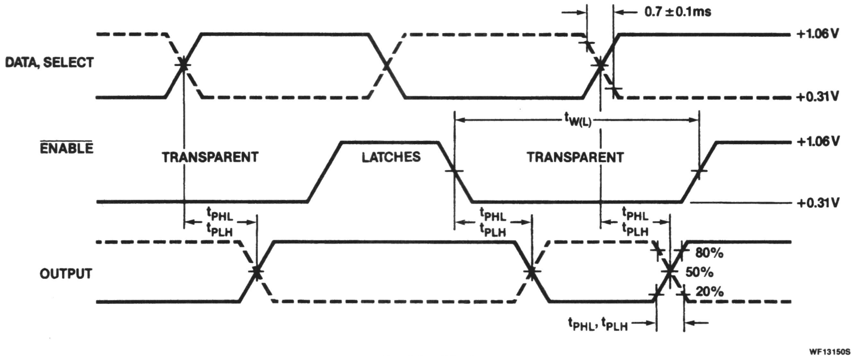
| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 2.00 | 6.70 | 2.10 | 6.60 | 2.10 | 7.20 | ns | Figs. 5, 6, 7 |
| $t_{PHL}$ | $A_n$, $B_n$, to $F_n$ | 2.00 | 6.70 | 2.10 | 6.60 | 2.10 | 7.20 | ns | |
| $t_{PLH}$ | Propagation delay | 1.40 | 4.50 | 1.40 | 4.20 | 1.40 | 4.50 | ns | |
| $t_{PHL}$ | $A_n$, $B_n$, to $\overline{P}$, $\overline{G}$ | 1.40 | 4.50 | 1.40 | 4.20 | 1.40 | 4.50 | ns | |
| $t_{PLH}$ | Propagation delay | 2.00 | 6.30 | 2.00 | 6.30 | 2.10 | 6.60 | ns | |
| $t_{PHL}$ | $A_n$, $B_n$, to $\overline{C}_{n+4}$ | 2.00 | 6.30 | 2.00 | 6.30 | 2.10 | 6.60 | ns | |
| $t_{PLH}$ | Propagation delay | 1.60 | 4.90 | 1.60 | 5.00 | 1.60 | 5.30 | ns | |
| $t_{PHL}$ | $\overline{C}_n$ to $F_n$ | 1.60 | 4.90 | 1.60 | 5.00 | 1.60 | 5.30 | ns | |
| $t_{PLH}$ | Propagation delay | 1.30 | 2.80 | 1.40 | 2.80 | 1.40 | 2.90 | ns | |
| $t_{PHL}$ | $\overline{C}_n$ to $\overline{C}_{n+4}$ | 1.30 | 2.80 | 1.40 | 2.80 | 1.40 | 2.90 | ns | |
| $t_{PLH}$ | Propagation delay | 1.40 | 8.60 | 1.50 | 8.40 | 1.50 | 8.80 | ns | |
| $t_{PHL}$ | $S_n$ to $F_n$ | 1.40 | 8.60 | 1.50 | 8.40 | 1.50 | 8.80 | ns | |
| $t_{PLH}$ | Propagation delay | 1.70 | 7.20 | 2.00 | 5.70 | 2.00 | 6.30 | ns | |
| $t_{PHL}$ | $S_n$ to $\overline{P}$, $\overline{G}$ | 1.70 | 7.20 | 2.00 | 5.70 | 2.00 | 6.30 | ns | |
| $t_{PLH}$ | Propagation delay | 2.70 | 9.90 | 2.80 | 8.30 | 2.90 | 8.50 | ns | |
| $t_{PHL}$ | $\overline{S}_n$ to $\overline{C}_{n+4}$ | 2.70 | 9.90 | 2.80 | 8.30 | 2.90 | 8.50 | ns | |
| $t_{PLH}$ | Propagation delay | 1.00 | 3.20 | 0.90 | 3.40 | 1.10 | 3.60 | ns | |
| $t_{PHL}$ | $\overline{E}$ to $F_n$ | 1.00 | 3.20 | 0.90 | 3.40 | 1.10 | 3.60 | ns | |
| $t_{TLH}$ | Transition time | 0.45 | 3.50 | 0.45 | 3.50 | 0.45 | 3.50 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 3.50 | 0.45 | 3.50 | 0.45 | 3.50 | ns | |
| $t_s$ | Setup time $A_n$, $B_n$ to $\overline{E}$ | 7.50 | | 7.50 | | 8.00 | | ns | Figs. 6, 8 |
| $t_h$ | Hold time $A_n$, $B_n$ to $\overline{E}$ | 0.00 | | 0.00 | | 0.00 | | ns | |
| $t_s$ | Setup time $S_n$ to $\overline{E}$ | 8.60 | | 8.40 | | 9.50 | | ns | |
| $t_h$ | Hold time $S_n$ to $\overline{E}$ | 0.50 | | 0.50 | | 0.50 | | ns | |
| $t_s$ | Setup time $\overline{C}_n$ to $\overline{E}$ | 4.70 | | 4.90 | | 5.20 | | ns | |
| $t_h$ | Hold time $\overline{C}_n$ to $\overline{E}$ | 0.50 | | 0.50 | | 0.50 | | ns | |
| $t_w(L)$ | Pulse width, LOW $\overline{E}$ | 2.50 | | 2.50 | | 2.50 | | ns | Figs. 5, 8 |

## AC ELECTRICAL CHARACTERISTICS

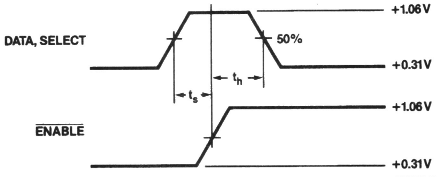
**Flat Pack** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V \pm 5\%$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$ | Propagation delay | 2.00 | 6.70 | 2.10 | 6.60 | 2.10 | 7.20 | ns | Figs. 5, 6, 7 |
| $t_{PHL}$ | $A_n$, $B_n$, to $F_n$ | 2.00 | 6.70 | 2.10 | 6.60 | 2.10 | 7.20 | ns | |
| $t_{PLH}$ | Propagation delay | 1.40 | 4.50 | 1.40 | 4.20 | 1.40 | 4.50 | ns | |
| $t_{PHL}$ | $A_n$, $B_n$, to $\overline{P}$, $\overline{G}$ | 1.40 | 4.50 | 1.40 | 4.20 | 1.40 | 4.50 | ns | |
| $t_{PLH}$ | Propagation delay | 2.00 | 6.30 | 2.00 | 6.30 | 2.10 | 6.60 | ns | |
| $t_{PHL}$ | $A_n$, $B_n$, to $\overline{C}_{n+4}$ | 2.00 | 6.30 | 2.00 | 6.30 | 2.10 | 6.60 | ns | |
| $t_{PLH}$ | Propagation delay | 1.60 | 4.90 | 1.60 | 5.00 | 1.60 | 5.30 | ns | |
| $t_{PHL}$ | $\overline{C}_n$ to $F_n$ | 1.60 | 4.90 | 1.60 | 5.00 | 1.60 | 5.30 | ns | |
| $t_{PLH}$ | Propagation delay | 1.30 | 2.80 | 1.40 | 2.80 | 1.40 | 2.90 | ns | |
| $t_{PHL}$ | $\overline{C}_n$ to $\overline{C}_{n+4}$ | 1.30 | 2.80 | 1.40 | 2.80 | 1.40 | 2.90 | ns | |
| $t_{PLH}$ | Propagation delay | 1.40 | 8.60 | 1.50 | 8.40 | 1.50 | 8.80 | ns | |
| $t_{PHL}$ | $S_n$ to $F_n$ | 1.40 | 8.60 | 1.50 | 8.40 | 1.50 | 8.80 | ns | |
| $t_{PLH}$ | Propagation delay | 1.70 | 7.20 | 2.00 | 5.70 | 2.00 | 6.30 | ns | |
| $t_{PHL}$ | $S_n$ to $\overline{P}$, $\overline{G}$ | 1.70 | 7.20 | 2.00 | 5.70 | 2.00 | 6.30 | ns | |
| $t_{PLH}$ | Propagation delay | 2.70 | 9.90 | 2.80 | 8.30 | 2.90 | 8.50 | ns | |
| $t_{PHL}$ | $\overline{S}_n$ to $\overline{C}_{n+4}$ | 2.70 | 9.90 | 2.80 | 8.30 | 2.90 | 8.50 | ns | |
| $t_{PLH}$ | Propagation delay | 1.00 | 3.20 | 0.90 | 3.40 | 1.10 | 3.60 | ns | |
| $t_{PHL}$ | $\overline{E}$ to $F_n$ | 1.00 | 3.20 | 0.90 | 3.40 | 1.10 | 3.60 | ns | |
| $t_{TLH}$ | Transition time | 0.45 | 3.50 | 0.45 | 3.50 | 0.45 | 3.50 | ns | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 3.50 | 0.45 | 3.50 | 0.45 | 3.50 | ns | |
| $t_s$ | Setup time $A_n$, $B_n$ to $\overline{E}$ | 7.50 | | 7.50 | | 8.00 | | ns | Figs. 6, 8 |
| $t_h$ | Hold time $A_n$, $B_n$ to $\overline{E}$ | 0.00 | | 0.00 | | 0.00 | | ns | |
| $t_s$ | Setup time $S_n$ to $\overline{E}$ | 8.60 | | 8.40 | | 9.50 | | ns | |
| $t_h$ | Hold time $S_n$ to $\overline{E}$ | 0.50 | | 0.50 | | 0.50 | | ns | |
| $t_s$ | Setup time $\overline{C}_n$ to $\overline{E}$ | 4.70 | | 4.90 | | 5.20 | | ns | |
| $t_h$ | Hold time $\overline{C}_n$ to $\overline{E}$ | 0.50 | | 0.50 | | 0.50 | | ns | |
| $t_w(L)$ | Pulse width, LOW $\overline{E}$ | 2.50 | | 2.50 | | 2.50 | | ns | Figs. 5, 8 |

## AC WAVEFORMS


0.7 ±0.1ms
+1.06V
DATA, SELECT
+0.31V
$t_{W(L)}$
ENABLE
TRANSPARENT
LATCHES
TRANSPARENT
+1.06V
+0.31V
$t_{PHL}$
$t_{PLH}$
$t_{PHL}$
$t_{PLH}$
$t_{PHL}$
$t_{PLH}$
OUTPUT
80%
50%
20%
$t_{PHL}$, $t_{PLH}$
WF13150S

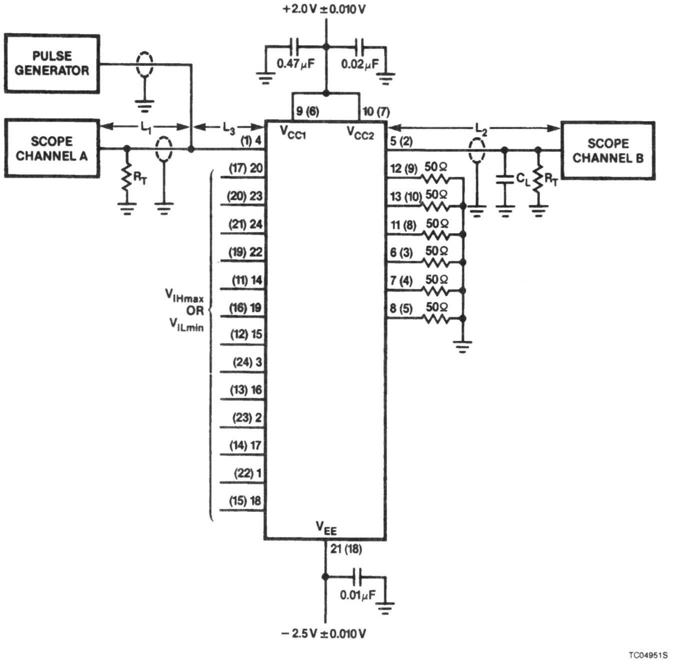
a. Enable Timing


DATA, SELECT
+1.06V
50%
+0.31V
$t_h$
$t_s$
ENABLE
+1.06V
+0.31V
WF13160S

b. Setup and Hold Times

Figure 5

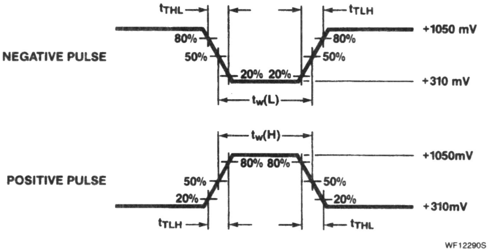
## TEST CIRCUITS AND WAVEFORMS


+2.0V ±0.010V
0.47μF
0.02μF
PULSE GENERATOR
SCOPE CHANNEL A
L1
L3
RT
9 (6)
10 (7)
VCC1
VCC2
(1) 4
(17) 20
(20) 23
(21) 24
(19) 22
(11) 14
(16) 19
(12) 15
(24) 3
(13) 16
(23) 2
(14) 17
(22) 1
(15) 18
VIHmax OR VILmin
5 (2)
12 (9) 50Ω
13 (10) 50Ω
11 (8) 50Ω
6 (3) 50Ω
7 (4) 50Ω
8 (5) 50Ω
L2
CL
RT
SCOPE CHANNEL B
VEE
21 (18)
0.01μF
−2.5V ±0.010V
TC04951S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1μF and 25μF from GND to $V_{CC}$, 0.01μF and 25μF from GND to $V_{EE}$. (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance $\leqslant$ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ±1% or better.
11. Pin connections are for Flat Pack and in parentheses for Ceramic DIP.

Figure 6. Test Circuit


NEGATIVE PULSE
tTHL
tTLH
80%
50%
20%
20%
80%
50%
+1050 mV
+310 mV
tw(L)
tw(H)
POSITIVE PULSE
80%
80%
50%
20%
50%
20%
+1050mV
+310mV
tTLH
tTHL
WF12290S

| INPUT PULSE REQUIREMENTS<br>$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -2.5V \pm 0.010V$, $V_T$ = GND (0V) | | | | | |
|---|---|---|---|---|---|
| **Family** | **Amplitude** | **Rep Rate** | **Pulse Width** | $t_{TLH}$ | $t_{THL}$ |
| 100K ECL | 740mVp-p | 1MHz | 500ns | 0.7 ±0.1ns | 0.7 ±0.1ns |

Figure 7. Input Pulse Definition

Signetics

# 100231
## Flip-Flop

**Triple D-Type Master-Slave Flip-Flop (High-speed version of 100131)**
***Product Specification***

**ECL Products**

## DESCRIPTION

100231 is a high-speed version of the 100131.

100231 has three D-type master-slave flip-flops, with true and complementary output, separate clock, set and reset. In addition, all three flip-flops have a common clock, set and reset.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|
| 100131 | 1.3ns | 110mA |

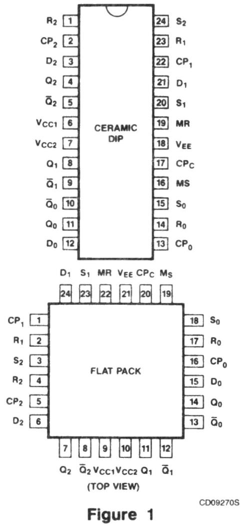
## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC1} = V_{CC2} = GND$; $V_{EE} = -4.2V$ to $-4.8V$ $T_A = 0°C$ to $+85°C$ |
|---|---|
| Ceramic DIP | 100131F |
| Ceramic Flat Pack | 100131Y |

## PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $D_0 - D_2$ | Data Inputs |
| $CP_c$ | Common Clock Input |
| $CP_0 - CP_2$ | Clock Inputs |
| MS | Master Set Input |
| $S_0 - S_2$ | Set Inputs |
| MR | Master Reset Input |
| $R_0 - R_2$ | Reset Inputs |
| $Q_0 - Q_2$, $\overline{Q}_0 - \overline{Q}_2$ | Data Outputs |

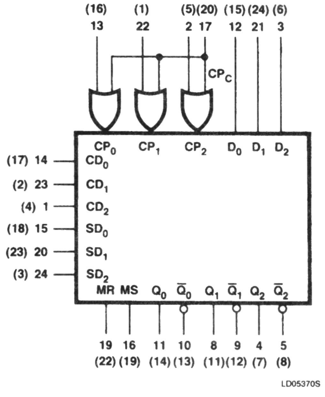
## PIN CONFIGURATION



R2 1
CP2 2
D2 3
Q2 4
Q̄2 5
VCC1 6
VCC2 7
Q1 8
Q̄1 9
Q̄0 10
Q0 11
D0 12
24 S2
23 R1
22 CP1
21 D1
20 S1
19 MR
18 VEE
17 CPC
16 MS
15 S0
14 R0
13 CP0
CERAMIC DIP
D1 S1 MR VEE CPC MS
24 23 22 21 20 19
CP1 1
R1 2
S2 3
R2 4
CP2 5
D2 6
18 S0
17 R0
16 CP0
15 D0
14 Q0
13 Q̄0
FLAT PACK
7 8 9 10 11 12
Q2 Q̄2 VCC1 VCC2 Q1 Q̄1
(TOP VIEW)
CD09270S

Figure 1

## LOGIC SYMBOL



(16) 13
(1) 22
(5)(20) 2 17
(15)(24)(6) 12 21 3
CPC
CP0 CP1 CP2 D0 D1 D2
(17) 14 CD0
(2) 23 CD1
(4) 1 CD2
(18) 15 SD0
(23) 20 SD1
(3) 24 SD2
MR MS Q0 Q̄0 Q1 Q̄1 Q2 Q̄2
19 16 11 10 8 9 4 5
(22) (19) (14) (13) (11) (12) (7) (8)
LD05370S

Figure 2

# Flip-Flop

# 100231

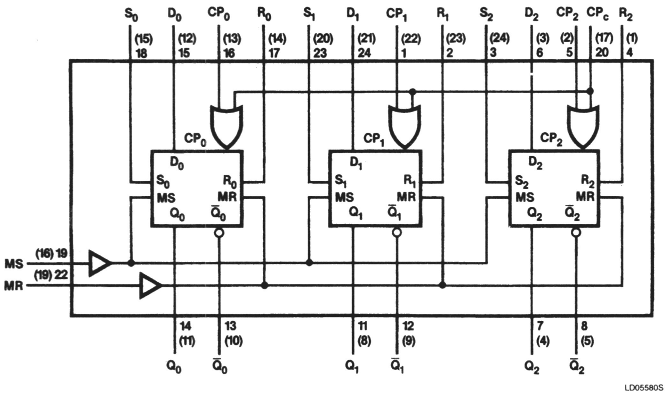

S0
D0
CP0
R0
S1
D1
CP1
R1
S2
D2
CP2
CPc
R2
(15) 18
(12) 15
(13) 16
(14) 17
(20) 23
(21) 24
(22) 1
(23) 2
(24) 3
(3) 6
(2) 5
(17) 20
(1) 4
CP0
D0
S0
R0
MS
MR
Q0
Q̄0
CP1
D1
S1
R1
MS
MR
Q1
Q̄1
CP2
D2
S2
R2
MS
MR
Q2
Q̄2
MS
(16) 19
MR
(19) 22
14 (11)
13 (10)
11 (8)
12 (9)
7 (4)
8 (5)
Q0
Q̄0
Q1
Q̄1
Q2
Q̄2
LD05580S

Figure 3. Logic Diagram

## FUNCTION TABLE

| INPUTS | | | | | | | OUTPUTS | |
|---|---|---|---|---|---|---|---|---|
| $D_n$ | $CP_C$ | $CP_n$ | MS | $S_n$ | MR | $R_n$ | $Q_{n+1}$ | $\overline{Q}_{n+1}$ |
| X | X | X | L | L | H | X | L | H |
| X | X | X | L | L | X | H | L | H |
| X | X | X | H | X | L | L | H | L |
| X | X | X | X | H | L | L | H | L |
| X | X | ↑ | L | L | L | L | $Q_n$ | $\overline{Q}_n$ |
| X | ↑ | H | L | L | L | L | $Q_n$ | $\overline{Q}_n$ |
| X | X | X | L | L | L | L | $Q_n$ | $\overline{Q}_n$ |
| H | ↑ | L | L | L | L | L | H | L |
| L | ↑ | L | L | L | L | L | L | H |
| H | L | ↑ | L | L | L | L | H | L |
| L | L | ↑ | L | L | L | L | L | H |

$D_n$: Data input; $CP_C$: Common Clock; $CP_n$: Clock; MS: Master Set; $S_n$: Set; MR: Master Reset; $R_n$: Reset; Q: Direct output; $\overline{Q}$: Complement output; n: State before transition; n + 1: State after transition;
↑ : LOW to HIGH transition.

Data enters a master, when both Clock and Common Clock are LOW, and transfers to the slave, when the clock or master clock (or both) go HIGH. If the set (or master set) is HIGH while the reset (or master reset) is HIGH, the output is undefined.

Positive Logic:
H = HIGH state (more positive voltage) = 1
L = LOW state (less positive voltage) = 0
↑ = LOW-to-HIGH transition
X = Don't Care

## Flip-Flop 100231

**ABSOLUTE MAXIMUM RATINGS** (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | 100K ECL | UNIT |
|---|---|---|---|
| $V_{EE}$ | Supply voltage ($V_{CC1} = V_{CC2} = GND$) | −7.0 to 0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | $V_{EE}$ to +0.5 | V |
| $I_O$ | Output source current | −55 | mA |
| $T_S$ | Storage temperature | −65 to +150 | °C |
| $T_J$ | Maximum junction temperature | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | | 100K ECL | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | −4.2 | −4.5 | −4.8 | V |
| $V_{EE}$ | Supply voltage (negative) when operating with 10K ECL family | | | | | −5.7 | V |
| $V_{IH}$ | HIGH level input voltage | $V_{CC1} = V_{CC2} = GND$<br>$T_A = 0°C$ to $+85°C$ | $V_{EE} = -4.2V$ | −1150 | | −880 | mV |
| | | | $V_{EE} = -4.5V$ | −1165 | | | |
| | | | $V_{EE} = -4.8V$ | | | | |
| $V_{IHT}$ | HIGH level input threshold voltage | | $V_{EE} = -4.2V$ | −1150 | | | mV |
| | | | $V_{EE} = -4.5V$ | −1165 | | | mV |
| | | | $V_{EE} = -4.8V$ | | | | |
| $V_{ILT}$ | LOW level input threshold voltage | | $V_{EE} = -4.2V$ | | | −1475 | mV |
| | | | $V_{EE} = -4.5V$ | | | | |
| | | | $V_{EE} = -4.8V$ | | | −1490 | mV |
| $V_{IL}$ | LOW level input voltage | | $V_{EE} = -4.2V$ | −1810 | | −1475 | mV |
| | | | $V_{EE} = -4.5V$ | | | | |
| | | | $V_{EE} = -4.8V$ | | | −1490 | |
| $T_A$ | Operating ambient temperature | | | 0 | +25 | +85 | °C |

**NOTE:**
When operating at other than specified voltages (−4.2V, −4.5V, −4.8V) DC & AC Characteristics will vary slightly from specified values.

**DC ELECTRICAL CHARACTERISTICS** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$, $T_A = 0°C$ to $+85°C$ unless otherwise specified[1, 3]

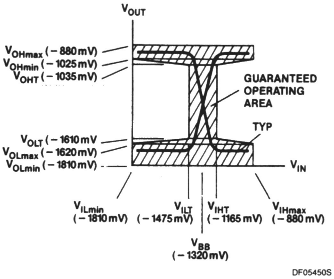
| PARAMETER | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] | |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | $V_{EE} = -4.2V$ | −1025 | | −870 | mV | $V_{IN} = V_{IHmax}$<br>or<br>$V_{IN} = V_{ILmin}$ | Loading with 50Ω to −2.0V ±0.010V |
| | | $V_{EE} = -4.5V$ | −1025 | −955 | −880 | mV | | |
| | | $V_{EE} = -4.8V$ | −1035 | | −880 | mV | | |
| $V_{OHT}$ | HIGH level output threshold voltage | $V_{EE} = -4.2V$ | −1035 | | | mV | $V_{IN} = V_{IHmin}$<br>or<br>$V_{IN} = V_{ILmax}$ | |
| | | $V_{EE} = -4.5V$ | −1035 | | | mV | | |
| | | $V_{EE} = -4.8V$ | −1045 | | | mV | | |
| $V_{OLT}$ | LOW level output threshold voltage | $V_{EE} = -4.2V$ | | | −1590 | mV | $V_{IN} = V_{IHmin}$<br>or<br>$V_{IN} = V_{ILmax}$ | |
| | | $V_{EE} = -4.5V$ | | | −1610 | mV | | |
| | | $V_{EE} = -4.8V$ | | | −1610 | mV | | |
| $V_{OL}$ | LOW level output voltage | $V_{EE} = -4.2V$ | −1810 | | −1600 | mV | $V_{IN} = V_{IHmax}$<br>or<br>$V_{IN} = V_{ILmin}$ | |
| | | $V_{EE} = -4.5V$ | −1810 | −1705 | −1620 | mV | | |
| | | $V_{EE} = -4.8V$ | −1830 | | −1620 | mV | | |
| $I_{IH}$ | HIGH level input current | $D_n$, $CP_n$ | | | 240 | μA | $V_{IN} = V_{IHMAX}$ | |
| | | $CP_C$, MS, MR, | | | 450 | μA | | |
| | | $R_n$, $S_n$ | | | 530 | μA | | |
| $I_{IL}$ | LOW level input current | | 0.5 | | | μA | $V_{IN} = V_{ILmin}$ | |
| $-I_{EE}$ | $V_{EE}$ supply current | | 74 | 110 | 149 | mA | Inputs open | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | $V_{EE} = -4.2V$<br>$T_A = +25°C$ | | | 0.035 | V/V | | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | | 0.070 | V/V | | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 4.

## Flip-Flop

## 100231



**NOTES:**

| | |
|---|---|
| $V_{IHmax}$ | – Maximum HIGH level input voltage (the most positive $V_{IH}$). |
| $V_{IHT}$ | – HIGH level input threshold voltage. |
| $V_{ILT}$ | – LOW level input threshold voltage. |
| $V_{ILmin}$ | – Minimum LOW level input voltage (the most negative $V_{IL}$). |
| $V_{OHmax}$ | – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition. |
| $V_{OHmin}$ | – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition. |
| $V_{OHT}$ | – HIGH level output threshold voltage with the inputs set to their respective threshold levels. |
| $V_{OLT}$ | – LOW level output threshold voltage with the inputs set to their respective threshold levels. |
| $V_{OLmax}$ | – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions. |
| $V_{OLmin}$ | – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions. |
| $V_{BB}$ | – Reference bias voltage. The internally generated reference voltage which is used to set the input and output threshold level. |

**Figure 4. Transfer Characteristics**

## AC ELECTRICAL CHARACTERISTICS

**Ceramic DIP** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | | |
| $f_{MAX}$ | Maximum clock frequency | 400 | | 400 | | 400 | | MHz | Figs. 5, 9, 10 | |
| $t_{PLH}$ | Propagation delay | 0.75 | 2.00 | 0.75 | 2.00 | 0.70 | 2.05 | ns | | |
| $t_{PHL}$ | $CP_C$ to $Q_n$ | 0.75 | 2.00 | 0.75 | 2.00 | 0.70 | 2.05 | ns | | |
| $t_{PLH}$ | Propagation delay | 0.70 | 1.80 | 0.70 | 1.80 | 0.70 | 1.80 | ns | Figs. 6, 8, 10 | |
| $t_{PHL}$ | $CP_n$ to $Q_n$ | 0.70 | 1.80 | 0.70 | 1.80 | 0.70 | 1.80 | ns | | |
| $t_{PLH}$ | Propagation delay | 1.05 | 2.50 | 1.05 | 2.50 | 1.05 | 2.50 | ns | $CP_n$ = LOW | Figs. 7, 8, 10 |
| $t_{PHL}$ | MS, MR to $Q_n$ | 1.05 | 2.50 | 1.05 | 2.50 | 1.05 | 2.50 | ns | | |
| $t_{PLH}$ | Propagation delay | 1.10 | 2.80 | 1.10 | 2.80 | 1.10 | 2.80 | ns | $CP_n$ = HIGH | |
| $t_{PHL}$ | MS, MR to $Q_n$ | 1.10 | 2.80 | 1.10 | 2.80 | 1.10 | 2.80 | ns | | |
| $t_{PLH}$ | Propagation delay | 0.65 | 1.70 | 0.70 | 1.70 | 0.70 | 1.90 | ns | $CP_n$ = LOW | |
| $t_{PHL}$ | $R_n$, $S_n$ to $Q_n$ | 0.65 | 1.70 | 0.70 | 1.70 | 0.70 | 1.90 | ns | | |
| $t_{PLH}$ | Propagation delay | 0.70 | 2.00 | 0.70 | 1.90 | 0.70 | 2.20 | ns | $CP_n$ = HIGH | |
| $t_{PHL}$ | $R_n$, $S_n$ to $Q_n$ | 0.70 | 2.00 | 0.70 | 1.90 | 0.70 | 2.20 | ns | | |
| $t_{TLH}$ | Transition time | 0.45 | 1.40 | 0.45 | 1.40 | 0.45 | 1.40 | ns | Figs. 6, 7, 10 | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.40 | 0.45 | 1.40 | 0.45 | 1.40 | ns | | |
| $t_s$ | Setup time $D_n$ to $CP_n$ | 0.90 | | 0.70 | | 0.90 | | ns | Figs. 7, 8, 10 | |
| $t_h$ | Hold time $CP_n$ to $D_n$ | 0.60 | | 0.60 | | 0.80 | | ns | | |
| $t_r$ | Release time $R_n$, $S_n$ to $CP_n$ | 1.50 | | 1.30 | | 1.50 | | ns | | |
| $t_r$ | Release time MR, MS to $CP_n$ | 2.50 | | 2.30 | | 2.50 | | ns | | |
| $t_w(H)$ | Pulse width HIGH<br>MR, MS, $R_n$, $S_n$, $CP_n$ | 2.50 | | 2.50 | | 2.50 | | ns | Figs. 6, 7 | |

## AC ELECTRICAL CHARACTERISTICS

**Ceramic DIP** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V \pm 5\%$

| PARAMETER | | $T_A$ = 0°C | | $T_A$ = +25°C | | $T_A$ = +85°C | | UNIT | TEST CONDITIONS | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | | |
| $f_{MAX}$ | Maximum clock frequency | 400 | | 400 | | 400 | | MHz | Figs. 5, 9, 10 | |
| $t_{PLH}$ | Propagation delay | 0.75 | 2.00 | 0.75 | 2.00 | 0.70 | 2.05 | ns | | |
| $t_{PHL}$ | $CP_C$ to $Q_n$ | 0.75 | 2.00 | 0.75 | 2.00 | 0.70 | 2.05 | ns | | |
| $t_{PLH}$ | Propagation delay | 0.70 | 1.80 | 0.70 | 1.80 | 0.70 | 1.80 | ns | Figs. 6, 8, 10 | |
| $t_{PHL}$ | $CP_n$ to $Q_n$ | 0.70 | 1.80 | 0.70 | 1.80 | 0.70 | 1.80 | ns | | |
| $t_{PLH}$ | Propagation delay | 1.05 | 2.50 | 1.05 | 2.50 | 1.05 | 2.50 | ns | $CP_n$ = LOW | Figs. 7, 8, 10 |
| $t_{PHL}$ | MS, MR to $Q_n$ | 1.05 | 2.50 | 1.05 | 2.50 | 1.05 | 2.50 | ns | | |
| $t_{PLH}$ | Propagation delay | 1.10 | 2.80 | 1.10 | 2.80 | 1.10 | 2.80 | ns | $CP_n$ = HIGH | |
| $t_{PHL}$ | MS, MR to $Q_n$ | 1.10 | 2.80 | 1.10 | 2.80 | 1.10 | 2.80 | ns | | |
| $t_{PLH}$ | Propagation delay | 0.65 | 1.70 | 0.70 | 1.70 | 0.70 | 1.90 | ns | $CP_n$ = LOW | |
| $t_{PHL}$ | $R_n$, $S_n$ to $Q_n$ | 0.65 | 1.70 | 0.70 | 1.70 | 0.70 | 1.90 | ns | | |
| $t_{PLH}$ | Propagation delay | 0.70 | 2.00 | 0.70 | 1.90 | 0.70 | 2.20 | ns | $CP_n$ = HIGH | |
| $t_{PHL}$ | $R_n$, $S_n$ to $Q_n$ | 0.70 | 2.00 | 0.70 | 1.90 | 0.70 | 2.20 | ns | | |
| $t_{TLH}$ | Transition time | 0.45 | 1.40 | 0.45 | 1.40 | 0.45 | 1.40 | ns | Figs. 6, 7, 10 | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.40 | 0.45 | 1.40 | 0.45 | 1.40 | ns | | |
| $t_s$ | Setup time $D_n$ to $CP_n$ | 0.90 | | 0.70 | | 0.90 | | ns | Figs. 7, 8, 10 | |
| $t_h$ | Hold time $CP_n$ to $D_n$ | 0.60 | | 0.60 | | 0.80 | | ns | | |
| $t_r$ | Release time $R_n$, $S_n$ to $CP_n$ | 1.50 | | 1.30 | | 1.50 | | ns | | |
| $t_r$ | Release time MR, MS to $CP_n$ | 2.50 | | 2.30 | | 2.50 | | ns | | |
| $t_w(H)$ | Pulse width HIGH<br>MR, MS, $R_n$, $S_n$, $CP_n$ | 2.50 | | 2.50 | | 2.50 | | ns | Figs. 6, 7 | |

## AC ELECTRICAL CHARACTERISTICS

**Flat Pack** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$

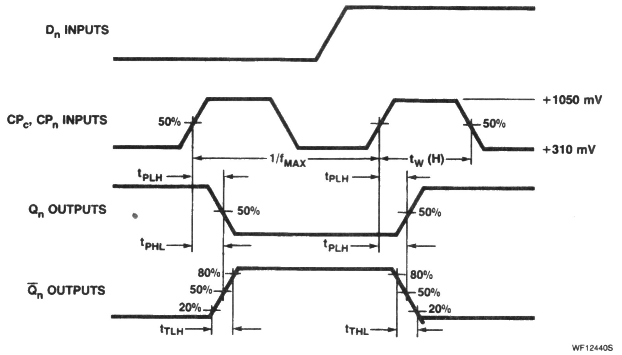
| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | | |
| $f_{MAX}$ | Maximum toggle frequency | 400 | | 400 | | 400 | | MHz | Figs. 5, 9, 10 | |
| $t_{PLH}$ | Propagation delay | 0.75 | 1.80 | 0.75 | 1.80 | 0.70 | 1.85 | ns | | |
| $t_{PHL}$ | $CP_C$ to $Q_n$ | 0.75 | 1.80 | 0.75 | 1.80 | 0.70 | 1.85 | ns | | |
| $t_{PLH}$ | Propagation delay | 0.70 | 1.60 | 0.70 | 1.60 | 0.70 | 1.70 | ns | Figs. 6, 8, 10 | |
| $t_{PHL}$ | $CP_n$ to $Q_n$ | 0.70 | 1.60 | 0.70 | 1.60 | 0.70 | 1.70 | ns | | |
| $t_{PLH}$ | Propagation delay | 1.05 | 2.30 | 1.05 | 2.30 | 1.05 | 2.40 | ns | $CP_n$ = LOW | Figs. 7, 8, 10 |
| $t_{PHL}$ | MS, MR to $Q_n$ | 1.05 | 2.30 | 1.05 | 2.30 | 1.05 | 2.40 | ns | | |
| $t_{PLH}$ | Propagation delay | 1.10 | 2.60 | 1.10 | 2.50 | 1.10 | 2.70 | ns | $CP_n$ = HIGH | |
| $t_{PHL}$ | MS, MR to $Q_n$ | 1.10 | 2.60 | 1.10 | 2.50 | 1.10 | 2.70 | ns | | |
| $t_{PLH}$ | Propagation delay | 0.65 | 1.50 | 0.70 | 1.50 | 0.70 | 1.70 | ns | $CP_n$ = LOW | |
| $t_{PHL}$ | $R_n$, $S_n$ to $Q_n$ | 0.65 | 1.50 | 0.70 | 1.50 | 0.70 | 1.70 | ns | | |
| $t_{PLH}$ | Propagation delay | 0.70 | 1.80 | 0.70 | 1.70 | 0.70 | 2.00 | ns | $CP_n$ = HIGH | |
| $t_{PHL}$ | $R_n$, $S_n$ to $Q_n$ | 0.70 | 1.80 | 0.70 | 1.70 | 0.70 | 2.00 | ns | | |
| $t_{TLH}$ | Transition time | 0.45 | 1.40 | 0.45 | 1.40 | 0.45 | 1.40 | ns | Figs. 6, 7, 10 | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.40 | 0.45 | 1.40 | 0.45 | 1.40 | ns | | |
| $t_s$ | Setup time $D_n$ to $CP_n$ | 0.80 | | 0.60 | | 0.80 | | ns | Figs. 7, 8, 10 | |
| $t_h$ | Hold time $CP_n$ to $D_n$ | 0.50 | | 0.50 | | 0.70 | | ns | | |
| $t_r$ | Release time $R_n$, $S_n$ to $CP_n$ | 1.40 | | 1.20 | | 1.40 | | ns | | |
| $t_r$ | Release time MR, MS to $CP_n$ | 2.40 | | 2.20 | | 2.40 | | ns | | |
| $t_w(H)$ | Pulse width HIGH<br>MR, MS, $R_n$, $S_n$, $CP_n$ | 2.50 | | 2.50 | | 2.50 | | ns | Figs. 6, 7 | |

## AC ELECTRICAL CHARACTERISTICS

**Flat Pack** $V_{CC1} = V_{CC2} = GND$, $V_{EE} = -5.2V$ ±5%

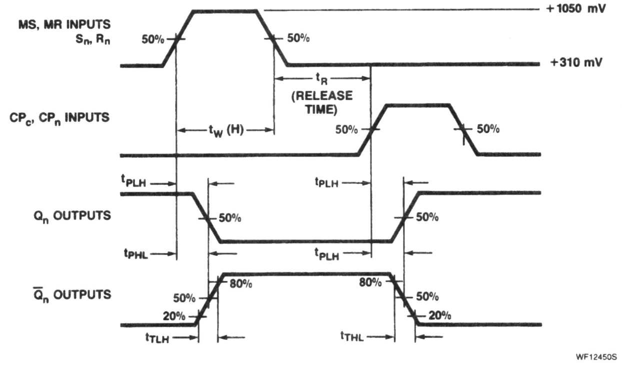
| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | | |
| $f_{MAX}$ | Maximum toggle frequency | 400 | | 400 | | 400 | | MHz | Figs. 5, 9, 10 | |
| $t_{PLH}$ | Propagation delay | 0.75 | 1.80 | 0.75 | 1.80 | 0.70 | 1.85 | ns | | |
| $t_{PHL}$ | $CP_C$ to $Q_n$ | 0.75 | 1.80 | 0.75 | 1.80 | 0.70 | 1.85 | ns | | |
| $t_{PLH}$ | Propagation delay | 0.70 | 1.60 | 0.70 | 1.60 | 0.70 | 1.70 | ns | Figs. 6, 8, 10 | |
| $t_{PHL}$ | $CP_n$ to $Q_n$ | 0.70 | 1.60 | 0.70 | 1.60 | 0.70 | 1.70 | ns | | |
| $t_{PLH}$ | Propagation delay | 1.05 | 2.30 | 1.05 | 2.30 | 1.05 | 2.40 | ns | $CP_n$ = LOW | Figs. 7, 8, 10 |
| $t_{PHL}$ | MS, MR to $Q_n$ | 1.05 | 2.30 | 1.05 | 2.30 | 1.05 | 2.40 | ns | | |
| $t_{PLH}$ | Propagation delay | 1.10 | 2.60 | 1.10 | 2.50 | 1.10 | 2.70 | ns | $CP_n$ = HIGH | |
| $t_{PHL}$ | MS, MR to $Q_n$ | 1.10 | 2.60 | 1.10 | 2.50 | 1.10 | 2.70 | ns | | |
| $t_{PLH}$ | Propagation delay | 0.65 | 1.50 | 0.70 | 1.50 | 0.70 | 1.70 | ns | $CP_n$ = LOW | |
| $t_{PHL}$ | $R_n$, $S_n$ to $Q_n$ | 0.65 | 1.50 | 0.70 | 1.50 | 0.70 | 1.70 | ns | | |
| $t_{PLH}$ | Propagation delay | 0.70 | 1.80 | 0.70 | 1.70 | 0.70 | 2.00 | ns | $CP_n$ = HIGH | |
| $t_{PHL}$ | $R_n$, $S_n$ to $Q_n$ | 0.70 | 1.80 | 0.70 | 1.70 | 0.70 | 2.00 | ns | | |
| $t_{TLH}$ | Transition time | 0.45 | 1.40 | 0.45 | 1.40 | 0.45 | 1.40 | ns | Figs. 6, 7, 10 | |
| $t_{THL}$ | 20% to 80%, 80% to 20% | 0.45 | 1.40 | 0.45 | 1.40 | 0.45 | 1.40 | ns | | |
| $t_s$ | Setup time $D_n$ to $CP_n$ | 0.80 | | 0.60 | | 0.80 | | ns | Figs. 7, 8, 10 | |
| $t_h$ | Hold time $CP_n$ to $D_n$ | 0.50 | | 0.50 | | 0.70 | | ns | | |
| $t_r$ | Release time $R_n$, $S_n$ to $CP_n$ | 1.40 | | 1.20 | | 1.40 | | ns | | |
| $t_r$ | Release time MR, MS to $CP_n$ | 2.40 | | 2.20 | | 2.40 | | ns | | |
| $t_w(H)$ | Pulse width HIGH<br>MR, MS, $R_n$, $S_n$, $CP_n$ | 2.50 | | 2.50 | | 2.50 | | ns | Figs. 6, 7 | |

## AC WAVEFORMS



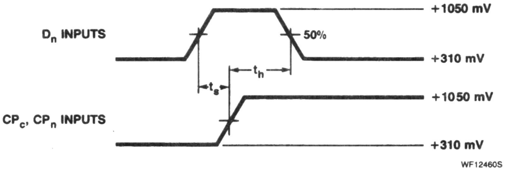
$D_n$ INPUTS
$CP_c$, $CP_n$ INPUTS
50%
+1050 mV
+310 mV
$1/f_{MAX}$
$t_W$ (H)
$t_{PLH}$
$Q_n$ OUTPUTS
$t_{PHL}$
$\overline{Q}_n$ OUTPUTS
80%
50%
20%
$t_{TLH}$
$t_{THL}$
WF12440S

Figure 5. Propagation Delay for Clock to Output and Transition Times



MS, MR INPUTS
$S_n$, $R_n$
50%
+1050 mV
+310 mV
$t_R$
(RELEASE TIME)
$CP_c$, $CP_n$ INPUTS
$t_W$ (H)
$t_{PLH}$
$Q_n$ OUTPUTS
$t_{PHL}$
$\overline{Q}_n$ OUTPUTS
80%
20%
$t_{TLH}$
$t_{THL}$
WF12450S

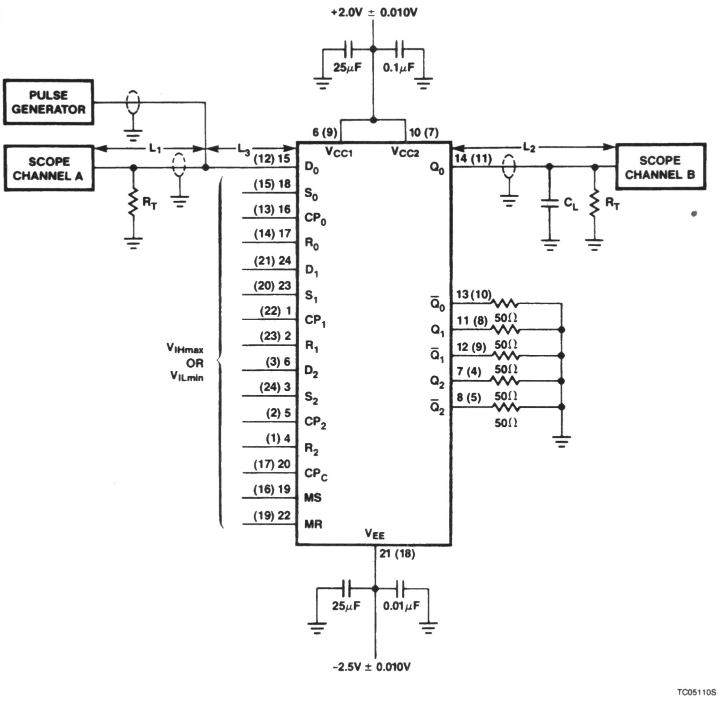
Figure 6. Propagation Delay for Sets and Resets to Outputs



$D_n$ INPUTS
50%
+1050 mV
+310 mV
$t_h$
$t_s$
$CP_c$, $CP_n$ INPUTS
WF12460S

Figure 7. Data Setup and Hold Times

## TEST CIRCUITS AND WAVEFORMS


+2.0V ± 0.010V
25µF
0.1µF
PULSE GENERATOR
SCOPE CHANNEL A
L1
L3
RT
6 (9)
10 (7)
VCC1
VCC2
(12) 15
D0
(15) 18
S0
(13) 16
CP0
(14) 17
R0
(21) 24
D1
(20) 23
S1
(22) 1
CP1
(23) 2
R1
(3) 6
D2
(24) 3
S2
(2) 5
CP2
(1) 4
R2
(17) 20
CPC
(16) 19
MS
(19) 22
MR
VIHmax OR VILmin
Q0
14 (11)
L2
SCOPE CHANNEL B
CL
RT
Q̄0
13 (10)
Q1
11 (8)
Q̄1
12 (9)
Q2
7 (4)
Q̄2
8 (5)
50Ω
50Ω
50Ω
50Ω
50Ω
VEE
21 (18)
25µF
0.01µF
-2.5V ± 0.010V
TC05110S

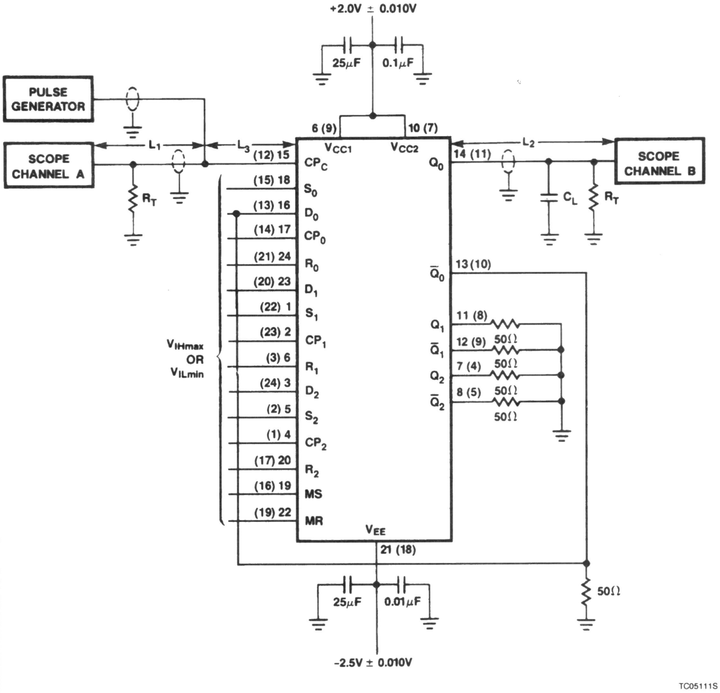
**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1µF and 25µF from GND to $V_{CC}$, 0.01µF and 25µF from GND to $V_{EE}$. (0.01 and 0.1µF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50 Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance ⩽ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50 Ω resistors should have tolerance of ± 1% or better.
11. Pin connections are for Flat Pack and in parentheses for Ceramic DIP.

Figure 8. Test Circuit

# Flip-Flop

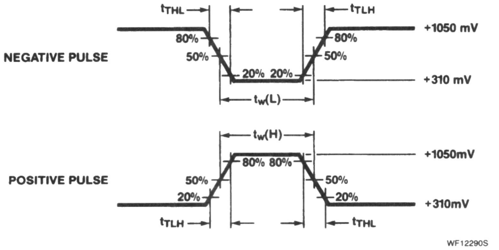
# 100231


+2.0V ± 0.010V
25μF
0.1μF
PULSE GENERATOR
SCOPE CHANNEL A
L1
L3
RT
6 (9)
10 (7)
VCC1
VCC2
(12) 15 CPC
(15) 18 S0
(13) 16 D0
(14) 17 CP0
(21) 24 R0
(20) 23 D1
(22) 1 S1
(23) 2 CP1
(3) 6 R1
(24) 3 D2
(2) 5 S2
(1) 4 CP2
(17) 20 R2
(16) 19 MS
(19) 22 MR
VIHmax OR VILmin
Q0 14 (11)
Q̄0 13 (10)
Q1 11 (8)
Q̄1 12 (9)
Q2 7 (4)
Q̄2 8 (5)
50Ω
L2
SCOPE CHANNEL B
CL
RT
VEE
21 (18)
25μF
0.01μF
-2.5V ± 0.010V
50Ω
TC05111S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1μF and 25μF from GND to $V_{CC}$, 0.01μF and 25μF from GND to $V_{EE}$. (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50 Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T = 50\Omega$ terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance $\leqslant 3pF$.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50 Ω resistors should have tolerance of ± 1% or better.
11. Pin connections are for Flat Pack and in parentheses for Ceramic DIP.

**Figure 9. Maximum Clock Frequency (Toggle Mode)**


NEGATIVE PULSE
tTHL
tTLH
80%
50%
20% 20%
80%
50%
tw(L)
+1050 mV
+310 mV
POSITIVE PULSE
tw(H)
80% 80%
50%
20%
50%
20%
tTLH
tTHL
+1050mV
+310mV
WF12290S

| INPUT PULSE REQUIREMENTS<br>$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -2.5V \pm 0.010V$, $V_T$ = GND (0V) | | | | | |
|---|---|---|---|---|---|
| **Family** | **Amplitude** | **Rep Rate** | **Pulse Width** | **$t_{TLH}$** | **$t_{THL}$** |
| 100K ECL | 740mVp-p | 1MHz | 500ns | 0.7 ±0.1ns | 0.7 ±0.1ns |

**Figure 10. Input Pulse Definition**

# Signetics

# 100255
## Translator

**Quint Bidirectional 100K-to-TTL Translator**
***Product Specification***

**ECL Products**

## DESCRIPTION

The 100255 is a Quint Bidirectional ECL 100K-to-TTL Translator. The ECL input/outputs ($\mathrm{I/OE_n}$) are compatible with the temperature- and voltage-compensated ECL 100K series. $\mathrm{I/OT_n}$ are TTL compatible input/outputs. A mode control input selects the translation and the $\overline{\mathrm{CE}}$ input enables the translation.

M and $\overline{\mathrm{CE}}$ are ECL inputs.

| TYPE | TYPICAL PROPAGATION DELAY | | TYPICAL SUPPLY CURRENT ($-I_{EE}$) |
|---|---|---|---|
| 100255 | TTL-to-ECL | 2.40ns | 105mA |
| | ECL-to-TTL | 4.50ns | |

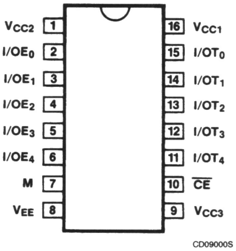
## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC1} = V_{CC2} = \mathrm{GND}$; $V_{CC3} = +5\mathrm{V}$<br>$V_{EE} = -4.2\mathrm{V}$ to $-4.8\mathrm{V}$, $T_A = 0°\mathrm{C}$ to $+85°\mathrm{C}$ |
|---|---|
| Ceramic DIP | 100255F |

## PIN DESCRIPTION

| PINS | DESCRIPTION |
|---|---|
| $\mathrm{I/OE_0 - I/OE_4}$ | ECL Data Inputs And Outputs |
| $\mathrm{I/OT_0 - I/OT_4}$ | TTL Data Inputs And Outputs |
| M | ECL/TTL Mode Select ECL Input |
| $\overline{\mathrm{CE}}$ | ECL/TTL Enable ECL Input |

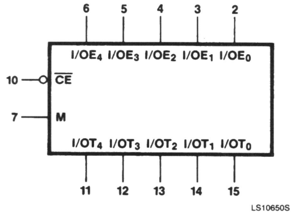
## PIN CONFIGURATION



$V_{CC2}$ 1
$\mathrm{I/OE_0}$ 2
$\mathrm{I/OE_1}$ 3
$\mathrm{I/OE_2}$ 4
$\mathrm{I/OE_3}$ 5
$\mathrm{I/OE_4}$ 6
M 7
$V_{EE}$ 8
16 $V_{CC1}$
15 $\mathrm{I/OT_0}$
14 $\mathrm{I/OT_1}$
13 $\mathrm{I/OT_2}$
12 $\mathrm{I/OT_3}$
11 $\mathrm{I/OT_4}$
10 $\overline{\mathrm{CE}}$
9 $V_{CC3}$
CD09000S

**Figure 1**

## LOGIC SYMBOL



6
5
4
3
2
$\mathrm{I/OE_4}$ $\mathrm{I/OE_3}$ $\mathrm{I/OE_2}$ $\mathrm{I/OE_1}$ $\mathrm{I/OE_0}$
10
$\overline{\mathrm{CE}}$
7
M
$\mathrm{I/OT_4}$ $\mathrm{I/OT_3}$ $\mathrm{I/OT_2}$ $\mathrm{I/OT_1}$ $\mathrm{I/OT_0}$
11
12
13
14
15
LS10650S

**Figure 2**

# Translator

# 100255

## LOGIC DIAGRAM

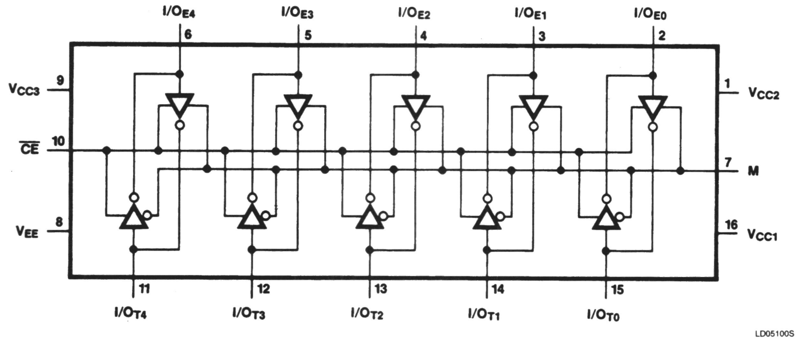

I/O$_{E4}$
6
I/O$_{E3}$
5
I/O$_{E2}$
4
I/O$_{E1}$
3
I/O$_{E0}$
2
V$_{CC3}$
9
$\overline{CE}$
10
V$_{EE}$
8
1
V$_{CC2}$
7
M
16
V$_{CC1}$
11
I/O$_{T4}$
12
I/O$_{T3}$
13
I/O$_{T2}$
14
I/O$_{T1}$
15
I/O$_{T0}$
LD05100S

Figure 3

## FUNCTION TABLE

| $\overline{CE}$ | M | ECL INPUT | TTL OUTPUT |
|---|---|---|---|
| L | X | L | Z* |
| H | H | H | L |
| H | H | L | H |
| **$\overline{CE}$** | **M** | **TTL INPUT** | **ECL OUTPUT** |
| H | L | H | L |
| H | L | L | H |

Positive Logic:
H = HIGH state (more positive voltage) = 1
L = LOW state (more negative voltage) = 0
X = Don't Care
* ECL output in off state; $V_O = V_T$
Z = High impedance TTL output.

## ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.)

| PARAMETER | | 100K ECL | UNIT |
|---|---|---|---|
| $V_{EE}$ | Supply voltage ($V_{CC1} = V_{CC2} =$ GND) | −7.0 to 0 | V |
| $V_{IN}$ | Input voltage ($V_{IN}$ should never be more negative than $V_{EE}$) | $V_{EE}$ to +0.5 | V |
| $I_O$ | Output source current | −55 | mA |
| $T_S$ | Storage temperature | −65 to +150 | °C |
| $T_J$ | Maximum junction temperature | +150 | °C |
| **PARAMETER** | | **TTL** | **UNIT** |
| $V_{CC}$ | Supply voltage | 7.0 | V |
| $V_{IN}$ | Input voltage | −0.5 to +5.5 | V |
| $I_{IN}$ | Input current | −30 to +5.0 | mA |
| $V_{OUT}$ | Voltage applied to output in HIGH output state | −0.5 to $+V_{CC}$ | V |
| $T_S$ | Storage temperature | −55 to +125 | °C |
| $T_J$ | Maximum junction temperature | +150 | °C |

## DC OPERATING CONDITIONS

| PARAMETER | | | | 100K ECL | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | Min | Nom | Max | |
| $V_{CC1}$, $V_{CC2}$ | Circuit ground | | | 0 | 0 | 0 | V |
| $V_{EE}$ | Supply voltage (negative) | | | −4.2 | −4.5 | −4.8 | V |
| $V_{EE}$ | Supply voltage (negative) when operating with 10K ECL family | | | | | −5.7 | V |
| $V_{IH}$ | HIGH level input voltage | $V_{CC1} = V_{CC2} =$ GND<br>$T_A = 0°C$ to $+85°C$ | $V_{EE} = -4.2V$ | −1150 | | −880 | mV |
| | | | $V_{EE} = -4.5V$ | −1165 | | | |
| | | | $V_{EE} = -4.8V$ | | | | |
| $V_{IHT}$ | HIGH level input threshold voltage | | $V_{EE} = -4.2V$ | −1150 | | | mV |
| | | | $V_{EE} = -4.5V$ | −1165 | | | mV |
| | | | $V_{EE} = -4.8V$ | | | | |
| $V_{ILT}$ | LOW level input threshold voltage | | $V_{EE} = -4.2V$ | | | −1475 | mV |
| | | | $V_{EE} = -4.5V$ | | | | |
| | | | $V_{EE} = -4.8V$ | | | −1490 | mV |
| $V_{IL}$ | LOW level input voltage | | $V_{EE} = -4.2V$ | −1810 | | −1475 | mV |
| | | | $V_{EE} = -4.5V$ | | | | |
| | | | $V_{EE} = -4.8V$ | | | −1490 | |
| $T_A$ | Operating ambient temperature | | | 0 | +25 | +85 | °C |

**NOTE:**

When operating at other than specified voltages (−4.2V, −4.5V, −4.8V) DC & AC Characteristics will vary slightly from specified values.

## Translator 100255

### DC OPERATING CONDITIONS FOR TTL

| PARAMETER | | TTL Min | TTL Nom | TTL Max | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 4.5 | 5.0 | 5.5 | V |
| $V_{IH}$ | HIGH level input voltage | 2.0 | | | V |
| $V_{IL}$ | LOW level input voltage | | | +0.8 | V |
| $I_{IK}$ | Input clamp current | | | −18 | mA |
| $I_{OH}$ | HIGH level output current | | | −1 | mA |
| $I_{OL}$ | LOW level output current | 2.0 | | 20 | mA |
| $T_A$ | Operating ambient temperature | 0 | | +85 | °C |

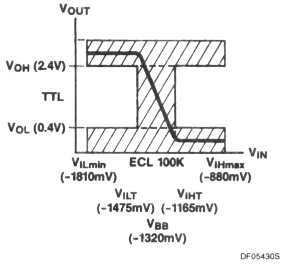
### DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2} = GND$, $V_{CC3} = +5V$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$, $T_A = 0°C$ to $+85°C$ unless otherwise specified[1, 3]

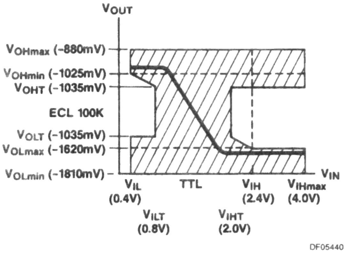
| PARAMETER | | | MIN | TYP | MAX | UNIT | TEST CONDITIONS[2] | |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage | $V_{EE} = -4.2V$ | −1025 | | −870 | mV | $V_{IN} = 0.4V$(TTL) | Loading with 25Ω to −2.0V ±0.010V |
| | | $V_{EE} = -4.5V$ | −1025 | −955 | −880 | mV | | |
| | | $V_{EE} = -4.8V$ | −1035 | | −880 | mV | | |
| $V_{OHT}$ | HIGH level output threshold voltage | $V_{EE} = -4.2V$ | −1035 | | | mV | $V_{IN} = 0.8V$(TTL) | |
| | | $V_{EE} = -4.5V$ | −1035 | | | mV | | |
| | | $V_{EE} = -4.8V$ | −1045 | | | mV | | |
| $V_{OLT}$ | LOW level output threshold voltage | $V_{EE} = -4.2V$ | | | −1590 | mV | $V_{IN} = 2.0V$(TTL) | |
| | | $V_{EE} = -4.5V$ | | | −1610 | mV | | |
| | | $V_{EE} = -4.8V$ | | | −1610 | mV | | |
| $V_{OL}$ | LOW level output voltage | $V_{EE} = -4.2V$ | −1810 | | −1600 | mV | $V_{IN} = 2.4V$(TTL) | |
| | | $V_{EE} = -4.5V$ | −1810 | −1705 | −1620 | mV | | |
| | | $V_{EE} = -4.8V$ | −1830 | | −1620 | mV | | |
| $I_{IH}$ | HIGH level input current | M, $\overline{CE}$ | | | 350 | µA | Apply −880mV + 5mV to each input one at a time | |
| | | • I/O | | | 350 | | | |
| $I_{IL}$ | ECL LOW input current | | 0.5 | | | µA | Apply −1810mV + 5mV to each input one at a time | |
| $-I_{EE}$ | Supply current | | 60 | 105 | 150 | mA | For all modes | |
| $\frac{\Delta V_{OH}}{\Delta V_{EE}}$ | HIGH level output voltage compensation | $V_{EE} = -4.2V$<br>$T_A = +25°C$ | | | 0.035 | V/V | | |
| $\frac{\Delta V_{OL}}{\Delta V_{EE}}$ | LOW level output voltage compensation | | | | 0.070 | V/V | | |

**NOTES:**

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to Section 3 Testing, DC Testing.
3. The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 4.


$V_{OUT}$
$V_{OH}$ (2.4V)
TTL
$V_{OL}$ (0.4V)
$V_{IN}$
$V_{ILmin}$ (-1810mV)
ECL 100K
$V_{IHmax}$ (-880mV)
$V_{ILT}$ (-1475mV)
$V_{IHT}$ (-1165mV)
$V_{BB}$ (-1320mV)
DF05430S

a. ECL-to-TTL


$V_{OUT}$
$V_{OHmax}$ (-880mV)
$V_{OHmin}$ (-1025mV)
$V_{OHT}$ (-1035mV)
ECL 100K
$V_{OLT}$ (-1035mV)
$V_{OLmax}$ (-1620mV)
$V_{OLmin}$ (-1810mV)
$V_{IN}$
$V_{IL}$ (0.4V)
TTL
$V_{IH}$ (2.4V)
$V_{IHmax}$ (4.0V)
$V_{ILT}$ (0.8V)
$V_{IHT}$ (2.0V)
DF05440S

b. TTL-to-ECL

**NOTES:**

| | |
|---|---|
| $V_{IHmax}$ | – Maximum HIGH level input voltage (the most positive $V_{IH}$). |
| $V_{IHT}$ | – HIGH level input threshold voltage. |
| $V_{ILT}$ | – LOW level input threshold voltage. |
| $V_{ILmin}$ | – Minimum LOW level input voltage (the most negative $V_{IL}$). |
| $V_{OHmax}$ | – Maximum HIGH level output voltage (the most positive $V_{OH}$) under the specified input and loading condition. |
| $V_{OHmin}$ | – Minimum HIGH level output voltage (the most negative $V_{OH}$) under the specified input and loading condition. |
| $V_{OHT}$ | – HIGH level output threshold voltage with the inputs set to their respective threshold levels. |
| $V_{OLT}$ | – LOW level output threshold voltage with the inputs set to their respective threshold levels. |
| $V_{OLmax}$ | – Maximum LOW level output voltage (the most positive $V_{OL}$) under the specified input and loading conditions. |
| $V_{OLmin}$ | – Minimum LOW level output voltage (the most negative $V_{OL}$) under the specified input and loading conditions. |
| $V_{BB}$ | – Reference bias voltage. The internally generated reference voltage which is used to set the input and output threshold level. |

Figure 4. Transfer Characteristics

## AC ELECTRICAL CHARACTERISTICS

**Ceramic DIP** $V_{CC1} = V_{CC2} = GND$, $V_{CC3} = +5V$, $V_{EE} = -4.2V \pm 0.010V$ to $-4.8V \pm 0.010V$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>ECL I/O-to-TTL I/O | | 7.00<br>7.00 | | 7.00<br>7.00 | | 7.00<br>7.00 | ns<br>ns | Figs. 5, 8, 9 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>TTL I/O-to-ECL I/O | | 8.00<br>8.00 | | 8.00<br>8.00 | | 8.00<br>8.00 | ns<br>ns | Figs. 6, 8, 9 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$\overline{CE}$ to ECL I/O | | 8.00<br>8.00 | | 8.00<br>8.00 | | 8.00<br>8.00 | ns<br>ns | Figs. 7, 8, 9 |
| $t_{TLH}$<br>$t_{THL}$ | Transition time ECL<br>20% to 80%, 80% to 20% | 0.75<br>0.75 | | 0.75<br>0.75 | | 0.75<br>0.75 | | ns<br>ns | Figs. 6, 9 |
| $t_{TLH}$<br>$t_{THL}$ | Transition time TTL<br>20% to 80%, 80% to 20% | 0.75<br>0.75 | | 1.00<br>1.00 | | 1.00<br>1.00 | | ns<br>ns | Figs. 6, 9 |

## AC ELECTRICAL CHARACTERISTICS

**Ceramic DIP** $V_{CC1} = V_{CC2} = \text{GND}$, $V_{EE} = -5.2V \pm 5\%$

| PARAMETER | | $T_A = 0°C$ | | $T_A = +25°C$ | | $T_A = +85°C$ | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>ECL I/O-to-TTL I/O | | 7.00<br>7.00 | | 7.00<br>7.00 | | 7.00<br>7.00 | ns<br>ns | Figs. 5, 8, 9 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>TTL I/O-to-ECL I/O | | 8.00<br>8.00 | | 8.00<br>8.00 | | 8.00<br>8.00 | ns<br>ns | Figs. 6, 8, 9 |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$\overline{CE}$ to ECL I/O | | 8.00<br>8.00 | | 8.00<br>8.00 | | 8.00<br>8.00 | ns<br>ns | Figs. 7, 8, 9 |
| $t_{TLH}$<br>$t_{THL}$ | Transition time ECL<br>20% to 80%, 80% to 20% | 0.75<br>0.75 | | 0.75<br>0.75 | | 0.75<br>0.75 | | ns<br>ns | Figs. 6, 9 |
| $t_{TLH}$<br>$t_{THL}$ | Transition time TTL<br>20% to 80%, 80% to 20% | 0.75<br>0.75 | | 1.00<br>1.00 | | 1.00<br>1.00 | | ns<br>ns | Figs. 6, 9 |

## AC WAVEFORMS

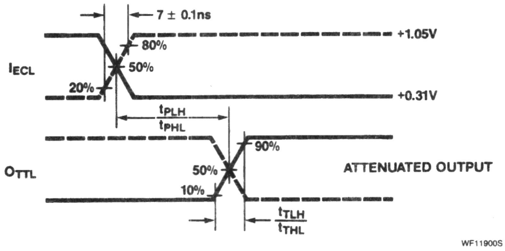

7 ± 0.1ns
+1.05V
80%
50%
I_ECL
20%
+0.31V
tPLH
tPHL
90%
O_TTL
50%
10%
ATTENUATED OUTPUT
tTLH
tTHL
WF11900S

Figure 5. Waveforms Interface ECL to TTL

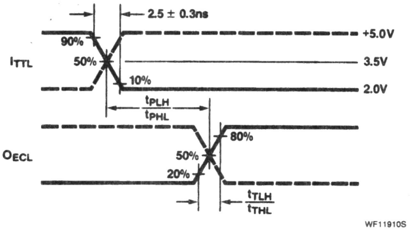

2.5 ± 0.3ns
+5.0V
90%
I_TTL
50%
3.5V
10%
2.0V
tPLH
tPHL
80%
O_ECL
50%
20%
tTLH
tTHL
WF11910S

Figure 6. Waveforms Interface TTL to ECL

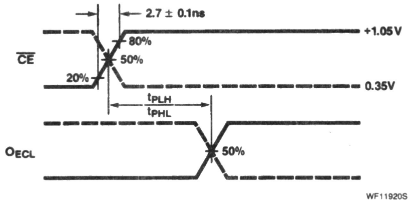
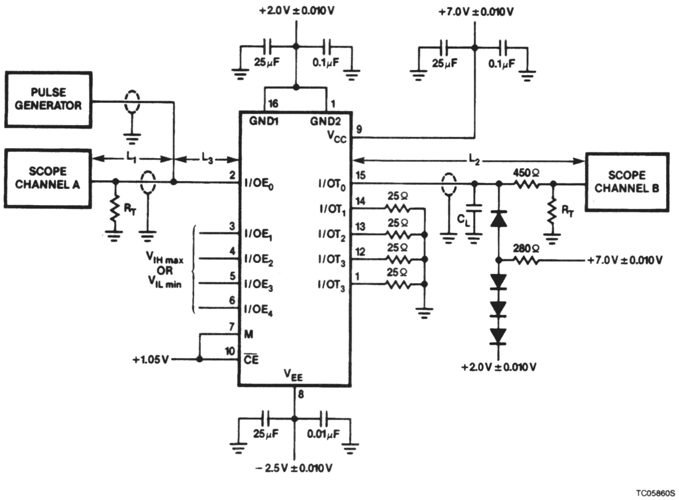

2.7 ± 0.1ns
+1.05V
80%
CE
50%
20%
0.35V
tPLH
tPHL
O_ECL
50%
WF11920S

Figure 7. Waveforms $\overline{CE}$ to ECL Outputs

## TEST CIRCUITS AND WAVEFORMS

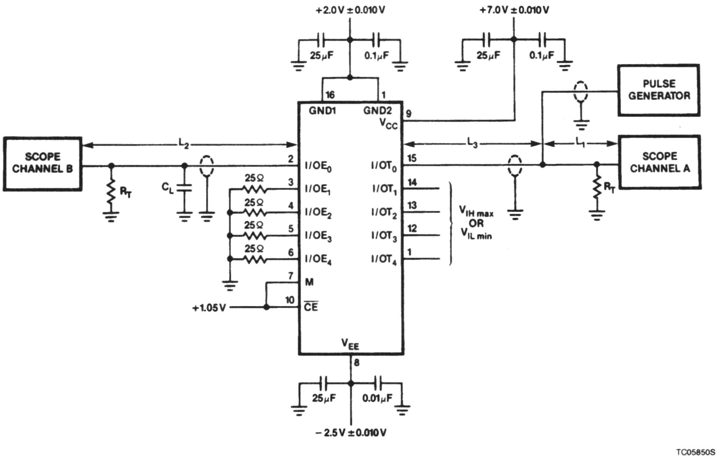

+2.0V ±0.010V
+7.0V ±0.010V
25µF
0.1µF
PULSE GENERATOR
SCOPE CHANNEL A
$R_T$
$L_1$
$L_3$
$L_2$
16
1
GND1
GND2
9
$V_{CC}$
2
$I/OE_0$
3
$I/OE_1$
4
$I/OE_2$
5
$I/OE_3$
6
$I/OE_4$
7
M
10
$\overline{CE}$
$V_{EE}$
8
15
$I/OT_0$
14
$I/OT_1$
13
$I/OT_2$
12
$I/OT_3$
1
$I/OT_3$
25Ω
$V_{IH\,max}$ OR $V_{IL\,min}$
+1.05V
$C_L$
450Ω
280Ω
SCOPE CHANNEL B
+7.0V ±0.010V
+2.0V ±0.010V
0.01µF
−2.5V ±0.010V
TC05860S

a. ECL → TTL

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1µF and 25µF from GND to $V_{CC}$, 0.01µF and 25µF from GND to $V_{EE}$. (0.01 and 0.1µF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance ≤ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.
11. Pin connections are for Flat Pack and in parentheses for Ceramic DIP.

Figure 8. Test Circuit


+2.0V ±0.010V
+7.0V ±0.010V
25µF
0.1µF
PULSE GENERATOR
SCOPE CHANNEL A
SCOPE CHANNEL B
$R_T$
$C_L$
$L_1$
$L_2$
$L_3$
16
1
GND1
GND2
9
$V_{CC}$
2
$I/OE_0$
3
$I/OE_1$
4
$I/OE_2$
5
$I/OE_3$
6
$I/OE_4$
7
M
10
$\overline{CE}$
25Ω
+1.05V
15
$I/OT_0$
14
$I/OT_1$
13
$I/OT_2$
12
$I/OT_3$
1
$I/OT_4$
$V_{IH\,max}$ OR $V_{IL\,min}$
$V_{EE}$
8
0.01µF
−2.5V ±0.010V
TC05850S

b. ECL → ECL

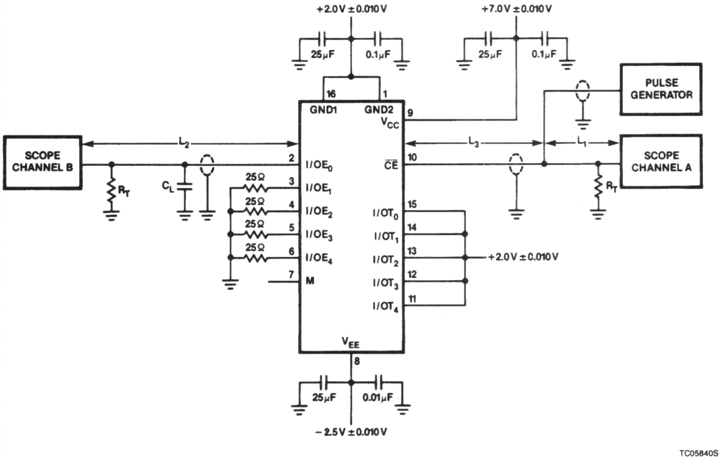
**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1µF and 25µF from GND to $V_{CC}$, 0.01µF and 25µF from GND to $V_{EE}$. (0.01 and 0.1µF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T$ = 50Ω terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance ≤ 3pF.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.
11. Pin connections are for Flat Pack and in parentheses for Ceramic DIP.

Figure 8. Test Circuit (Continued)

# Translator

# 100255

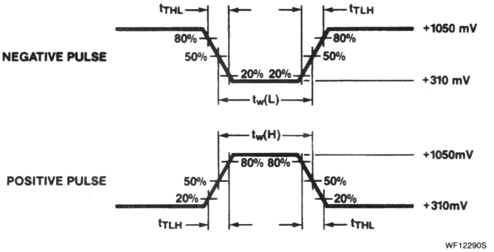

+2.0V ±0.010V
+7.0V ±0.010V
25µF
0.1µF
16
1
GND1
GND2
$V_{CC}$
9
PULSE GENERATOR
SCOPE CHANNEL B
SCOPE CHANNEL A
$L_2$
$L_3$
$L_1$
$R_T$
$C_L$
25Ω
2
3
4
5
6
7
I/OE₀
I/OE₁
I/OE₂
I/OE₃
I/OE₄
M
$\overline{CE}$
10
15
14
13
12
11
I/OT₀
I/OT₁
I/OT₂
I/OT₃
I/OT₄
+2.0V ±0.010V
$V_{EE}$
8
0.01µF
−2.5V ±0.010V
TC05840S

**NOTES:**

1. $V_{CC1} = V_{CC2} = +2V \pm 0.010V$, $V_{EE} = -3.2V \pm 0.010V$.
2. Decoupling 0.1µF and 25µF from GND to $V_{CC}$, 0.01µF and 25µF from GND to $V_{EE}$. (0.01 and 0.1µF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either HIGH or LOW state consistent with the LOGIC function required.
4. All unused outputs are loaded with 50Ω to GND.
5. $L_1$ and $L_2$ are equal length 50Ω impedance lines. $L_3$, the distance from the DUT pin to the junction of the cable from the Pulse Generator and the cable to the Scope, should not exceed 1/4 inch (6mm).
6. $R_T = 50\Omega$ terminator internal to Scope.
7. The unmatched wire stub between coaxial cable and pins under test must be less than 1/4 inch (6mm) long for proper test.
8. $C_L$ = Fixture and stray capacitance $\leqslant 3pF$.
9. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section on AC setup procedure).
10. All 50Ω resistors should have tolerance of ± 1% or better.
11. Pin connections are for Flat Pack and in parentheses for Ceramic DIP.

**c. TTL → ECL**

Figure 8. Test Circuit (Continued)


NEGATIVE PULSE
POSITIVE PULSE
$t_{THL}$
$t_{TLH}$
80%
50%
20%
$t_w(L)$
$t_w(H)$
+1050 mV
+310 mV
WF12290S

| INPUT PULSE REQUIREMENTS<br>$V_{CC1} = V_{CC2} = +2.0V \pm 0.010V$, $V_{EE} = -2.5V \pm 0.010V$, $V_T$ = GND (0V) | | | | | |
|---|---|---|---|---|---|
| **Family** | **Amplitude** | **Rep Rate** | **Pulse Width** | $t_{TLH}$ | $t_{THL}$ |
| 100K ECL | 740mVp-p | 1MHz | 500ns | 0.7 ±0.1ns | 0.7 ±0.1ns |

Figure 9. Input Pulse Definition

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# Section 8
# ECL RAM Data Sheets

Bipolar Memory Products

## INDEX

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**100422C** 1K-Bit ECL Bipolar RAM (256 × 4) ............................. 8-20
**100470A** 4K-Bit ECL Bipolar RAM (4096 × 1) ............................ 8-23
**100474A** 4K-Bit ECL Bipolar RAM (1024 × 4) ............................ 8-26

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# ECL RAM
# Overview

**Bipolar Memory Products**

All ECL RAMs described in this section are desiged with our advanced oxide-isolated process. This process provides the performance characteristics neccessary for today's ECL RAMs. Current designs manufactured with this process have demonstrated excellent results when subjected to alpha particle tests, with the latest test resulting in over 4 million device hours with zero soft failures.

Each of the configurations, (256 × 4, 4K × 1 and 1K × 4) are compatible with 10K and 100K logic levels through the application of a mask option.

Performance of these devices allows applications such as high-speed buffers, scratch pad, cache memory and other ECL high-speed data processing.

# 10422B
## 1K-Bit ECL Bipolar RAM

*Preliminary Specification*

**Bipolar Memory Products**

## DESCRIPTION

The 10422B device is a 256-word by 4-bit, fully encoded ECL Read/Write Random Access Memory designed for high-speed scratchpad, control, and buffer storage applications. The 10422B is available in a slimline 24-pin dual-in-line, flat or leadless package. This circuit may be reconfigured as 512 × 2 or 1024 × 1 organization by utilizing the block select feature. Each block has its own LOW active block select to enable the output. Write enable LOW active enables the write function in selected blocks. The memory has eight Address inputs, four Data inputs, four Block Select inputs, one Write Enable input and four Data outputs. The Open Emitter outputs have a 50Ω drive capability. The input pull-down resistor to $V_{CC}$ is 50,000Ω typical for the block selects.

Ordering information can be found on the following page.

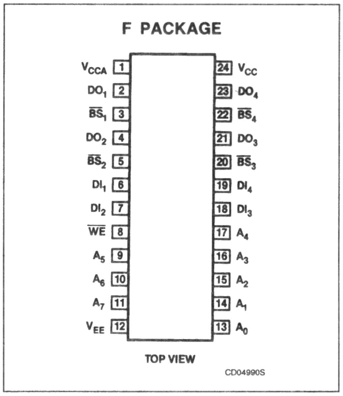
## FEATURES

- **256 words × 4 bits organization**
- **Fully compatible with 10K series ECL families**
- **Address access time:**
  - **10422B, 10ns max.**
- **Low power dissipation of 0.8mW/bit**
- **Operating temperature: 0°C to +75°C (ambient)**
- **Block select allows variable organization**

## APPLICATIONS

- **High-speed scratchpad**
- **Control and buffer storage**

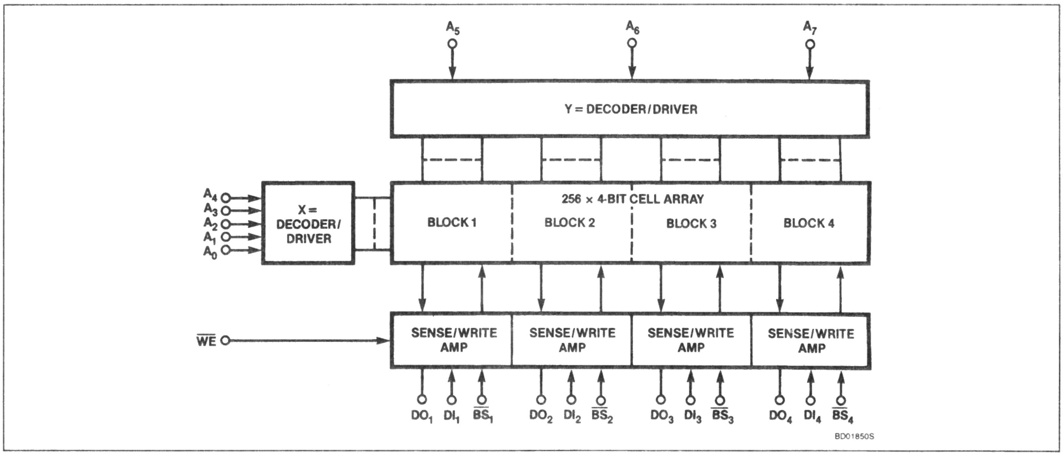
## PIN CONFIGURATION


F PACKAGE
$V_{CCA}$ 1
$DO_1$ 2
$\overline{BS}_1$ 3
$DO_2$ 4
$\overline{BS}_2$ 5
$DI_1$ 6
$DI_2$ 7
$\overline{WE}$ 8
$A_5$ 9
$A_6$ 10
$A_7$ 11
$V_{EE}$ 12
24 $V_{CC}$
23 $DO_4$
22 $\overline{BS}_4$
21 $DO_3$
20 $\overline{BS}_3$
19 $DI_4$
18 $DI_3$
17 $A_4$
16 $A_3$
15 $A_2$
14 $A_1$
13 $A_0$
TOP VIEW
CD04990S

## ABSOLUTE MAXIMUM RATINGS

| | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $V_{EE}$ | Supply voltage | +0.5 to −7 | $V_{DC}$ |
| $V_{IN}$ | Input voltage | 0 to $V_{EE}$ | |
| $I_O$ | Output current | −30 | mA |
| $T_A$ | Operating ambient temperature | 0 to +75 | °C |
| $T_J$ | Operating junction temperature | +125 | |
| $T_{STG}$ | Storage temperature | −55 to +150 | |

## BLOCK DIAGRAM


$A_5$
$A_6$
$A_7$
Y = DECODER/DRIVER
$A_4$
$A_3$
$A_2$
$A_1$
$A_0$
X = DECODER/ DRIVER
256 × 4-BIT CELL ARRAY
BLOCK 1
BLOCK 2
BLOCK 3
BLOCK 4
$\overline{WE}$
SENSE/WRITE AMP
SENSE/WRITE AMP
SENSE/WRITE AMP
SENSE/WRITE AMP
$DO_1$ $DI_1$ $\overline{BS}_1$
$DO_2$ $DI_2$ $\overline{BS}_2$
$DO_3$ $DI_3$ $\overline{BS}_3$
$DO_4$ $DI_4$ $\overline{BS}_4$
BD01850S

# 1K-Bit ECL Bipolar RAM (256 × 4) 10422B

## ORDERING CODE

| DESCRIPTION | ORDER CODE |
|---|---|
| Ceramic Dual-In-line<br>400mil wide 24-pin | 10422B F |

## DC ELECTRICAL CHARACTERISTICS $V_{EE} = -5.2V \pm 5\%$, $R_L = 50\Omega$ to $-2V$

| PARAMETER | | TEST CONDITIONS | 0°C | | +25°C | | +75°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | |
| **Input voltage** | | | | | | | | | |
| $V_{IH}$ | High | | −1.145 | −0.840 | −1.105 | −0.810 | −1.045 | −0.720 | V |
| $V_{IL}$ | Low | | −1.870 | −1.490 | −1.850 | −1.475 | −1.830 | −1.450 | |
| **Output voltage** | | | | | | | | | |
| $V_{OH}$ | High | $V_{IH}$ = Max | −1.0 | −0.840 | −0.960 | −0.810 | −0.900 | −0.720 | |
| $V_{OL}$ | Low | $V_{IL}$ = Min | −1.870 | −1.665 | −1.850 | −1.650 | −1.830 | −1.625 | V |
| $V_{OHT}$ | Threshold HIGH | $V_{IH}$ = Min | −1.020 | | −0.980 | | −0.920 | | |
| $V_{OLT}$ | Threshold LOW | $V_{IL}$ = Max | | −1.645 | | −1.630 | | −1.605 | |
| **Input current** | | | | | | | | | |
| $I_{IH}$ | High | $V_{IH}$ = Max | | 220 | | 220 | | 220 | µA |
| $I_{IL}$ | Low | $V_{IL}$ = Min | −50 | | −50 | | −50 | | |
| $I_{IL}$ | $\overline{BS}$ | $V_{IL}$ = Min | 0.5 | | 0.5 | | 0.5 | | |
| $I_{EE}$ | Supply current | $V_{IL}$ = Min | | 200 | | 200 | | 200 | mA |

**NOTES:**

1. Voltages are defined with respect to ground, pins 1 and 24.
2. Unit is in a test socket or mounted in a printed circuit board with transverse air flow > 400ft/min.
3. DC limits apply after thermal equilibrium has been established.
4. For current measurement, maximum is defined as the maximum absolute value.

## AC ELECTRICAL CHARACTERISTICS $V_{CC} = 0V$, $V_{EE} = -5.2V \pm 5\%$, $R_L = 50\Omega$ to $-2V$, $T_A = 0°C$ to $+75°C$

| PARAMETER | | LIMITS | | | UNIT |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $t_{AA}$ | Address access time | | | 10 | ns |
| $t_{RBS}$ | Block select recovery time | | | 5 | |
| $t_{ABS}$ | Block select access time | | | 5 | |
| $t_{WD}$ | Write disable time | | | 5 | |
| $t_{WPW}$ | Write pulse width | 7 | | | |
| $t_{WR}$ | Write recovery time | | 4.5 | 9 | |
| $t_{WHA}$ | Address hold time | 2 | 1 | | |
| $t_{WHBS}$ | Block select hold time | 2 | 1 | | |
| $t_{WHD}$ | Data hold time | 2 | 1 | | |
| $t_{WSA}$ | Address setup time | 3 | 1 | | |
| $t_{WSBS}$ | Block select setup time | 2 | 1 | | |
| $t_{WSD}$ | Data setup time | 2 | 1 | | |
| $t_f$ | Output fall time | | 2 | | |
| $t_r$ | Output rise time | | 2 | | |
| **Capacitance** | | | | | |
| $C_{IN}$ | Input | | | 8 | pF |
| $C_{OUT}$ | Output | | | 8 | |

**NOTES:**

1. AC limits apply after thermal equilibrium has been established.
2. Unit is in a test socket or mounted on a printed circuit board with transverse air flow > 400ft/min.
3. Output fall and rise times are measured between 20% and 80% points.
4. All propagation measurements to output are measured from 50% of the input pulse to 50% output level.

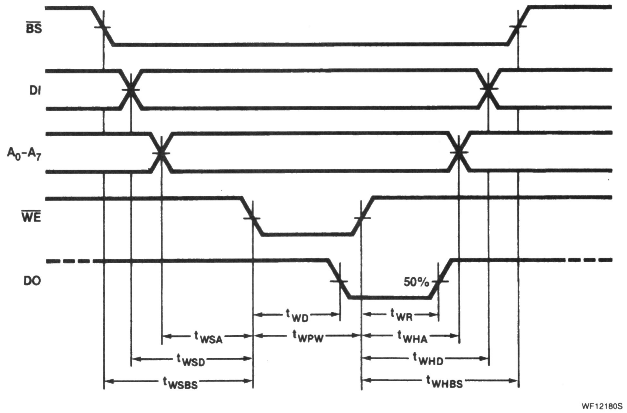
## 1K-Bit ECL Bipolar RAM (256 × 4) · 10422B

### TRUTH TABLE

| MODE | INPUTS | | | OUTPUTS |
|---|---|---|---|---|
| | $\overline{BS}_N$ | $\overline{WE}$ | $DI_N$ | |
| Disable | H | X | X | L |
| Write 0 | L | L | L | L |
| Write 1 | L | L | H | L |
| Read | L | H | X | $D_{OUT}$ |

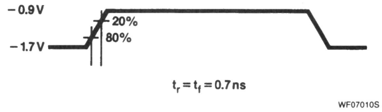
**NOTES:**
H = HIGH voltage level
L = LOW voltage level
X = Don't Care
N = Blocks 1 – 4

### TIMING DIAGRAMS



$\overline{BS}$
DI
$A_0$-$A_7$
$\overline{WE}$
DO
50%
$t_{WD}$
$t_{WR}$
$t_{WSA}$
$t_{WPW}$
$t_{WHA}$
$t_{WSD}$
$t_{WHD}$
$t_{WSBS}$
$t_{WHBS}$
WF12180S

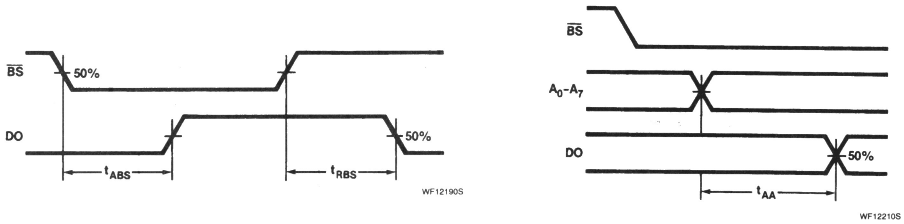
**Write Mode**



– 0.9 V
– 1.7 V
20%
80%
$t_r = t_f = 0.7$ ns
WF07010S

**NOTE:**
All timing measurements referenced to 50% of input levels.

**Input Levels**



$\overline{BS}$
50%
DO
50%
$t_{ABS}$
$t_{RBS}$
WF12190S
$\overline{BS}$
$A_0$-$A_7$
DO
50%
$t_{AA}$
WF12210S

**Read Mode**

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# 10422C
## 1K-Bit ECL Bipolar RAM

***Preliminary Specification***

**Bipolar Memory Products**

### DESCRIPTION

The 10422C device is a 256-word by 4-bit, fully encoded ECL Read/Write Random Access Memory designed for high-speed scratch pad, control, and buffer storage applications. The 10422C is available in a slimline 24-pin dual-in-line, flat or leadless package. This circuit may be reconfigured as 512 × 2 or 1024 × 1 organization by utilizing the block select feature. Each block has its own LOW active block select to enable the output. Write enable LOW active enables the write function in selected blocks. The memory has eight Address inputs, four Data inputs, four Block Select inputs, one Write Enable input and four Data outputs. The Open Emitter outputs have a 50Ω drive capability. The input pull-down resistor to $V_{CC}$ is 50,000Ω typical for the block selects.

Ordering information can be found on the following page.

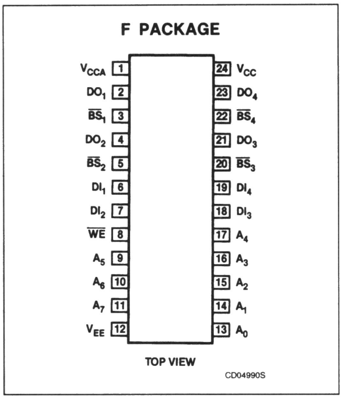
### FEATURES

- **256 words × 4 bits organization**
- **Fully compatible with 10K series ECL families**
- **Address access time:**
  - **10422C, 7ns max**
- **Low power dissipation of 0.8mW/bit**
- **Operating temperature: 0°C to +75°C (ambient)**
- **Block select allows variable organization**

### APPLICATIONS

- **High speed scratch pad**
- **Control and buffer storage**

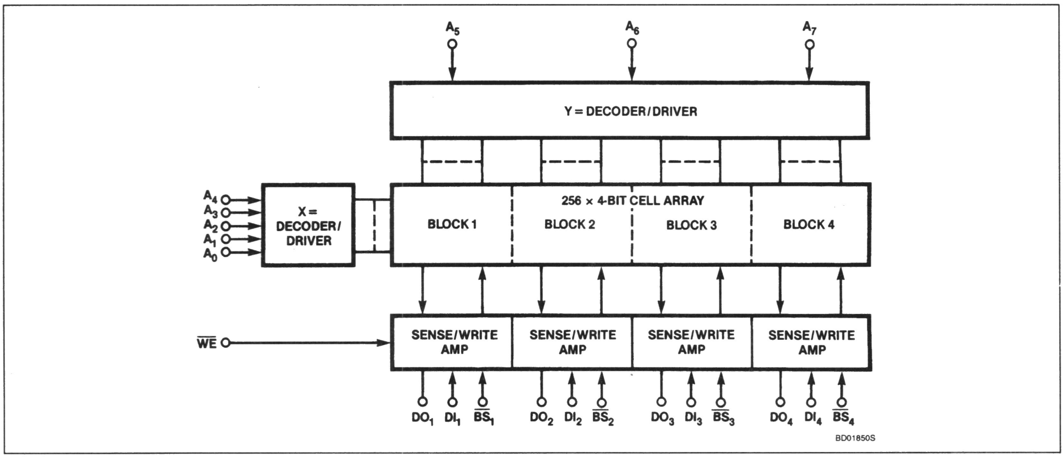
### PIN CONFIGURATION


F PACKAGE
VCCA 1
DO1 2
BS1 3
DO2 4
BS2 5
DI1 6
DI2 7
WE 8
A5 9
A6 10
A7 11
VEE 12
24 VCC
23 DO4
22 BS4
21 DO3
20 BS3
19 DI4
18 DI3
17 A4
16 A3
15 A2
14 A1
13 A0
TOP VIEW
CD04990S

### ABSOLUTE MAXIMUM RATINGS

| PARAMETER | | RATING | UNIT |
|---|---|---|---|
| $V_{EE}$ | Supply voltage | +0.5 to −7 | $V_{dc}$ |
| $V_{IN}$ | Input voltage | 0 to $V_{EE}$ | |
| $I_O$ | Output current | −30 | mA |
| $T_A$ | Operating | 0 to +75 | °C |
| $T_J$ | Operating junction | 125 | |
| $T_{STG}$ | Storage | −55 to +150 | |

### BLOCK DIAGRAM


A5
A6
A7
Y = DECODER/DRIVER
A4
A3
A2
A1
A0
X = DECODER/ DRIVER
256 × 4-BIT CELL ARRAY
BLOCK 1
BLOCK 2
BLOCK 3
BLOCK 4
WE
SENSE/WRITE AMP
SENSE/WRITE AMP
SENSE/WRITE AMP
SENSE/WRITE AMP
DO1 DI1 BS1
DO2 DI2 BS2
DO3 DI3 BS3
DO4 DI4 BS4
BD01850S

# 1K-Bit ECL Bipolar RAM (256 × 4) 10422C

## ORDERING CODE

| DESCRIPTION | ORDER CODE |
|---|---|
| Ceramic Dual Inline<br>400mil wide 24-pin | 10422C F |

## DC ELECTRICAL CHARACTERISTICS $V_{EE}$ = −5.2V±5%, $R_L$ = 50Ω to −2V

| PARAMETER | | TEST CONDITIONS | 0°C | | +25°C | | +75°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | |
| **Input voltage** | | | | | | | | | |
| $V_{IH}$ | High | | −1.145 | −0.840 | −1.105 | −0.810 | −1.045 | −0.720 | V |
| $V_{IL}$ | Low | | −1.870 | −1.490 | −1.850 | −1.475 | −1.830 | −1.450 | |
| **Output voltage** | | | | | | | | | |
| $V_{OH}$ | High | $V_{IH}$ = Max | −1.0 | −0.840 | −0.960 | −0.810 | −0.900 | −0.720 | V |
| $V_{OL}$ | Low | $V_{IL}$ = Min | −1.870 | −1.665 | −1.850 | −1.650 | −1.830 | −1.625 | |
| $V_{OHT}$ | Threshold HIGH | $V_{IH}$ = Min | −1.020 | | −0.980 | | −0.920 | | |
| $V_{OLT}$ | Threshold LOW | $V_{IL}$ = Max | | −1.645 | | −1.630 | | −1.605 | |
| **Input current** | | | | | | | | | |
| $I_{IH}$ | High | $V_{IH}$ = Max | | 220 | | 220 | | 220 | µA |
| $I_{IL}$ | Low | $V_{IL}$ = Min | −50 | | −50 | | −50 | | |
| $I_{IL}$ | $\overline{BS}$ | $V_{IL}$ = Min | 0.5 | | 0.5 | | 0.5 | | |
| $I_{EE}$ | Supply current | $V_{IL}$ = Min | | 200 | | 200 | | 200 | mA |

**NOTES:**

1. Voltages are defined with respect to ground, pins 1 and 24.
2. Unit is in a test socket or mounted in a printed circuit board with transverse air flow > 400 ft/min.
3. DC limits apply after thermal equilibrium has been established.
4. For current measurement, maximum is defined as the maximum absolute value.

## AC ELECTRICAL CHARACTERISTICS $V_{CC}$ = 0V, $V_{EE}$ = −5.2V±5%, $R_L$ = 50Ω to −2V, $T_A$ = 0°C to +75°C

| PARAMETER | | LIMITS | | | UNIT |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $T_{AA}$ | Address access time | | | 7 | ns |
| $T_{RBS}$ | Block select recovery time | | 4 | | |
| $T_{ABS}$ | Block select access time | | 6 | | |
| $T_{WD}$ | Write disable time | | 4 | | |
| $T_{WPW}$ | Write pulse width | 5 | | | |
| $T_{WR}$ | Write recovery time | | 6 | | |
| $T_{WHA}$ | Address hold time | | 1 | | |
| $T_{WHBS}$ | Block select hold time | | 1 | | |
| $T_{WHD}$ | Data hold time | | 1 | | |
| $T_{WSA}$ | Address set-up time | | 1 | | |
| $T_{WSBS}$ | Block select set-up time | | 1 | | |
| $T_{WSD}$ | Data set-up time | | 1 | | |
| $t_f$ | Output fall time | | 2 | | |
| $t_r$ | Output rise time | | 2 | | |
| **Capacitance** | | | | | |
| $C_{IN}$ | Input | | | 8 | pF |
| $C_{OUT}$ | Output | | | 8 | |

**NOTES:**

1. AC limits apply after thermal equilibrium has been established.
2. Unit is in a test socket or mounted on a printed circuit board with transverse air flow > 400 ft/min.
3. Output fall and rise times are measured between 20% and 80% points.
4. All propagation measurements to output are measured from 50% of the input pulse to 50% output level.

# 1K-Bit ECL Bipolar RAM (256 × 4)

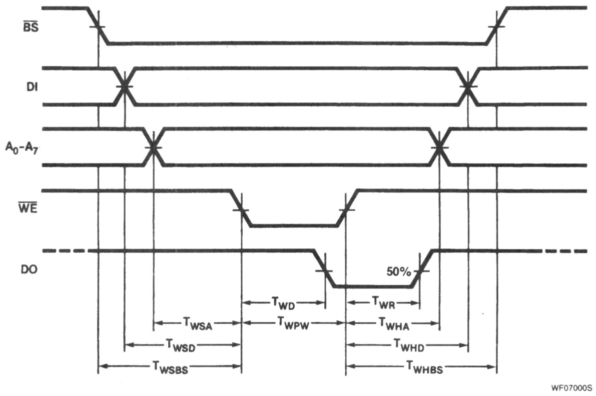
# 10422C

## TRUTH TABLE

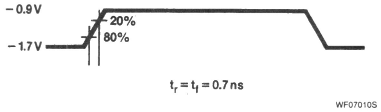
| MODE | INPUTS | | | OUTPUTS |
|---|---|---|---|---|
| | $\overline{BS}_N$ | $\overline{WE}$ | $DI_N$ | |
| Disable | H | X | X | L |
| Write 0 | L | L | L | L |
| Write 1 | L | L | H | L |
| Read | L | H | X | $D_{OUT}$ |

**NOTES:**
H = HIGH voltage level
L = LOW voltage level
X = Don't care
N = Blocks 1 – 4

## TIMING DIAGRAMS

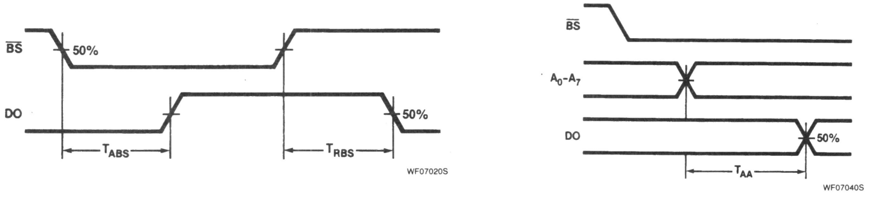

$\overline{BS}$
DI
$A_0$-$A_7$
$\overline{WE}$
DO
50%
$T_{WD}$
$T_{WR}$
$T_{WSA}$
$T_{WPW}$
$T_{WHA}$
$T_{WSD}$
$T_{WHD}$
$T_{WSBS}$
$T_{WHBS}$
WF07000S

**Write Mode**


– 0.9 V
– 1.7 V
20%
80%
$t_r = t_f = 0.7$ ns
WF07010S

**NOTE:**
All timing measurements referenced to 50% of input levels.

**Input Levels**


$\overline{BS}$
50%
DO
50%
$T_{ABS}$
$T_{RBS}$
WF07020S
$\overline{BS}$
$A_0$-$A_7$
DO
50%
$T_{AA}$
WF07040S

**Read Mode**

# 10470A

## 4K-Bit ECL Bipolar RAM

***Preliminary Specification***

**Bipolar Memory Products**

### DESCRIPTION

The 10470A device is a 4096 words by 1 bit fully decoded Read/Write Random Access Memory, designed for high speed scratch pad, control and buffer storage applications. The device also includes full address decoding, on-chip separate data in and noninverting data out lines, and an active LOW Chip Select input.

The 10470A is compatible with the 10K ECL families and includes on-chip voltage compensation for improved noise margin.

Ordering information can be found on the following page.

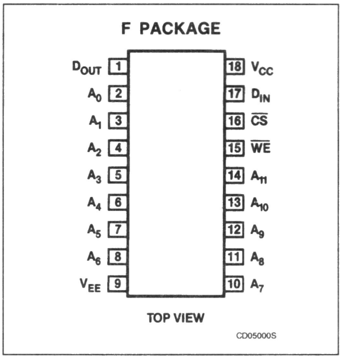
### FEATURES

- **Organization: 4096 words by 1 bit**
- **Fully compatible with 10K ECL families**
- **Operating temperature: 0°C to +75°C**
- **Address access time:**
  - **10470A: 15ns max**
- **Low supply current of 150mA max**
- **Read cycle time**
  - **10470A: 15ns**

### APPLICATIONS

- **High speed scratch pad**
- **Control and buffer storage**

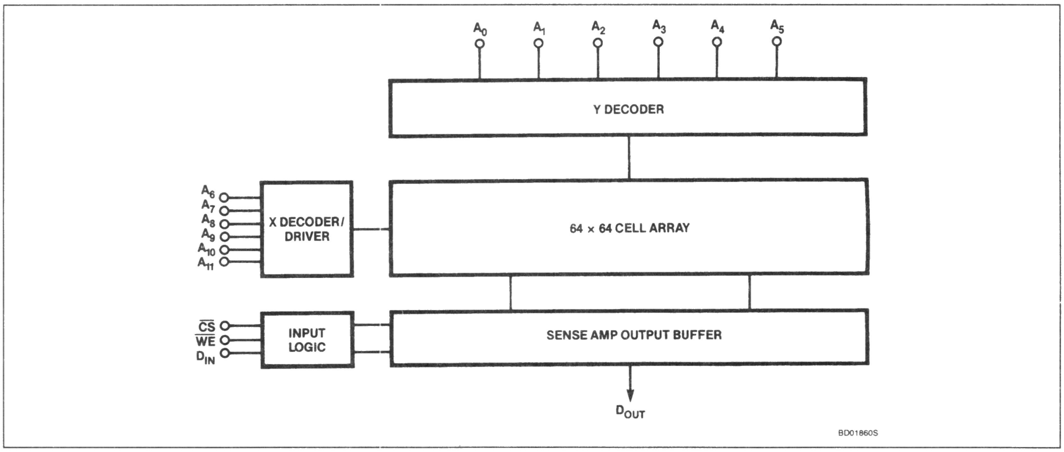
### PIN CONFIGURATION


F PACKAGE
$D_{OUT}$ 1
$A_0$ 2
$A_1$ 3
$A_2$ 4
$A_3$ 5
$A_4$ 6
$A_5$ 7
$A_6$ 8
$V_{EE}$ 9
18 $V_{CC}$
17 $D_{IN}$
16 $\overline{CS}$
15 $\overline{WE}$
14 $A_{11}$
13 $A_{10}$
12 $A_9$
11 $A_8$
10 $A_7$
TOP VIEW
CD05000S

### ABSOLUTE MAXIMUM RATINGS

| PARAMETER | | RATING | UNIT |
|---|---|---|---|
| $V_{EE}$ | Supply voltage | +0.5 to −7 | $V_{dc}$ |
| $V_{IN}$ | Input voltage | +0.5 to $V_{EE}$ | |
| $I_O$ | Output current | −30 | mA |
| $T_A$ | Operating | 0 to +75 | °C |
| $T_{STG}$ | Storage | −55 to +150 | |

### BLOCK DIAGRAM


$A_0$
$A_1$
$A_2$
$A_3$
$A_4$
$A_5$
Y DECODER
$A_6$
$A_7$
$A_8$
$A_9$
$A_{10}$
$A_{11}$
X DECODER/ DRIVER
64 × 64 CELL ARRAY
$\overline{CS}$
$\overline{WE}$
$D_{IN}$
INPUT LOGIC
SENSE AMP OUTPUT BUFFER
$D_{OUT}$
BD01860S

# 4K-Bit ECL Bipolar RAM (4096 × 1) 10470A

## ORDERING CODE

| DESCRIPTION | ORDER CODE |
|---|---|
| Ceramic Dual Inline<br>300mil wide 18-pin | 10470A F |

## DC ELECTRICAL CHARACTERISTICS $V_{EE} = -5.2V \pm 5\%$, $R_L = 50\Omega$ to $-2V$

| PARAMETER | | TEST CONDITIONS | 0°C | | +25°C | | +75°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | |
| **Input voltage** | | | | | | | | | |
| $V_{IH}$ | High | | −1.145 | −0.840 | −1.105 | −0.810 | −1.045 | −0.720 | V |
| $V_{IL}$ | Low | | −1.870 | −1.490 | −1.850 | −1.475 | −1.830 | −1.450 | |
| **Output voltage** | | | | | | | | | |
| $V_{OH}$ | High | $V_{IH}$ = Max | −1.0 | −0.840 | −0.960 | −0.810 | −0.900 | −0.720 | V |
| $V_{OL}$ | Low | $V_{IL}$ = Min | −1.870 | −1.665 | −1.850 | −1.650 | −1.830 | −1.625 | |
| $V_{OHT}$ | Threshold HIGH | $V_{IH}$ = Min | −1.020 | | −0.980 | | −0.920 | | |
| $V_{OLT}$ | Threshold LOW | $V_{IL}$ = Max | | −1.645 | | −1.630 | | −1.605 | |
| **Input current** | | | | | | | | | |
| $I_{IH}$ | High | $V_{IH}$ = Max | | 220 | | 220 | | 220 | μA |
| $I_{IL}$ | Low | $V_{IL}$ = Min | −50 | | −50 | | −50 | | |
| $I_{IL}$ | $\overline{CS}$ | $V_{IL}$ = Min | 0.5 | | 0.5 | | 0.5 | | |
| $I_{EE}$ | Supply current | $V_{IL}$ = Min | | 150 | | 150 | | 150 | mA |

**NOTES:**
1. Voltages are defined with respect to ground, pin 18.
2. Unit is in a test socket or mounted in a printed circuit board with transverse air flow > 400 ft/min.
3. DC limits apply after thermal equilibrium has been established.
4. For current measurement, maximum is defined as the maximum absolute value.

## AC ELECTRICAL CHARACTERISTICS $V_{CC} = 0V$, $V_{EE} = -5.2V \pm 5\%$, $R_L = 50\Omega$ to $-2V$, $T_A = 0°C$ to $+75°C$

| PARAMETER | | LIMITS | | | UNIT |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $T_{AA}$ | Address access time | | | 15 | ns |
| $T_{RCS}$ | Chip select recovery time | | | 5 | |
| $T_{ACS}$ | Chip select access time | | | 5 | |
| $T_{WD}$ | Write disable time | | | 6 | |
| $T_{WPW}$ | Write pulse width | 10 | | | |
| $T_{WR}$ | Write recovery time | | | 10 | |
| $T_{WHA}$ | Address hold time | 3 | | | |
| $T_{WHCS}$ | Chip select hold time | 3 | | | |
| $T_{WHD}$ | Data hold time | 3 | | | |
| $T_{WSA}$ | Address set-up time | 3 | | | |
| $T_{WSCS}$ | Chip select set-up time | 3 | | | |
| $T_{WSD}$ | Data set-up time | 3 | | | |
| $t_f$ | Output fall time | | 1.5 | | |
| $t_r$ | Output rise time | | 1.5 | | |
| **Capacitance** | | | | | |
| $C_{IN}$ | Input | | | 8 | pF |
| $C_{OUT}$ | Output | | | 8 | |

**NOTES:**
1. AC limits apply after thermal equilibrium has been established.
2. Unit is in a test socket or mounted on a printed circuit board with transverse air flow > 400 ft/min.
3. Output fall and rise times are measured between 20% and 80% points.
4. All propagation measurements to output are measured from 50% of the input pulse to 50% output level.

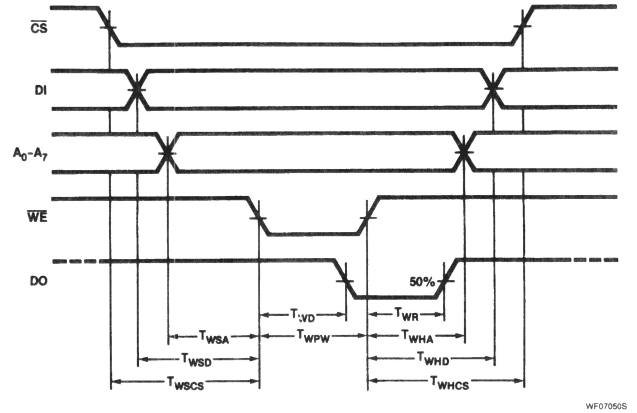
## 4K-Bit ECL Bipolar RAM (4096 × 1) 10470A

### TRUTH TABLE

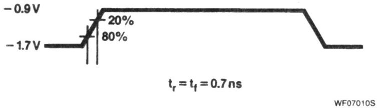
| MODE | INPUTS | | | OUTPUTS |
|---|---|---|---|---|
| | $\overline{CS}$ | $\overline{WE}$ | $D_{IN}$ | |
| Disable | H | X | X | L |
| Write 0 | L | L | L | L |
| Write 1 | L | L | H | L |
| Read | L | H | X | $D_{OUT}$ |

**NOTES:**
H = HIGH voltage level
L = LOW voltage level
X = Don't care

### TIMING DIAGRAMS

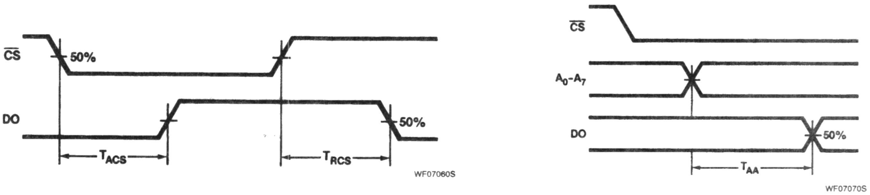

CS
DI
A0-A7
WE
DO
50%
TWVD
TWR
TWSA
TWPW
TWHA
TWSD
TWHD
TWSCS
TWHCS
WF07050S

**Write Mode**


-0.9V
-1.7V
20%
80%
tr = tf = 0.7ns
WF07010S

**NOTE:**
All timing measurements referenced to 50% of input levels.

**Input Levels**


CS
50%
DO
50%
TACS
TRCS
WF07060S
CS
A0-A7
DO
50%
TAA
WF07070S

**Read Mode**

**Signetics**

**Bipolar Memory Products**

# 10474A

## 4K-Bit ECL Bipolar RAM

***Preliminary Specification***

## DESCRIPTION

The 10474A device is a 1024 words by 4 bits fully decoded Read/Write Random Access Memory, designed for high speed scratch pad, control and buffer storage applications. The device also includes full address decoding, on-chip separate data in and noninverting data out lines.

The 10474A is compatible with the 10K ECL families and includes on-chip voltage compensation for improved noise margin.

Ordering information can be found on the following page.

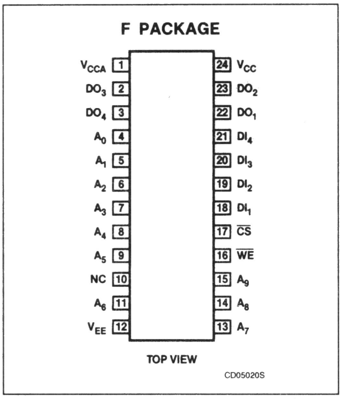
## FEATURES

- **Organization: 1024 words by 4 bits**
- **Fully compatible with 10K ECL families**
- **Operating temperature: 0°C to +75°C**
- **Address access time**
  - **- 10474A: 15ns max**
- **Low supply current of 210mA max**
- **Read cycle time:**
  - **- 10474A: 15ns**

## APPLICATIONS

- **High speed scratch pad**
- **Control and buffer storage**

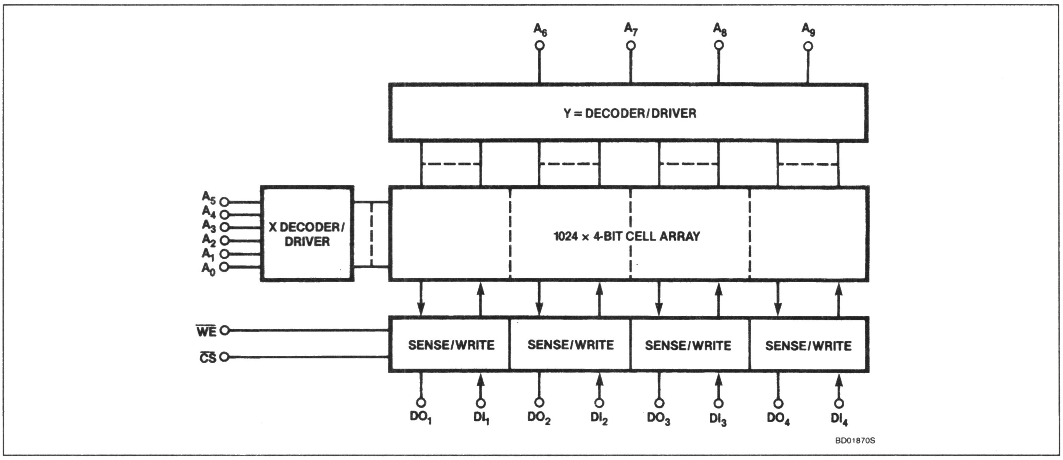
## PIN CONFIGURATION


F PACKAGE
$V_{CCA}$ 1
$DO_3$ 2
$DO_4$ 3
$A_0$ 4
$A_1$ 5
$A_2$ 6
$A_3$ 7
$A_4$ 8
$A_5$ 9
NC 10
$A_6$ 11
$V_{EE}$ 12
24 $V_{CC}$
23 $DO_2$
22 $DO_1$
21 $DI_4$
20 $DI_3$
19 $DI_2$
18 $DI_1$
17 $\overline{CS}$
16 $\overline{WE}$
15 $A_9$
14 $A_8$
13 $A_7$
TOP VIEW
CD05020S

## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | | RATING | UNIT |
|---|---|---|---|
| $V_{EE}$ | Supply voltage | +0.5 to −7 | $V_{dc}$ |
| $V_{IN}$ | Input voltage | +0.5 to $V_{EE}$ | |
| $I_O$ | Output current | −30 | mA |
| $T_A$ | Operating | 0 to +75 | °C |
| $T_{STG}$ | Storage | −55 to +150 | |

## BLOCK DIAGRAM


$A_6$
$A_7$
$A_8$
$A_9$
Y = DECODER/DRIVER
$A_5$
$A_4$
$A_3$
$A_2$
$A_1$
$A_0$
X DECODER/ DRIVER
1024 × 4-BIT CELL ARRAY
$\overline{WE}$
$\overline{CS}$
SENSE/WRITE
SENSE/WRITE
SENSE/WRITE
SENSE/WRITE
$DO_1$
$DI_1$
$DO_2$
$DI_2$
$DO_3$
$DI_3$
$DO_4$
$DI_4$
BD01870S

# 4K-Bit ECL Bipolar RAM (1024 × 4) 10474A

## ORDERING CODE

| DESCRIPTION | ORDER CODE |
|---|---|
| Ceramic Dual Inline<br>400mil wide 24-pin | 10474A F |

## DC ELECTRICAL CHARACTERISTICS $V_{EE} = -5.2V \pm 5\%$, $R_L = 50\Omega$ to $-2V$

| PARAMETER | | TEST CONDITIONS | 0°C | | +25°C | | +75°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | |
| **Input voltage** | | | | | | | | | |
| $V_{IH}$ | High | | −1.145 | −0.840 | −1.105 | −0.810 | −1.045 | −0.720 | V |
| $V_{IL}$ | Low | | −1.870 | −1.490 | −1.850 | −1.475 | −1.830 | −1.450 | |
| **Output voltage** | | | | | | | | | |
| $V_{OH}$ | High | $V_{IH}$ = Max | −1.0 | −0.840 | −0.960 | −0.810 | −0.900 | −0.720 | V |
| $V_{OL}$ | Low | $V_{IL}$ = Min | −1.870 | −1.665 | −1.850 | −1.650 | −1.830 | −1.625 | |
| $V_{OHT}$ | Threshold HIGH | $V_{IH}$ = Min | −1.020 | | −0.980 | | −0.920 | | |
| $V_{OLT}$ | Threshold LOW | $V_{IL}$ = Max | | −1.645 | | −1.630 | | −1.605 | |
| **Input current** | | | | | | | | | |
| $I_{IH}$ | High | $V_{IH}$ = Max | | 220 | | 220 | | 220 | μA |
| $I_{IL}$ | Low | $V_{IL}$ = Min | −50 | | −50 | | −50 | | |
| $I_{IL}$ | $\overline{CS}$ | $V_{IL}$ = Min | 0.5 | | 0.5 | | 0.5 | | |
| $I_{EE}$ | Supply current | $V_{IL}$ = Min | | 210 | | 210 | | 210 | mA |

**NOTES:**

1. Voltages are defined with respect to ground, pins 1 and 24.
2. Unit is in a test socket or mounted in a printed circuit board with transverse air flow > 400 ft/min.
3. DC inputs apply after thermal equilibrium has been established.
4. For current measurement, maximum is defined as the maximum absolute value.

## AC ELECTRICAL CHARACTERISTICS $V_{CC} = 0V$, $V_{EE} = -5.2V \pm 5\%$, $R_L = 50\Omega$ to $-2V$, $T_A = 0°C$ to $+75°C$

| PARAMETER | | LIMITS | | | UNIT |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $T_{AA}$ | Address access time | | | 15 | ns |
| $T_{RCS}$ | Chip select recovery time | | | 5 | |
| $T_{ACS}$ | Chip select access time | | | 5 | |
| $T_{WD}$ | Write disable time | | | 6 | |
| $T_{WPW}$ | Write pulse width | 10 | | | |
| $T_{WR}$ | Write recovery time | | | 10 | |
| $T_{WHA}$ | Address hold time | 3 | | | |
| $T_{WHCS}$ | Chip select hold time | 3 | | | |
| $T_{WHD}$ | Data hold time | 3 | | | |
| $T_{WSA}$ | Address setup time | 3 | | | |
| $T_{WSCS}$ | Chip select setup time | 3 | | | |
| $T_{WSD}$ | Data setup time | 3 | | | |
| $t_f$ | Output fall time | | 1.5 | | |
| $t_r$ | Output rise time | | 1.5 | | |
| **Capacitance** | | | | | |
| $C_{IN}$ | Input | | | 8 | pF |
| $C_{OUT}$ | Output | | | 8 | |

**NOTES:**

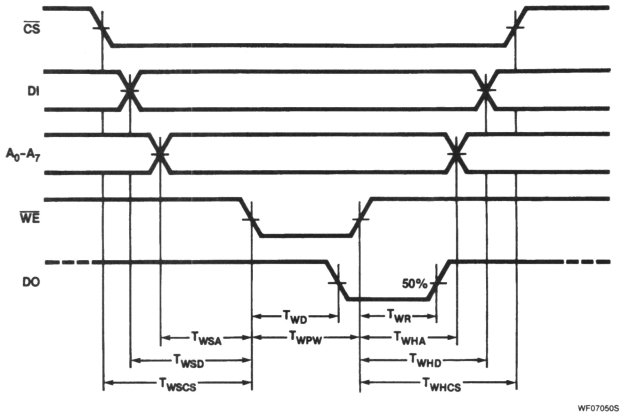
1. AC limits apply after thermal equilibrium has been established.
2. Unit is in a test socket or mounted on a printed circuit board with transverse air flow > 400 ft/min.
3. Output fall and rise times are measured between 20% and 80% points.
4. All propagation measurements to output are measured from 50% of the input pulse to 50% output level.

## TRUTH TABLE

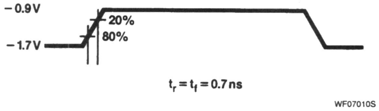
| MODE | INPUTS | | | OUTPUTS |
|---|---|---|---|---|
| | $\overline{CS}$ | $\overline{WE}$ | $D_{IN}$ | |
| Disable | H | X | X | L |
| Write 0 | L | L | L | L |
| Write 1 | L | L | H | L |
| Read | L | H | X | $D_{OUT}$ |

**NOTES:**
H = HIGH voltage level
L = LOW voltage level
X = Don't care

## TIMING DIAGRAMS

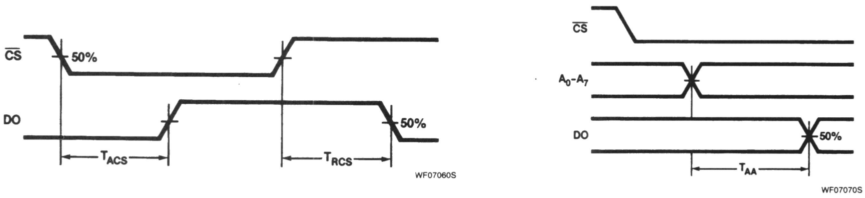

$\overline{CS}$
DI
$A_0$-$A_7$
$\overline{WE}$
DO
50%
$T_{WD}$
$T_{WR}$
$T_{WSA}$
$T_{WPW}$
$T_{WHA}$
$T_{WSD}$
$T_{WHD}$
$T_{WSCS}$
$T_{WHCS}$
WF07050S

**Write Mode**


−0.9V
−1.7V
20%
80%
$t_r = t_f = 0.7ns$
WF07010S

**NOTE:**
All timing measurements referenced to 50% of input levels.

**Input Levels**


$\overline{CS}$
50%
DO
50%
$T_{ACS}$
$T_{RCS}$
WF07060S
$\overline{CS}$
$A_0$-$A_7$
DO
50%
$T_{AA}$
WF07070S

**Read Mode**

**Signetics**

# 100422B
## 1K-Bit ECL Bipolar RAM

***Preliminary Specification***

**Bipolar Memory Products**

### DESCRIPTION

The 100422B device is a 256-word by 4-bit, fully encoded ECL Read/Write Random Access Memory designed for high-speed scratchpad, control, and buffer storage applications. The 100422B contains voltage and temperature compensation circuits making it 100K family compatible. The 100422B is available in a slimline 24-pin dual-in-line package. This circuit may be reconfigured as 512 × 2 or 1024 × 1 organization by utilizing the block select feature. Each block has its own LOW active block select to enable the output. Write enable LOW active enables the write function in selected blocks. The memory has eight Address inputs, four Data inputs, four Block Select inputs, one Write Enable input and four Data outputs. The outputs require external resistance terminations as they are not terminated internally through resistance to the $V_{EE}$ supply voltage. The input pull-down resistor to $V_{EE}$ is 50,000Ω typical for the block selects.

Ordering information can be found on the following page.

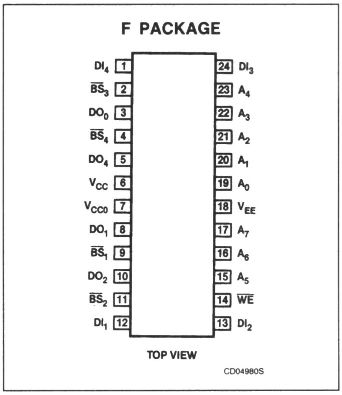
### FEATURES

- **256 words × 4 bits organization**
- **Fully compatible with 100K series ECL families**
- **Address access time:**
  - **100422B: 10ns max.**
- **Low power dissipation of 0.8mW/bit**
- **Operating temperature: 0°C to +85°C**
- **Block select allows variable organization**

### APPLICATIONS

- **High-speed scratchpad**
- **Control and buffer storage**

### PIN CONFIGURATION

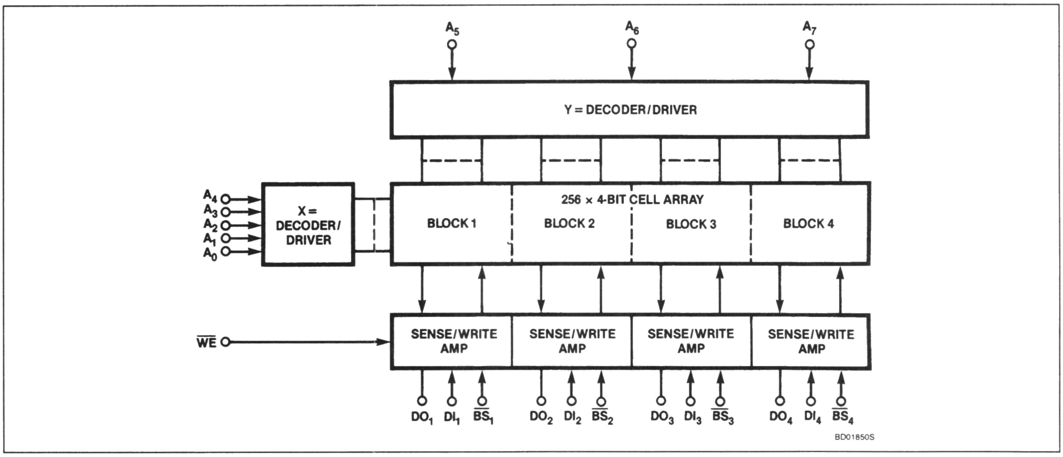


F PACKAGE
$DI_4$ 1
$\overline{BS}_3$ 2
$DO_0$ 3
$\overline{BS}_4$ 4
$DO_4$ 5
$V_{CC}$ 6
$V_{CCO}$ 7
$DO_1$ 8
$\overline{BS}_1$ 9
$DO_2$ 10
$\overline{BS}_2$ 11
$DI_1$ 12
24 $DI_3$
23 $A_4$
22 $A_3$
21 $A_2$
20 $A_1$
19 $A_0$
18 $V_{EE}$
17 $A_7$
16 $A_6$
15 $A_5$
14 $\overline{WE}$
13 $DI_2$
TOP VIEW
CD04980S

### ABSOLUTE MAXIMUM RATINGS

| PARAMETER | | RATING | UNIT |
|---|---|---|---|
| $V_{EE}$ | Supply voltage | +0.5 to −7 | $V_{DC}$ |
| $V_{IN}$ | Input voltage | 0 to $V_{EE}$ | |
| $I_O$ | Output current | −30 | mA |
| $T_A$ | Operating ambient temperature | 0 to +85 | °C |
| $T_J$ | Operating junction temperature | +125 | |
| $T_{STG}$ | Storage temperature | −55 to +150 | |

### BLOCK DIAGRAM



$A_5$
$A_6$
$A_7$
Y = DECODER/DRIVER
$A_4$
$A_3$
$A_2$
$A_1$
$A_0$
X = DECODER/ DRIVER
256 x 4-BIT CELL ARRAY
BLOCK 1
BLOCK 2
BLOCK 3
BLOCK 4
$\overline{WE}$
SENSE/WRITE AMP
SENSE/WRITE AMP
SENSE/WRITE AMP
SENSE/WRITE AMP
$DO_1$ $DI_1$ $\overline{BS}_1$
$DO_2$ $DI_2$ $\overline{BS}_2$
$DO_3$ $DI_3$ $\overline{BS}_3$
$DO_4$ $DI_4$ $\overline{BS}_4$
BD01850S

# 1K-Bit ECL Bipolar RAM (256 × 4) 100422B

## ORDERING CODE

| DESCRIPTION | ORDER CODE |
|---|---|
| Ceramic Dual-In-line<br>400mil wide 24-pin | 100422B F |

## DC ELECTRICAL CHARACTERISTICS $V_{CC} = 0V$, $V_{EE} = -4.5V \pm 5\%$, $R_L = 50\Omega$ to $-2V$, $T_A = 0°C$ to $85°C$

| PARAMETER | | TEST CONDITIONS | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| **Input voltage** | | | | | | V |
| $V_{IL}$ | Low | | −1.810 | | −1.475 | |
| $V_{IH}$ | High | | −1.165 | | −0.880 | |
| **Output voltage** | | | | | | V |
| $V_{OL}$ | Low | $V_{IL}$ = Min | −1.810 | −1.715 | −1.620 | |
| $V_{OH}$ | High | $V_{IH}$ = Max | −1.025 | −0.955 | −0.880 | |
| $V_{OLT}$ | Threshold LOW | $V_{IL}$ = Max | | | −1.610 | |
| $V_{OHT}$ | Threshold HIGH | $V_{IH}$ = Min | −1.035 | | | |
| **Input current** | | | | | | µA |
| $I_{IL}$ | Low | $V_{IL}$ = Min | −50 | | | |
| $I_{IL}$ | $\overline{BS}$ | $V_{IL}$ = Min | +0.5 | | | |
| $I_{IH}$ | High | $V_{IH}$ = Max | | | 220 | |
| $I_{EE}$ | Supply current | | | | 210 | mA |

**NOTES:**
1. Voltages are defined with respect to ground, pins 6 and 7.
2. Unit is in a test socket or mounted in a printed circuit board with transverse air flow > 400ft/min.
3. DC limits apply after thermal equilibrium has been established.
4. For current measurement, maximum is defined as the maximum absolute value.

## AC ELECTRICAL CHARACTERISTICS $V_{CC} = 0V$, $V_{EE} = -4.5V \pm 5\%$, $R_L = 50\Omega$ to $-2V$, $T_A = 0°C$ to $85°C$

| PARAMETER | | LIMITS | | | UNIT |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $t_{AA}$ | Address access time | | | 10 | ns |
| $t_{RBS}$ | Block select recovery time | | | 5 | |
| $t_{ABS}$ | Block select access time | | | 5 | |
| $t_{WD}$ | Write disable time | | | 5 | |
| $t_{WPW}$ | Write pulse width | 7 | | | |
| $t_{WR}$ | Write recovery time | | 4.5 | 9 | |
| $t_{WHA}$ | Address hold time | 2 | 1 | | |
| $t_{WHBS}$ | Block select hold time | 2 | 1 | | |
| $t_{WHD}$ | Data hold time | 2 | 1 | | |
| $t_{WSA}$ | Address setup time | 3 | 1 | | |
| $t_{WSBS}$ | Block select setup time | 2 | 1 | | |
| $t_{WSD}$ | Data setup time | 2 | 1 | | |
| $t_f$ | Output fall time | | 2 | | |
| $t_r$ | Output rise time | | 2 | | |
| **Capacitance** | | | | | pF |
| $C_{IN}$ | Input | | | 8 | |
| $C_{OUT}$ | Output | | | 8 | |

**NOTES:**
1. AC limits apply after thermal equilibrium has been established.
2. Unit is in a test socket or mounted on a printed circuit board with transverse air flow > 400ft/min.
3. Output fall and rise times are measured between 20% and 80% points.
4. All propagation measurements to output are measured from 50% of the input pulse to 50% output level.

# 1K-Bit ECL Bipolar RAM (256 × 4)

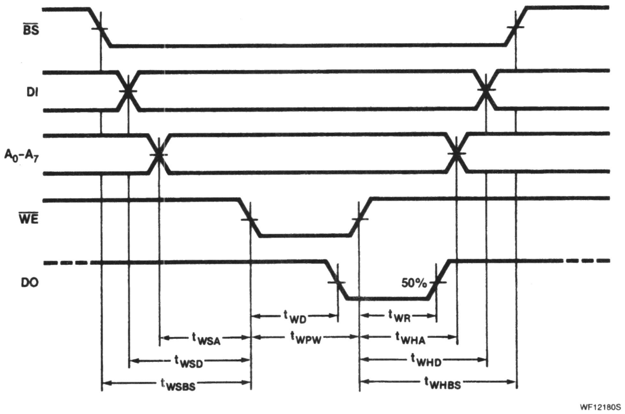
# 100422B

## TRUTH TABLE

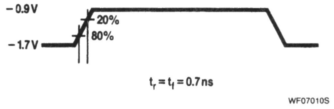
| MODE | INPUTS | | | OUTPUTS |
|---|---|---|---|---|
| | $\overline{BS_N}$ | $\overline{WE}$ | $DI_N$ | |
| Disable | H | X | X | L |
| Write 0 | L | L | L | L |
| Write 1 | L | L | H | L |
| Read | L | H | X | $D_{OUT}$ |

**NOTES:**
H = HIGH voltage level
L = LOW voltage level
X = Don't Care
N = Blocks 1 – 4

## TIMING DIAGRAMS

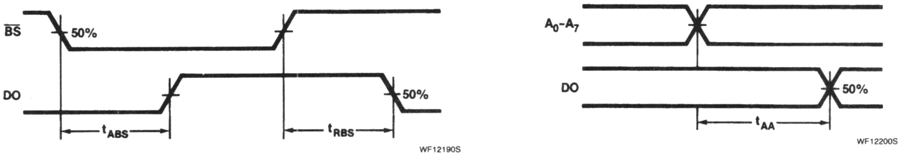

$\overline{BS}$
DI
$A_0$-$A_7$
$\overline{WE}$
DO
50%
$t_{WD}$
$t_{WR}$
$t_{WSA}$
$t_{WPW}$
$t_{WHA}$
$t_{WSD}$
$t_{WHD}$
$t_{WSBS}$
$t_{WHBS}$
WF12180S

**Write Mode**


−0.9V
−1.7V
20%
80%
$t_r = t_f = 0.7ns$
WF07010S

**NOTE:**
All timing measurements referenced to 50% of input levels.

**Input Levels**


$\overline{BS}$
50%
DO
50%
$t_{ABS}$
$t_{RBS}$
WF12190S
$A_0$-$A_7$
DO
50%
$t_{AA}$
WF12200S

**Read Mode**

**Signetics**

# 100422C
## 1K-Bit ECL Bipolar RAM

***Preliminary Specification***

**Bipolar Memory Products**

### DESCRIPTION

The 100422C device is a 256-word by 4-bit, fully encoded ECL Read/Write Random Access Memory designed for high-speed scratch pad, control, and buffer storage applications. The 100422C contains voltage and temperature compensation circuits making it 100K family compatible. The 100422C is available in a slimline 24-pin dual-in-line package. This circuit may be reconfigured as 512 × 2 or 1024 × 1 organization by utilizing the block select feature. Each block has its own LOW active block select to enable the output. Write enable LOW active enables the write function in selected blocks. The memory has eight Address inputs, four Data inputs, four Block Select inputs, one Write Enable input and four Data outputs. The outputs require external resistance terminations as they are not terminated internally through resistance to the $V_{EE}$ supply voltage. The input pull-down resistor to $V_{EE}$ is 50,000Ω typical for the block selects.

Ordering information can be found on the following page.

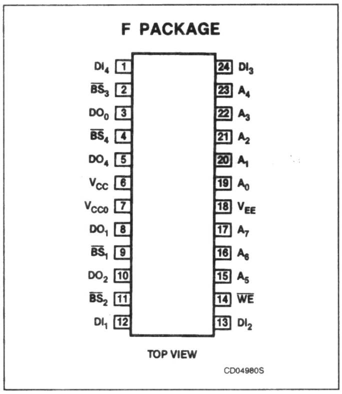
### FEATURES

- **256 words × 4 bits organization**
- **Fully compatible with 100K series ECL families**
- **Address access time:**
  - **100422C: 7ns max**
- **Low power dissipation of 0.8mW/bit**
- **Operating temperature: 0°C to +85°C**
- **Block select allows variable organization**

### APPLICATIONS

- **High speed scratch pad**
- **Control and buffer storage**

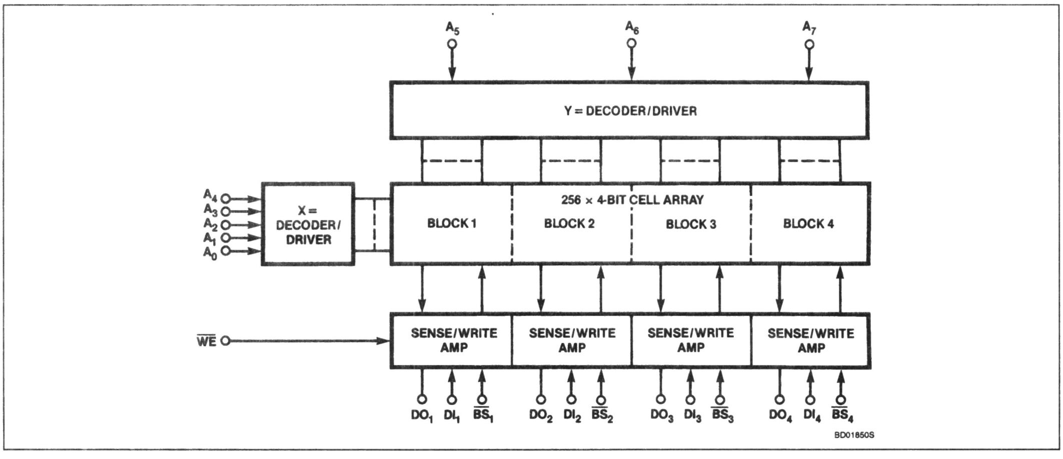
### PIN CONFIGURATION


F PACKAGE
$DI_4$ 1
$\overline{BS}_3$ 2
$DO_0$ 3
$\overline{BS}_4$ 4
$DO_4$ 5
$V_{CC}$ 6
$V_{CC0}$ 7
$DO_1$ 8
$\overline{BS}_1$ 9
$DO_2$ 10
$\overline{BS}_2$ 11
$DI_1$ 12
24 $DI_3$
23 $A_4$
22 $A_3$
21 $A_2$
20 $A_1$
19 $A_0$
18 $V_{EE}$
17 $A_7$
16 $A_6$
15 $A_5$
14 $\overline{WE}$
13 $DI_2$
TOP VIEW
CD04980S

### ABSOLUTE MAXIMUM RATINGS

| PARAMETER | | RATING | UNIT |
|---|---|---|---|
| $V_{EE}$ | Supply voltage | +0.5 to −7 | $V_{dc}$ |
| $V_{IN}$ | Input voltage | 0 to $V_{EE}$ | |
| $I_O$ | Output current | −30 | mA |
| $T_A$ | Operating | 0 to +85 | °C |
| $T_J$ | Operating junction | +125 | |
| $T_{STG}$ | Storage | −55 to +150 | |

### BLOCK DIAGRAM


$A_5$
$A_6$
$A_7$
Y = DECODER/DRIVER
$A_4$
$A_3$
$A_2$
$A_1$
$A_0$
X = DECODER/ DRIVER
256 × 4-BIT CELL ARRAY
BLOCK 1
BLOCK 2
BLOCK 3
BLOCK 4
$\overline{WE}$
SENSE/WRITE AMP
SENSE/WRITE AMP
SENSE/WRITE AMP
SENSE/WRITE AMP
$DO_1$ $DI_1$ $\overline{BS}_1$
$DO_2$ $DI_2$ $\overline{BS}_2$
$DO_3$ $DI_3$ $\overline{BS}_3$
$DO_4$ $DI_4$ $\overline{BS}_4$
BD01850S

# 1K-Bit ECL Bipolar RAM (256 × 4) 100422C

## ORDERING CODE

| DESCRIPTION | ORDER CODE |
|---|---|
| Ceramic Dual Inline<br>400mil wide 24-pin | 100422C F |

## DC ELECTRICAL CHARACTERISTICS $V_{CC} = 0V$, $V_{EE} = -4.5V \pm 5\%$, $R_L = 50\Omega$ to $-2V$, $T_A = 0°C$ to $85°C$

| PARAMETER | | TEST CONDITIONS | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| **Input voltage** | | | | | | |
| $V_{IL}$ | Low | | −1.810 | | −1.475 | V |
| $V_{IH}$ | High | | −1.165 | | −0.880 | |
| **Output voltage** | | | | | | |
| $V_{OL}$ | Low | $V_{IL}$ = Min | −1.810 | −1.715 | −1.620 | V |
| $V_{OH}$ | High | $V_{IH}$ = Max | −1.025 | −0.955 | −0.880 | |
| $V_{OLT}$ | Threshold LOW | $V_{IL}$ = Max | | | −1.610 | |
| $V_{OHT}$ | Threshold HIGH | $V_{IH}$ = Min | −1.035 | | | |
| **Input current** | | | | | | |
| $I_{IL}$ | Low | $V_{IL}$ = Min | −50 | | | µA |
| $I_{IL}$ | $\overline{BS}$ | $V_{IL}$ = Min | +0.5 | | | |
| $I_{IH}$ | High | $V_{IH}$ = Max | | | 220 | |
| $I_{EE}$ | Supply current | | | | 210 | mA |

**NOTES:**

1. Voltages are defined with respect to ground, pins 6 and 7.
2. Unit is in a test socket or mounted in a printed circuit board with transverse air flow > 400 ft/min.
3. DC limits apply after thermal equilibrium has been established.
4. For current measurement, maximum is defined as the maximum absolute value.

## AC ELECTRICAL CHARACTERISTICS $V_{CC} = 0V$, $V_{EE} = -4.5V \pm 5\%$, $R_L = 50\Omega$ to $-2V$, $T_A = 0°C$ to $85°C$

| PARAMETER | | LIMITS | | | UNIT |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $T_{AA}$ | Address access time | | | 7 | ns |
| $T_{RBS}$ | Block select recovery time | | 4 | | |
| $T_{ABS}$ | Block select access time | | 6 | | |
| $T_{WD}$ | Write disable time | | 4 | | |
| $T_{WPW}$ | Write pulse width | 5 | | | |
| $T_{WR}$ | Write recovery time | | 6 | | |
| $T_{WHA}$ | Address hold time | | 1 | | |
| $T_{WHBS}$ | Block select hold time | | 1 | | |
| $T_{WHD}$ | Data hold time | | 1 | | |
| $T_{WSA}$ | Address set-up time | | 1 | | |
| $T_{WSBS}$ | Block select set-up time | | 1 | | |
| $T_{WSD}$ | Data set-up time | | 1 | | |
| $t_f$ | Output fall time | | 2 | | |
| $t_r$ | Output rise time | | 2 | | |
| **Capacitance** | | | | | |
| $C_{IN}$ | Input | | | 8 | pF |
| $C_{OUT}$ | Output | | | 8 | |

**NOTES:**

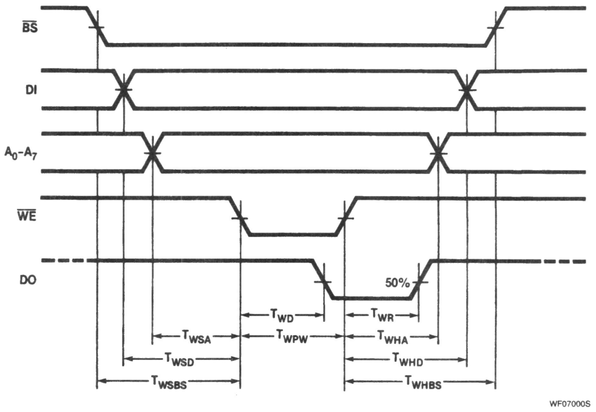
1. AC limits apply after thermal equilibrium has been established.
2. Unit is in a test socket or mounted on a printed circuit board with transverse air flow > 400 ft/min.
3. Output fall and rise times are measured between 20% and 80% points.
4. All propagation measurements to output are measured from 50% of the input pulse to 50% output level.

## TRUTH TABLE

| MODE | INPUTS | | | OUTPUTS |
|---|---|---|---|---|
| | $\overline{BS_N}$ | $\overline{WE}$ | $DI_N$ | |
| Disable | H | X | X | L |
| Write 0 | L | L | L | L |
| Write 1 | L | L | H | L |
| Read | L | H | X | $D_{OUT}$ |

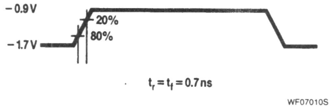
**NOTES:**
H = HIGH voltage level
L = LOW voltage level
X = Don't care
N = Blocks 1 – 4

## TIMING DIAGRAMS



$\overline{BS}$
DI
$A_0$-$A_7$
$\overline{WE}$
DO
50%
$T_{WD}$
$T_{WR}$
$T_{WSA}$
$T_{WPW}$
$T_{WHA}$
$T_{WSD}$
$T_{WHD}$
$T_{WSBS}$
$T_{WHBS}$
WF07000S

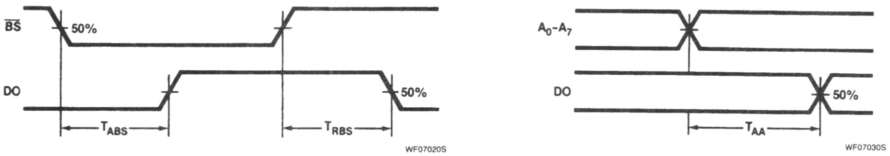
**Write Mode**



–0.9V
–1.7V
20%
80%
$t_r = t_f = 0.7ns$
WF07010S

NOTE:
All timing measurements referenced to 50% of input levels.

**Input Levels**



$\overline{BS}$
50%
DO
50%
$T_{ABS}$
$T_{RBS}$
WF07020S
$A_0$-$A_7$
DO
50%
$T_{AA}$
WF07030S

**Read Mode**

# 100470A
## 4K-Bit ECL Bipolar RAM

*Preliminary Specification*

**Bipolar Memory Products**

### DESCRIPTION

The 100470A device is a 4096 words by 1 bit fully decoded Read/Write Random Access Memory, designed for high speed scratch pad, control, and buffer storage applications. The device also includes full address decoding, on-chip separate data in and noninverting data out lines, and an active LOW Chip Select Input.

The 100470A is compatible with the 100K ECL families and includes on-chip voltage and temperature compensation.

Ordering information can be found on the following page.

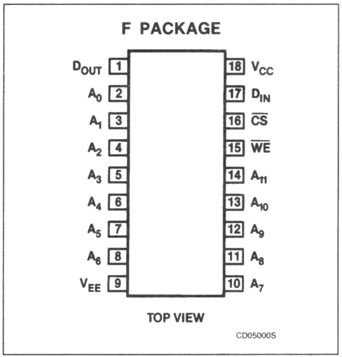
### FEATURES

- **Organization: 4096 words by 1 bit**
- **Fully compatible with 100K ECL families**
- **Operating temperature: 0°C to +85°C**
- **Address access time:**
  - **100470A: 15ns max**
- **Low supply current of 150mA max**
- **Read cycle time:**
  - **100470A: 15ns max**

### APPLICATIONS

- **High speed scratch pad**
- **Control and buffer storage**

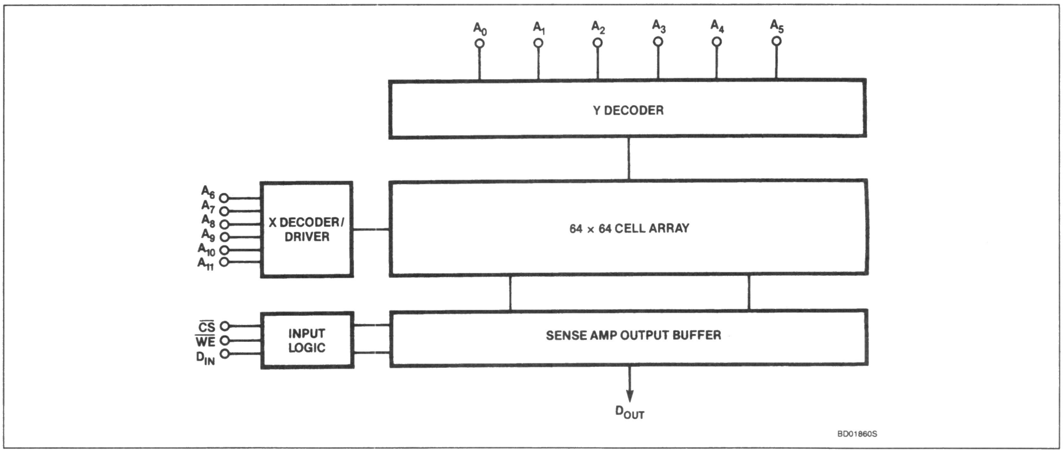
### PIN CONFIGURATION


F PACKAGE
$D_{OUT}$ 1
$A_0$ 2
$A_1$ 3
$A_2$ 4
$A_3$ 5
$A_4$ 6
$A_5$ 7
$A_6$ 8
$V_{EE}$ 9
18 $V_{CC}$
17 $D_{IN}$
16 $\overline{CS}$
15 $\overline{WE}$
14 $A_{11}$
13 $A_{10}$
12 $A_9$
11 $A_8$
10 $A_7$
TOP VIEW
CD05000S

### ABSOLUTE MAXIMUM RATINGS

| PARAMETER | | RATING | UNIT |
|---|---|---|---|
| $V_{EE}$ | Supply voltage | +0.5 to −7 | $V_{dc}$ |
| $V_{IN}$ | Input voltage | +0.5 to $V_{EE}$ | |
| $I_O$ | Output current | −30 | mA |
| $T_A$ | Operating | 0 to +85 | °C |
| $T_{STG}$ | Storage | −55 to +150 | |

### BLOCK DIAGRAM


$A_0$
$A_1$
$A_2$
$A_3$
$A_4$
$A_5$
Y DECODER
$A_6$
$A_7$
$A_8$
$A_9$
$A_{10}$
$A_{11}$
X DECODER/ DRIVER
64 × 64 CELL ARRAY
$\overline{CS}$
$\overline{WE}$
$D_{IN}$
INPUT LOGIC
SENSE AMP OUTPUT BUFFER
$D_{OUT}$
BD01860S

# 4K-Bit ECL Bipolar RAM (4096 × 1) 100470A

## ORDERING CODE

| DESCRIPTION | ORDER CODE |
|---|---|
| Ceramic Dual Inline<br>300mil wide 18-pin | 100470A F |

## DC ELECTRICAL CHARACTERISTICS $V_{CC} = 0V$, $V_{EE} = -4.5V \pm 5\%$, $R_L = 50\Omega$ to $-2V$, $T_A = 0°C$ to $85°C$

| PARAMETER | | TEST CONDITIONS | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| **Input voltage** | | | | | | |
| $V_{IL}$ | Low | | -1.810 | | -1.475 | V |
| $V_{IH}$ | High | | -1.165 | | -0.880 | |
| **Output voltage** | | | | | | |
| $V_{OL}$ | Low | $V_{IL}$ = Min | -1.810 | -1.715 | -1.620 | V |
| $V_{OH}$ | High | $V_{IH}$ = Max | -1.025 | -0.955 | -0.880 | |
| $V_{OLT}$ | Threshold LOW | $V_{IL}$ = Max | | | -1.610 | |
| $V_{OHT}$ | Threshold HIGH | $V_{IH}$ = Min | -1.035 | | | |
| **Input current** | | | | | | |
| $I_{IL}$ | Low | $V_{IL}$ = Min | -50 | | | μA |
| $I_{IL}$ | $\overline{CS}$ | $V_{IL}$ = Min | +0.5 | | | |
| $I_{IH}$ | High | $V_{IH}$ = Max | | | 220 | |
| $I_{EE}$ | Supply current | | | | 150 | mA |

**NOTES:**
1. Voltages are defined with respect to ground, pin 18.
2. Unit is in a test socket or mounted in a printed circuit board with transverse air flow > 400 ft/min.
3. DC limits apply after thermal equilibrium has been established.
4. For current measurement, maximum is defined as the maximum absolute value.

## AC ELECTRICAL CHARACTERISTICS $V_{CC} = 0V$, $V_{EE} = -4.5V \pm 5\%$, $R_L = 50\Omega$ to $-2V$, $T_A = 0°C$ to $85°C$

| PARAMETER | | LIMITS | | | UNIT |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $T_{AA}$ | Address access time | | | 15 | ns |
| $T_{RCS}$ | Chip select recovery time | | | 5 | |
| $T_{ACS}$ | Chip select access time | | | 5 | |
| $T_{WD}$ | Write disable time | | | 6 | |
| $T_{WPW}$ | Write pulse width | 10 | | | |
| $T_{WR}$ | Write recovery time | | | 10 | |
| $T_{WHA}$ | Address hold time | 3 | | | |
| $T_{WHCS}$ | Chip select hold time | 3 | | | |
| $T_{WHD}$ | Data hold time | 3 | | | |
| $T_{WSA}$ | Address set-up time | 3 | | | |
| $T_{WSCS}$ | Chip select set-up time | 3 | | | |
| $T_{WSD}$ | Data set-up time | 3 | | | |
| $t_f$ | Output fall time | | 1.5 | | |
| $t_r$ | Output rise time | | 1.5 | | |
| **Capacitance** | | | | | |
| $C_{IN}$ | Input | | | 8 | pF |
| $C_{OUT}$ | Output | | | 8 | |

**NOTES:**
1. AC limits apply after thermal equilibrium has been established.
2. Unit is in a test socket or mounted on a printed circuit board with transverse air flow > 400 ft/min.
3. Output fall and rise times are measured between 20% and 80% points.
4. All propagation measurements to output are measured from 50% of the input pulse to 50% output level.

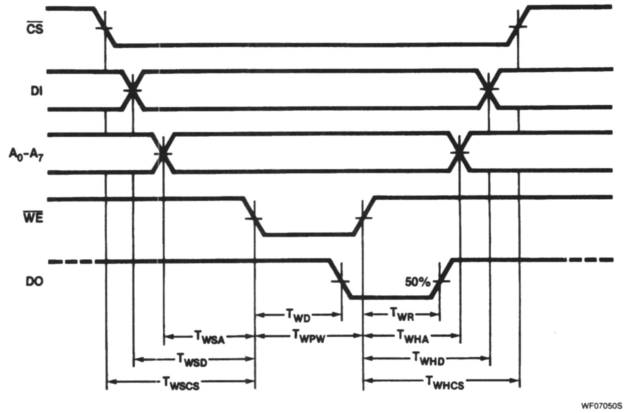
## 4K-Bit ECL Bipolar RAM (4096 × 1) 100470A

### TRUTH TABLE

| MODE | INPUTS | | | OUTPUTS |
|---|---|---|---|---|
| | $\overline{CS}$ | $\overline{WE}$ | $D_{IN}$ | |
| Disable | H | X | X | L |
| Write 0 | L | L | L | L |
| Write 1 | L | L | H | L |
| Read | L | H | X | $D_{OUT}$ |

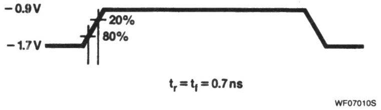
**NOTES:**
H = HIGH voltage level
L = LOW voltage level
X = Don't care

### TIMING DIAGRAMS



$\overline{CS}$
DI
$A_0$-$A_7$
$\overline{WE}$
DO
50%
$T_{WD}$
$T_{WR}$
$T_{WSA}$
$T_{WPW}$
$T_{WHA}$
$T_{WSD}$
$T_{WHD}$
$T_{WSCS}$
$T_{WHCS}$
WF07050S

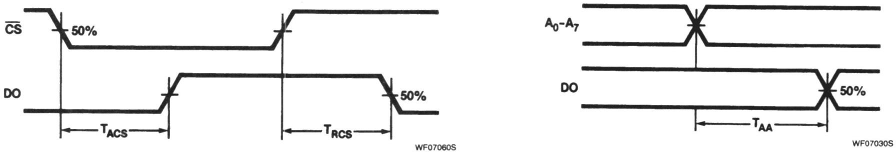
**Write Mode**



−0.9V
−1.7V
20%
80%
$t_r = t_f = 0.7ns$
WF07010S

**NOTE:**
All timing measurements referenced to 50% of input levels.

**Input Levels**



$\overline{CS}$
50%
DO
50%
$T_{ACS}$
$T_{RCS}$
WF07060S
$A_0$-$A_7$
DO
50%
$T_{AA}$
WF07030S

**Read Mode**

Signetics

**Bipolar Memory Products**

# 100474A
## 4K-Bit ECL Bipolar RAM

***Preliminary Specification***

## DESCRIPTION

The 100474A device is a 1024 words by 4 bits fully decoded Read/Write Random Access Memory, designed for high speed scratch pad, control, and buffer storage applications. The device also includes full address decoding, on-chip separate data in and noninverting data out lines.

The 100474A, with its voltage and temperature compensation, is compatible with the 100K ECL families.

Ordering information can be found on the following page.

## FEATURES

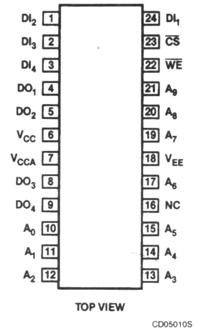
- **Organization: 1024 words by 4 bits**
- **Fully compatible with 100K ECL families**
- **Operating temperature: 0°C to +85°C**
- **Address access time:**
  - **100474A: 15ns max**
- **Low supply current of 210mA max**
- **Read Cycle time:**
  - **100474A: 15ns**

## APPLICATIONS

- **High speed scratch pad**
- **Control and buffer storage**

## PIN CONFIGURATION

**F PACKAGE**

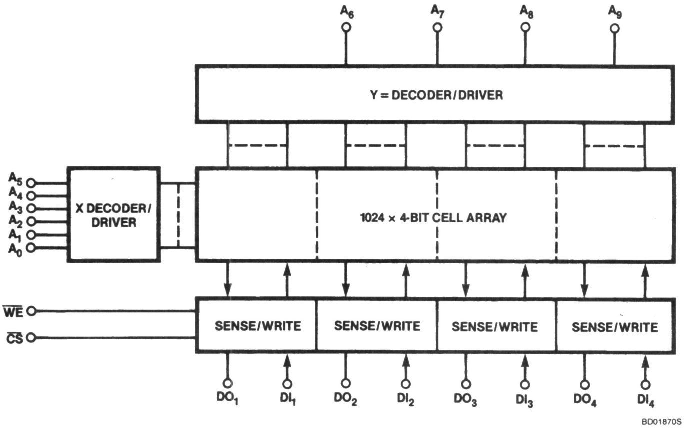


DI2 1
DI3 2
DI4 3
DO1 4
DO2 5
VCC 6
VCCA 7
DO3 8
DO4 9
A0 10
A1 11
A2 12
24 DI1
23 CS
22 WE
21 A9
20 A8
19 A7
18 VEE
17 A6
16 NC
15 A5
14 A4
13 A3
TOP VIEW
CD05010S

## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | | RATING | UNIT |
|---|---|---|---|
| $V_{EE}$ | Supply voltage | +0.5 to −7 | $V_{dc}$ |
| $V_{IN}$ | Input voltage | +0.5 to $V_{EE}$ | |
| $I_O$ | Output current | −30 | mA |
| $T_A$ | Operating | 0 to +85 | °C |
| $T_{stg}$ | Storage | −55 to +150 | |

## BLOCK DIAGRAM



A6
A7
A8
A9
Y = DECODER/DRIVER
A5
A4
A3
A2
A1
A0
X DECODER/ DRIVER
1024 × 4-BIT CELL ARRAY
WE
CS
SENSE/WRITE
SENSE/WRITE
SENSE/WRITE
SENSE/WRITE
DO1
DI1
DO2
DI2
DO3
DI3
DO4
DI4
BD01870S

## ORDERING CODE

| DESCRIPTION | ORDER CODE |
|---|---|
| Ceramic Dual Inline<br>400mil wide 24-pin | 100474A F |

## DC ELECTRICAL CHARACTERISTICS $V_{CC}$ = 0V, $V_{EE}$ = −4.5V± 5%, $R_L$ = 50Ω to −2V, $T_A$ = 0°C to 85°C

| PARAMETER | | TEST CONDITIONS | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| **Input voltage** | | | | | | |
| $V_{IL}$ | Low | | −1.810 | | −1.475 | V |
| $V_{IH}$ | High | | −1.165 | | −0.880 | |
| **Output voltage** | | | | | | |
| $V_{OL}$ | Low | $V_{IL}$ = Min | −1.810 | −1.715 | −1.620 | V |
| $V_{OH}$ | High | $V_{IH}$ = Max | −1.025 | −0.955 | −0.880 | |
| $V_{OLT}$ | Threshold LOW | $V_{IL}$ = Max | | | −1.610 | |
| $V_{OHT}$ | Threshold HIGH | $V_{IH}$ = Min | −1.035 | | | |
| **Input current** | | | | | | |
| $I_{IL}$ | Low | $V_{IL}$ = Min | −50 | | | µA |
| $I_{IL}$ | $\overline{BS}$ | $V_{IL}$ = Min | +0.5 | | | |
| $I_{IH}$ | High | $V_{IH}$ = Max | | | 220 | |
| $I_{EE}$ | Supply current | | | | 210 | mA |

**NOTES:**
1. Voltages are defined with respect to ground, pins 6 and 7.
2. Unit is in a test socket or mounted in a printed circuit board with transverse air flow > 400 ft/min.
3. DC limits apply after thermal equilibrium has been established.
4. For current measurement, maximum is defined as the maximum absolute value.

## AC ELECTRICAL CHARACTERISTICS $V_{CC}$ = 0V, $V_{EE}$ = −4.5V± 5%, $R_L$ = 50Ω to −2V, $T_A$ = 0°C to 85°C

| PARAMETER | | LIMITS | | | UNIT |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $T_{AA}$ | Address access time | | | 15 | ns |
| $T_{RCS}$ | Chip select recovery time | | | 5 | |
| $T_{ACS}$ | Chip select access time | | | 5 | |
| $T_{WD}$ | Write disable time | | | 6 | |
| $T_{WPW}$ | Write pulse width | 10 | | | |
| $T_{WR}$ | Write recovery time | | | 10 | |
| $T_{WHA}$ | Address hold time | 3 | | | |
| $T_{WHCS}$ | Chip select hold time | 3 | | | |
| $T_{WHD}$ | Data hold time | 3 | | | |
| $T_{WSA}$ | Address set-up time | 3 | | | |
| $T_{WSCS}$ | Chip select set-up time | 3 | | | |
| $T_{WSD}$ | Data set-up time | 3 | | | |
| $t_f$ | Output fall time | | 1.5 | | |
| $t_r$ | Output rise time | | 1.5 | | |
| **Capacitance** | | | | | |
| $C_{IN}$ | Input | | | 8 | pF |
| $C_{OUT}$ | Output | | | 8 | |

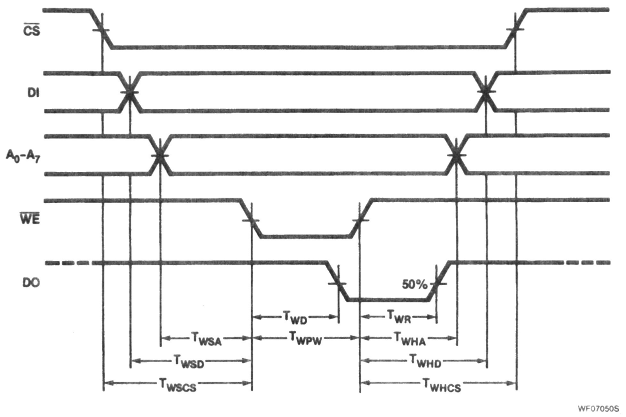
**NOTES:**
1. AC limits apply after thermal equilibrium has been established.
2. Unit is in a test socket or mounted on a printed circuit board with transverse air flow > 400 ft/min.
3. Output fall and rise times are measured between 20% and 80% points.
4. All propagation measurements to output are measured from 50% of the input pulse to 50% output level.

## TRUTH TABLE

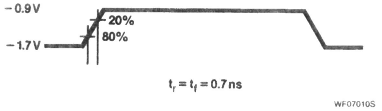
| MODE | INPUTS | | | OUTPUTS |
|---|---|---|---|---|
| | $\overline{CS}$ | $\overline{WE}$ | $D_{IN}$ | |
| Disable | H | X | X | L |
| Write 0 | L | L | L | L |
| Write 1 | L | L | H | L |
| Read | L | H | X | $D_{OUT}$ |

**NOTES:**
H = HIGH voltage level
L = LOW voltage level
X = Don't care

## TIMING DIAGRAMS

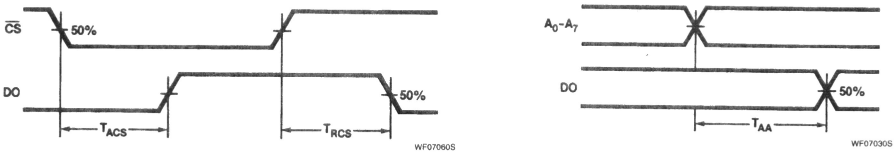

$\overline{CS}$
DI
$A_0$-$A_7$
$\overline{WE}$
DO
50%
$T_{WD}$
$T_{WR}$
$T_{WSA}$
$T_{WPW}$
$T_{WHA}$
$T_{WSD}$
$T_{WHD}$
$T_{WSCS}$
$T_{WHCS}$
WF07050S

**Write Mode**


−0.9 V
−1.7 V
20%
80%
$t_r = t_f = 0.7\,ns$
WF07010S

NOTE:
All timing measurements referenced to 50% of input levels.

**Input Levels**


$\overline{CS}$
50%
DO
50%
$T_{ACS}$
$T_{RCS}$
WF07060S
$A_0$-$A_7$
DO
50%
$T_{AA}$
WF07030S

**Read Mode**

Signetics

ECL Products

# Section 9
# Package Outlines

## INDEX

Data Information ........ 9-3
Soldering Recommendations ........ 9-3

**Signetics**

# Package Outlines and Soldering Recommendations

**ECL Products**

## INTRODUCTION

The following information applies to all packages unless otherwise specified on individual package outline drawings.

### General

1. Dimensions are shown in metric units (Millimeters) and English units (Inches).
2. Thermal resistance values are determined by temperature-sensitive parameter (TSP) method. This method uses the forward voltage drop of a calibrated diode to measure the change in junction temperature due to a known power application. The substrate diode of a bipolar technology device is generally the diode used in these tests. Die size and test environment have significant effects on thermal resistance values.

### Plastic DIP

3. Lead material: Copper Alloy, solder (63% Sn/37% Pb) dipped.
4. Body material: Plastic (Epoxy).
5. Index in top center denotes lead No. 1 for Plastic Dual-in-Line packages.
6. Body dimensions do not include molding flash.

### Ceramic DIP and Flat Pack

7. Lead material: Alloy 42, Tin-plated or solder (60% Sn/40% Pb) dipped.
8. Body material: Alumina with glass seal at leads.
9. Lid material: Alumina, glass seal.

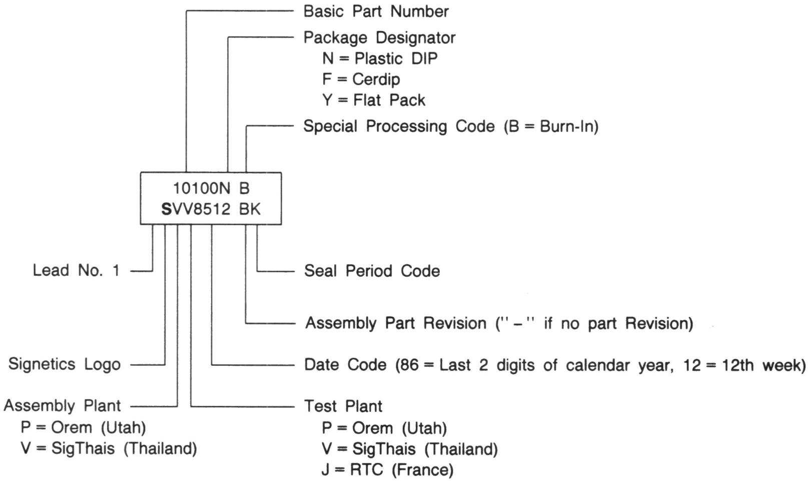
**ECL PACKAGE OUTLINES**

| PACKAGE TYPE | NUMBER OF LEADS | PACKAGE FEATURE | PACKAGE ORDERING CODE | PACKAGE OUTLINE CODE | THERMAL RESISTANCE $\theta_{JA}/_{JC}$ (°C/W) | DIE SIZE (SQUARE MILS) | TEST CONDITIONS | |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | **Test Ambient** | **Test Fixture** |
| Plastic (Copper Leadframe) | 16-pin | .300″ Lead row centers | N | NJ1 | 86/43 | 2,500 | Still air at room temp. | Device in Textool ZIF socket with 0.040 inch, stand-off. Accuracy: ± 15% |
| Ceramic | 16-pin | .400″ Lead row centers | F | FJ1* | 100/NA | 5,000 | Still air at room temp. | Device in Textool ZIF socket with 0.040 inch, stand-off. Accuracy: ± 15% |
| | 24-pin | | F | FN2 | 72/NA | 5,000 | | |
| Ceramic | 18-pin | .300″ Lead row centers | F | FK1 | 73/27 | 10,000 | Still air at room temp. | Device in Textool ZIF socket with 0.040 inch, stand-off. Accuracy: ± 15% |
| Flat pack | 24-pin | | Y | YN1 | 130/NA | 5,000 | Still air at room temp. | Device in Texttool socket with plastic carrier. Accuracy: ± 15% |

* = Package outline not available at time of publication
NA = Characteristics not available at time of publication

# Package Outlines and Soldering Recommendations

10. Package Symbolization for Plastic and Ceramic DIP, Top Side



Basic Part Number

Package Designator
N = Plastic DIP
F = Cerdip
Y = Flat Pack

Special Processing Code (B = Burn-In)

10100N B
**S**VV8512 BK

Lead No. 1

Seal Period Code

Assembly Part Revision ("–" if no part Revision)

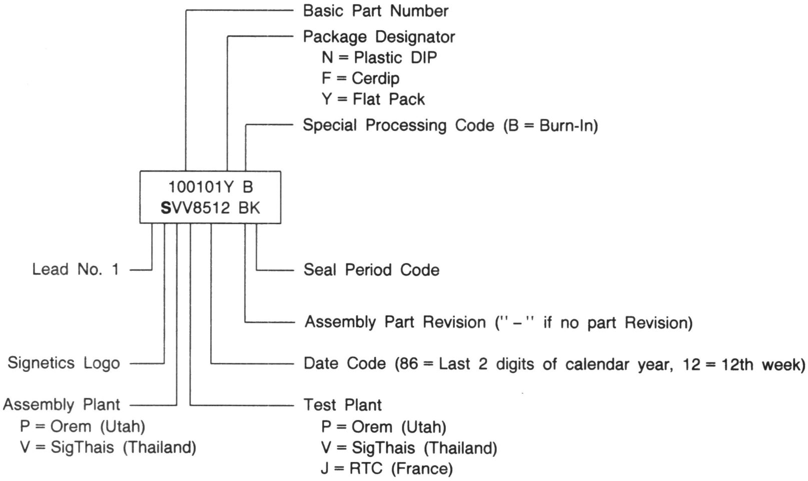
Signetics Logo

Date Code (86 = Last 2 digits of calendar year, 12 = 12th week)

Assembly Plant
P = Orem (Utah)
V = SigThais (Thailand)

Test Plant
P = Orem (Utah)
V = SigThais (Thailand)
J = RTC (France)

11. Package Symbolization for Flat Pack Top Side



Basic Part Number

Package Designator
N = Plastic DIP
F = Cerdip
Y = Flat Pack

Special Processing Code (B = Burn-In)

100101Y B
**S**VV8512 BK

Lead No. 1

Seal Period Code

Assembly Part Revision ("–" if no part Revision)

Signetics Logo

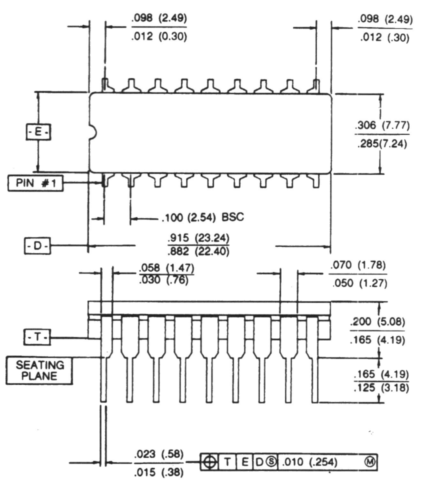
Date Code (86 = Last 2 digits of calendar year, 12 = 12th week)

Assembly Plant
P = Orem (Utah)
V = SigThais (Thailand)

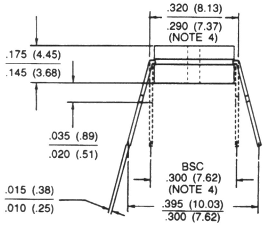
Test Plant
P = Orem (Utah)
V = SigThais (Thailand)
J = RTC (France)

# Package Outlines and Soldering Recommendations

## FK1 HERMETIC CDIP-18


.098 (2.49)
.012 (0.30)
.098 (2.49)
.012 (.30)
-E-
.306 (7.77)
.285(7.24)
PIN #1
.100 (2.54) BSC
-D-
.915 (23.24)
.882 (22.40)
.058 (1.47)
.030 (.76)
.070 (1.78)
.050 (1.27)
-T-
SEATING PLANE
.200 (5.08)
.165 (4.19)
.165 (4.19)
.125 (3.18)
.023 (.58)
.015 (.38)
T E D Ⓢ .010 (.254) Ⓜ

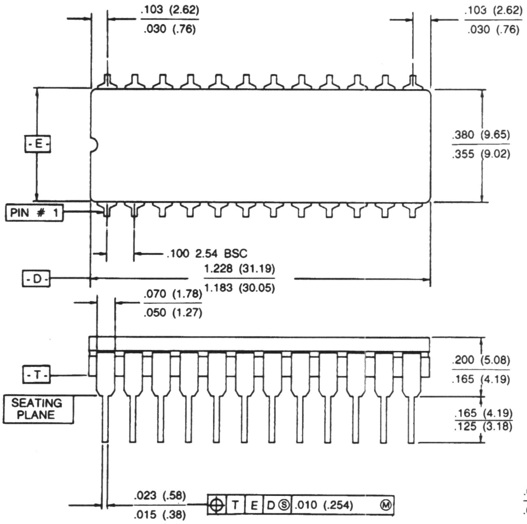
**NOTES:**
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M – 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #18 when viewed from the top.


.320 (8.13)
.290 (7.37)
(NOTE 4)
.175 (4.45)
.145 (3.68)
.035 (.89)
.020 (.51)
BSC
.300 (7.62)
(NOTE 4)
.015 (.38)
.010 (.25)
.395 (10.03)
.300 (7.62)

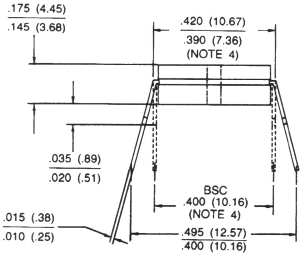
853-0583/081594

PO00470S

## FN2 HERMETIC CDIP-24


.103 (2.62)
.030 (.76)
.103 (2.62)
.030 (.76)
-E-
.380 (9.65)
.355 (9.02)
PIN # 1
.100 2.54 BSC
-D-
1.228 (31.19)
1.183 (30.05)
.070 (1.78)
.050 (1.27)
-T-
SEATING PLANE
.200 (5.08)
.165 (4.19)
.165 (4.19)
.125 (3.18)
.023 (.58)
.015 (.38)
T E D Ⓢ .010 (.254) Ⓜ

**NOTES:**
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M – 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #24 when viewed from the top.

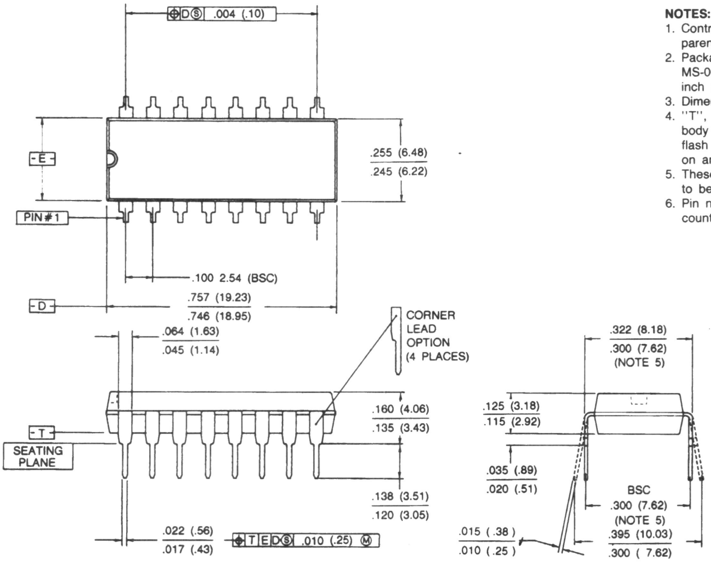

.175 (4.45)
.145 (3.68)
.420 (10.67)
.390 (7.36)
(NOTE 4)
.035 (.89)
.020 (.51)
BSC
.400 (10.16)
(NOTE 4)
.015 (.38)
.010 (.25)
.495 (12.57)
.400 (10.16)

853-0587/081594

PO00450S

# Package Outlines and Soldering Recommendations

## NJ1 PLASTIC PDIP-16


.004 (.10)
D
E
PIN #1
.255 (6.48)
.245 (6.22)
.100 2.54 (BSC)
.757 (19.23)
.746 (18.95)
.064 (1.63)
.045 (1.14)
CORNER
LEAD
OPTION
(4 PLACES)
T
SEATING PLANE
.160 (4.06)
.135 (3.43)
.138 (3.51)
.120 (3.05)
.022 (.56)
.017 (.43)
T E D .010 (.25) M
.125 (3.18)
.115 (2.92)
.035 (.89)
.020 (.51)
.015 (.38)
.010 (.25)
.322 (8.18)
.300 (7.62)
(NOTE 5)
BSC
.300 (7.62)
(NOTE 5)
.395 (10.03)
.300 ( 7.62)

**NOTES:**
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AA for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 16 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from the top.

853-0406/081232

PO00280S

Signetics

# Section 10
# Numerical Index

ECL Products

# Numerical Index

## ECL Products

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## 100K SERIES

| | | |
|---|---|---|
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